NTHLD040N65S3HF

MOSFET – Power, N-Channel, SUPERFET® III, FRFET®, 650 V, 65 A, 40 mΩ

ON Semiconductor®

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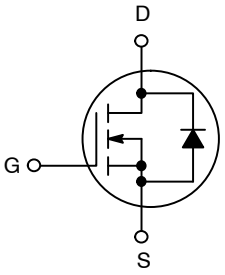
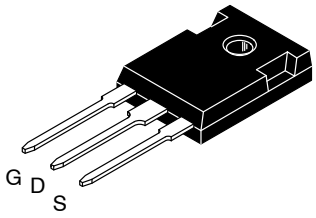
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	40 mΩ @ 10 V	65 A





TO−247AD
CASE 340AL

Description

SUPERFET III MOSFET is ON Semiconductor's brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 32 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 159 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 1367 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar

MARKING DIAGRAM

A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current	– Continuous (T_C = 25°C)	65	A
		– Continuous (T_C = 100°C)	45	
I_{DM}	Drain Current	– Pulsed (Note 1)	162.5	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1009	mJ
I_{AS}	Avalanche Current (Note 2)		9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		4.46	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25°C)	446	W
		– Derate Above 25°C	3.57	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 9 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 32.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.28	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTHLD040N65S3HF	NTHLD040N65S3HF	TO−247	Tube	N/A	N/A	30 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 15 mA, Referenced to 25°C		0.63		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			10	μA
		V_{DS} = 520 V, T_C = 125°C		213		
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 2.1 mA	3.0		5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 32.5 A		32	40	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 32.5 A		48		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		5945		pF
C_{oss}	Output Capacitance			135		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		1367		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		245		pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 32.5 A, V_{GS} = 10 V (Note 4)		159		nC
Q_{gs}	Gate to Source Gate Charge			46		nC
Q_{gd}	Gate to Drain “Miller” Charge			64		nC
ESR	Equivalent Series Resistance	f = 1 MHz		1.2		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 32.5 A, V_{GS} = 10 V, R_g = 2.2 Ω (Note 4)		40		ns
t_r	Turn-On Rise Time			32		ns
$t_{d(off)}$	Turn-Off Delay Time			102		ns
t_f	Turn-Off Fall Time			26		ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current				65	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current				162.5	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 32.5 A			1.3	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 32.5 A, dI_F/dt = 100 A/μs		160		ns
Q_{rr}	Reverse Recovery Charge			874		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

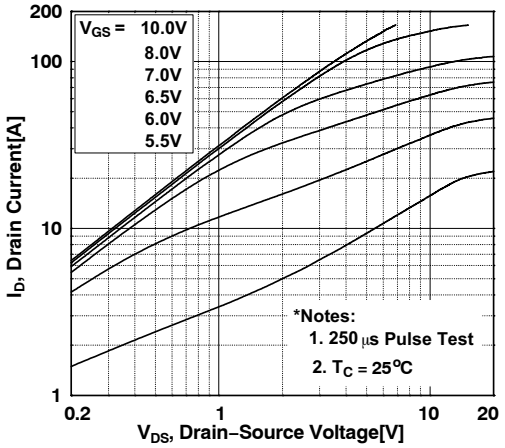


Figure 1. On−Region Characteristics

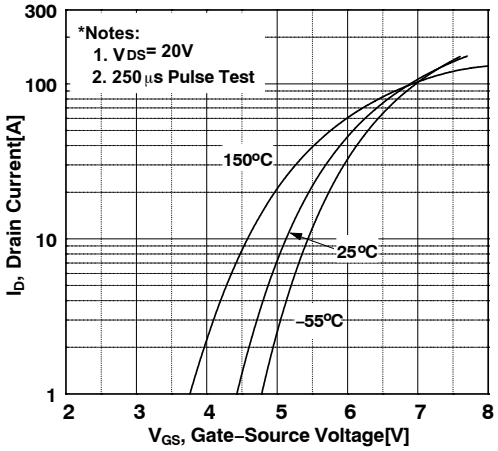


Figure 2. Transfer Characteristics

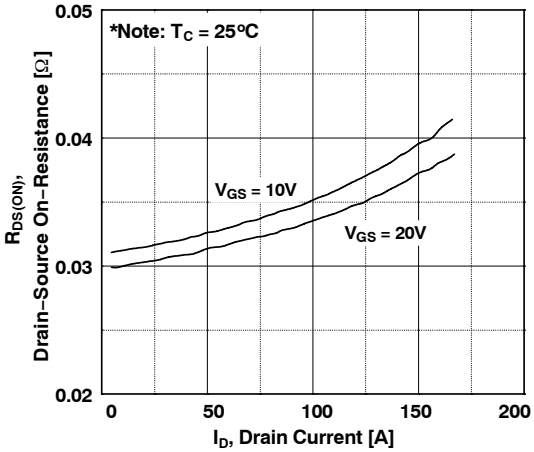


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

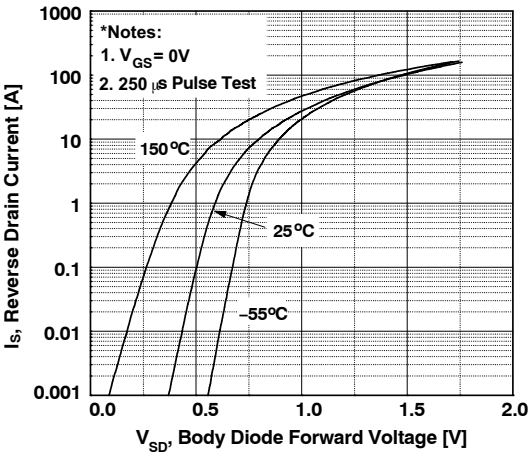


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

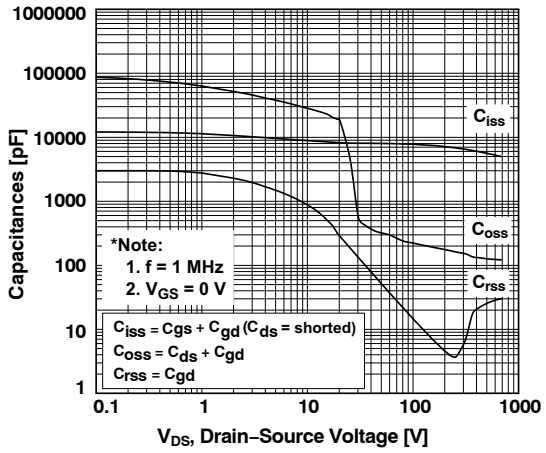


Figure 5. Capacitance Characteristics

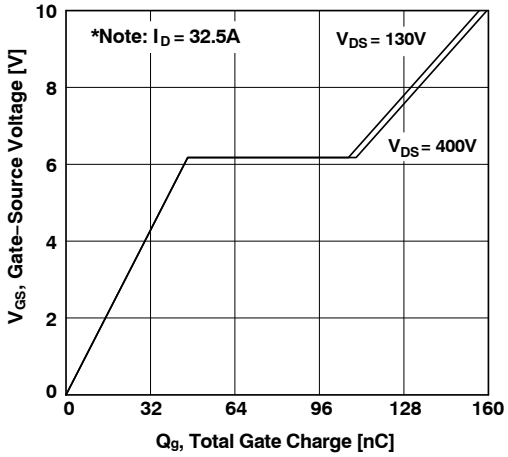


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

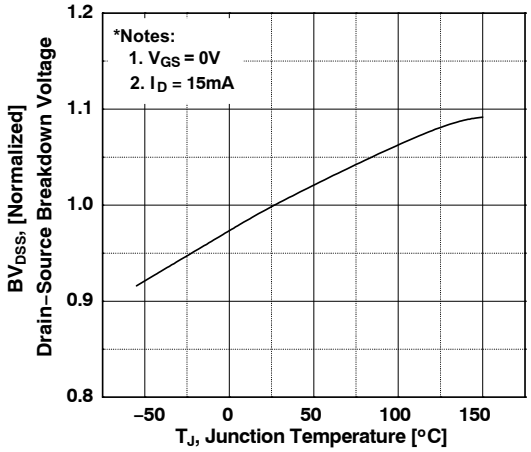


Figure 7. Breakdown Voltage Variation vs. Temperature

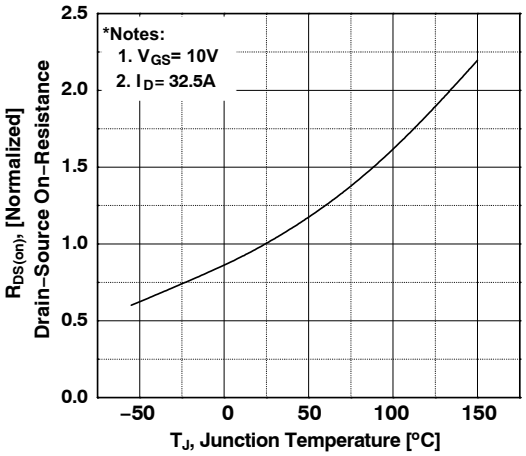


Figure 8. On−Resistance Variation vs. Temperature

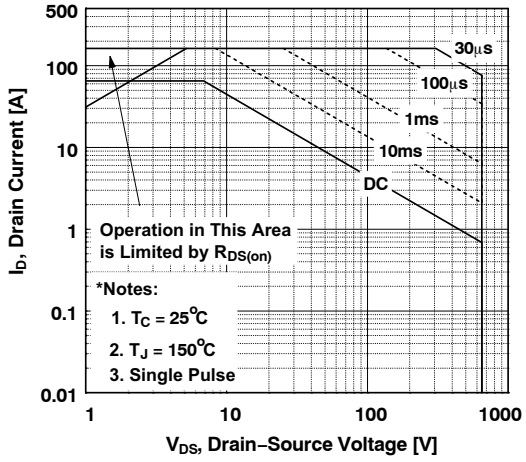


Figure 9. Maximum Safe Operating Area

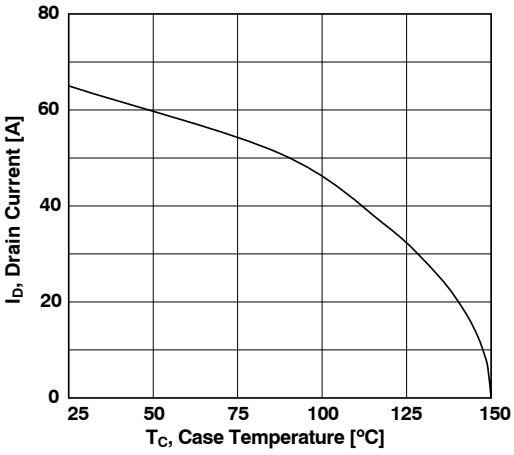


Figure 10. Maximum Drain Current vs. Case Temperature

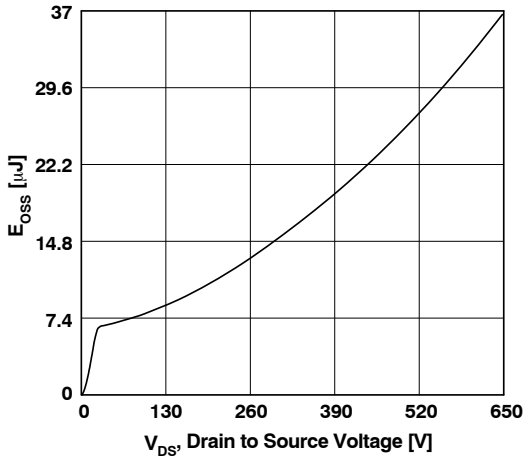


Figure 11. Eoss vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

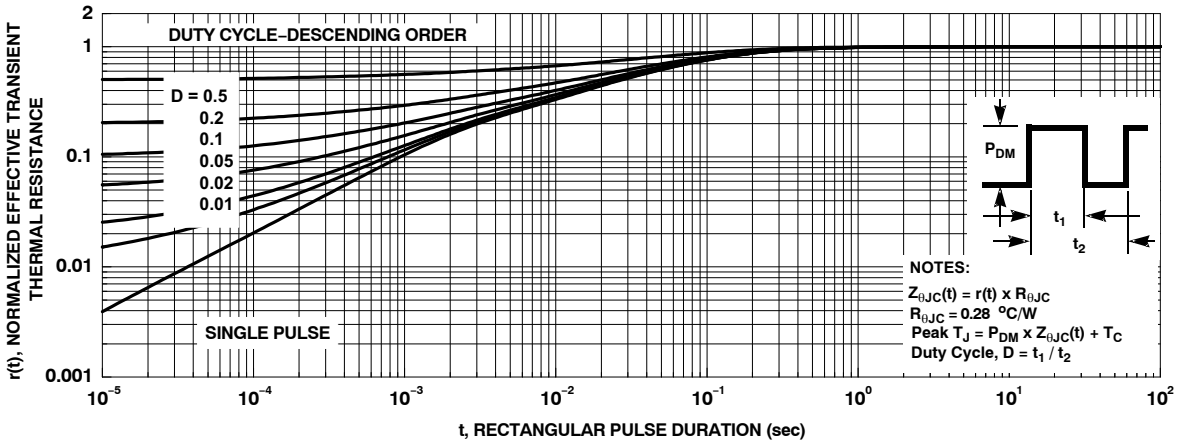


Figure 12. Transient Thermal Response Curve

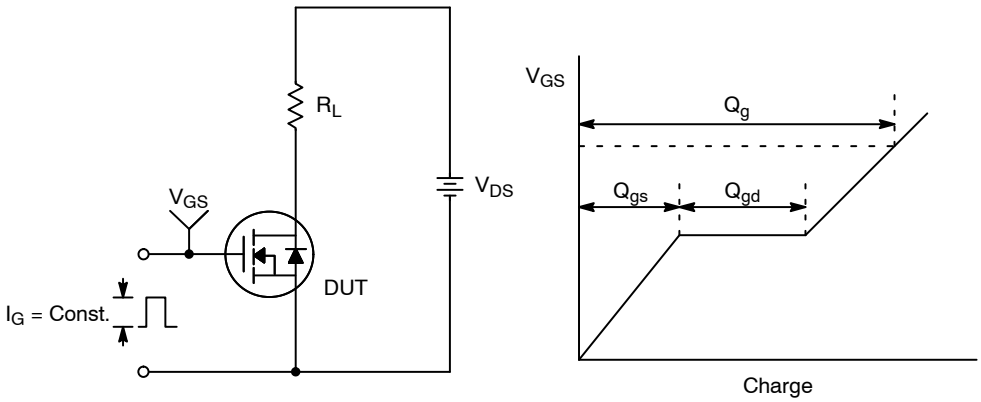


Figure 13. Gate Charge Test Circuit & Waveform

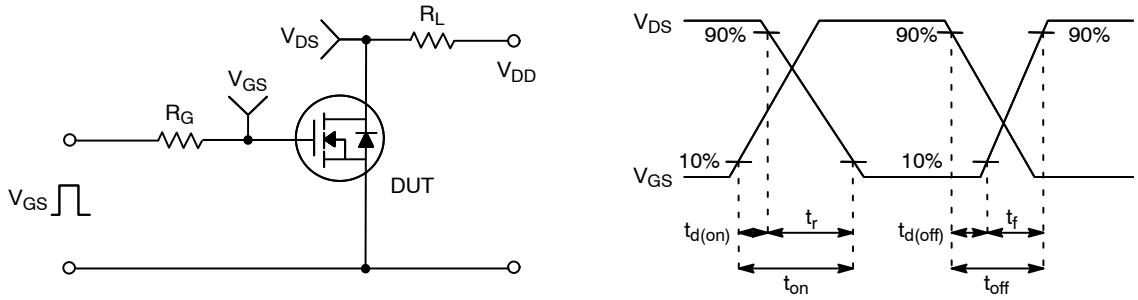


Figure 14. Resistive Switching Test Circuit & Waveforms

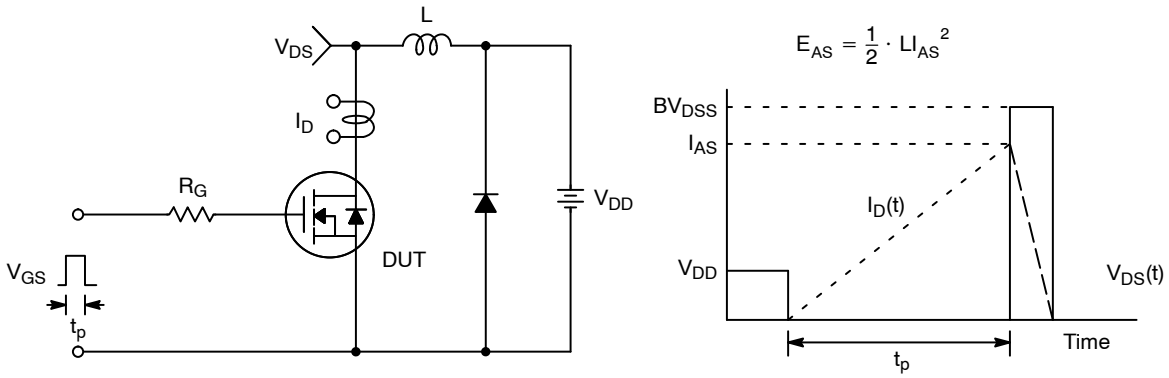


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

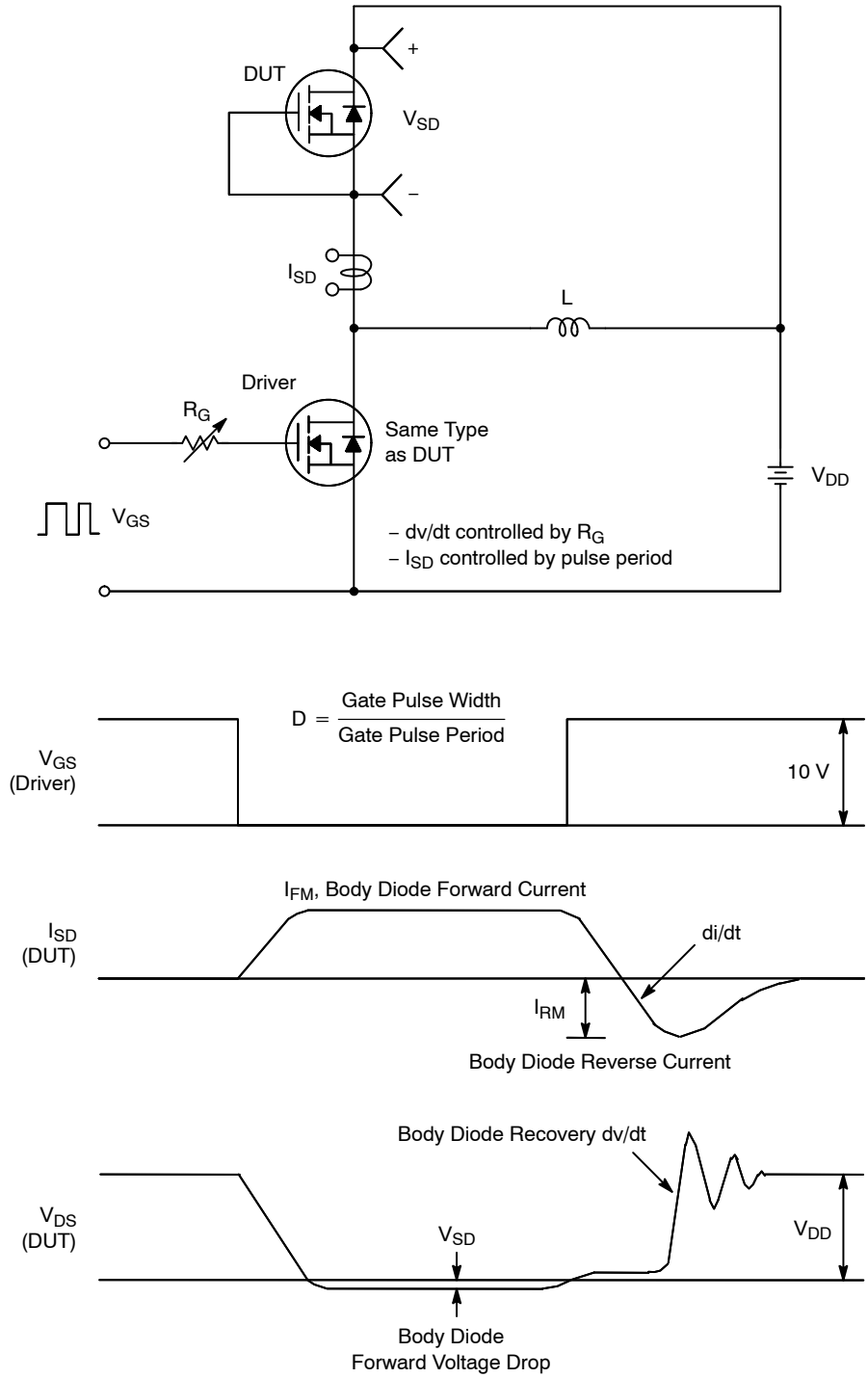


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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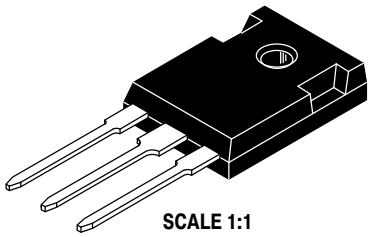
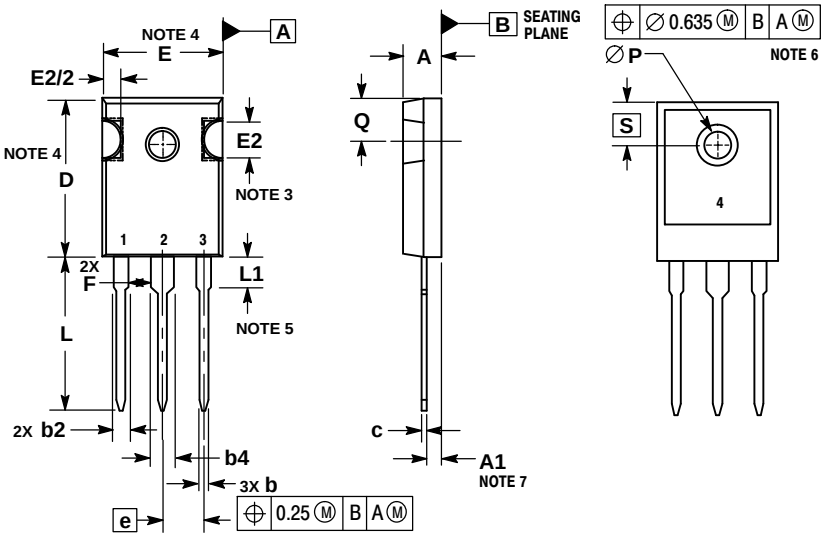
DATE 17 MAR 2017



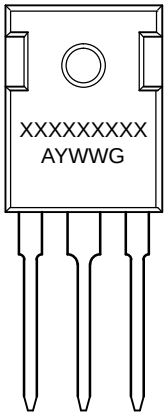
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. SLOT REQUIRED, NOTCH MAY BE ROUNDED.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
5. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.
6. ∅P SHALL HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM DIAMETER OF 3.91.
7. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.

	MILLIMETERS	
DIM	MIN	MAX
A	4.70	5.30
A1	2.20	2.60
b	1.07	1.33
b2	1.65	2.35
b4	2.60	3.40
c	0.45	0.68
D	20.80	21.34
E	15.50	16.25
E2	4.32	5.49
e	5.45 BSC	
F	2.655	---
L	19.80	20.80
L1	3.81	4.32
P	3.55	3.65
Q	5.40	6.20
S	6.15 BSC	

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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ISSUE	REVISION	DATE
O	RELEASED TO PRODUCTION. REQ. BY D. TRUHITTE.	26 JUN 2013
A	REMOVED DIMENSION A2. REQ. BY S. BRUTCHER.	01 AUG 2013
B	MODIFED DIMENSIONS D AND L1. REQ. BY C. ENRIQUEZ.	08 MAR 2016
C	ADDED DIMENSION F. REQ. BY C. ENRIQUEZ.	30 NOV 2016
D	MODIFED DIMENSIONS b AND c. REQ. BY C. ENRIQUEZ.	17 MAR 2017

PUBLICATION ORDERING INFORMATION

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