MOSFET – Power, Single, N-Channel, μCool, WDFN, 2X2 mm 30 V, 7.8 A

Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88
- Lowest R_{DS(on)} in 2x2 mm Package
- 1.8 V R_{DS(on)} Rating for Operation at Low Voltage Logic Level Gate Drive
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- DC-DC Conversion
- Boost Circuits for LED Backlights
- Optimized for Battery and Load Management Applications in Portable Equipment such as, Cell Phones, PDA's, Media Players, etc.
- Low Side Load Switch for Noisy Environment

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage	Gate-to-Source Voltage			±12	V
Continuous Drain	Steady	T _A = 25°C	I _D	6.0	Α
Current (Note 1)	State $T_A = 85^{\circ}C$			4.4	
	t ≤ 5 s	T _A = 25°C		7.8	
Power Dissipation (Note 1)	Steady State T _A = 25°C		P _D	1.92	W
	t ≤ 5 s			3.3	
Continuous Drain	T _A = 25°C		I _D	3.6	Α
Current (Note 2)	Steady	T _A = 85°C		2.6	
Power Dissipation (Note 2)	State	T _A = 25°C	P _D	0.70	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	28	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	3.0	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

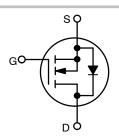
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX (Note 1)
	35 mΩ @ 4.5 V	
30 V	45 mΩ @ 2.5 V	7.8 A
	55 mΩ @ 1.8 V	



N-CHANNEL MOSFET

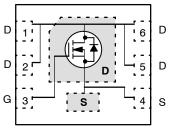


JA = Specific Device Code M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTLJS4114NT1G	WDFN6 (Pb-Free)	3000/Tape & Reel
NTLJS4114NTAG	WDFN6 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTLJS4114N
 Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces). Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm2, 2 oz Cu.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 3)	$R_{ heta JA}$	65	
Junction-to-Ambient – $t \le 5$ s (Note 3)	$R_{ heta JA}$	38	°C/W
Junction-to-Ambient - Steady State Min Pad (Note 4)	$R_{ heta JA}$	180	

- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
 Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

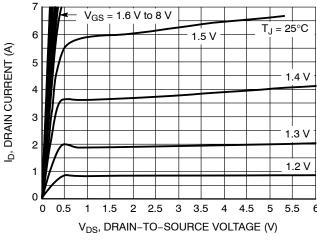
MOSFET ELECTRICAL CHARACTERISTICS (T_{.1} = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	าร	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 25	0 μΑ	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, Ref to 25°C			20		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	I_{DSS} $T_{J} = 25^{\circ}C$				1.0	μΑ
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	T _J = 85°C			10	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm$	12 V			±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 25$	50 μΑ	0.4	0.55	1.0	V
Negative Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J				3.18		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 2$	2.0 A		20.3	35	mΩ
		$V_{GS} = 2.5 \text{ V}, I_D = 2.5 \text{ V}$	2.0 A		25.8	45	1
		$V_{GS} = 1.8 \text{ V}, I_D = 1.8 \text{ V}$	1.8 A		35.2	55	1
Forward Transconductance	9 _{FS}	V _{DS} = 16 V, I _D = 2	2.0 A		8		S
CHARGES, CAPACITANCES AND GA	TE RESISTANO	CE			-	-	-
Input Capacitance	C _{ISS}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,} $ $V_{DS} = 15 \text{ V}$			650		pF
Output Capacitance	C _{OSS}				115.5		
Reverse Transfer Capacitance	C _{RSS}				70		
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V},$ $I_D = 2.0 \text{ A}$			8.5	13	nC
Threshold Gate Charge	Q _{G(TH)}				0.6		1
Gate-to-Source Charge	Q_{GS}				0.9		1
Gate-to-Drain Charge	Q_{GD}				2.1		1
Gate Resistance	R_{G}				3.0		Ω
SWITCHING CHARACTERISTICS (No	te 6)						
Turn-On Delay Time	t _{d(ON)}				5		ns
Rise Time	t _r	$V_{GS} = 4.5 \text{ V}, V_{DD} =$	15 V,		9		1
Turn-Off Delay Time	t _{d(OFF)}	V_{GS} = 4.5 V, V_{DD} = 15 V, I_D = 2.0 A, R_G = 3.0 Ω			20		1
Fall Time	t _f				4		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS				-	-	-
Forward Recovery Voltage	V_{SD}	T _J = 25°C	T _J = 25°C		0.71	1.2	Ι,,
-	$V_{CC} = 0 \text{ V } \text{ IS} = 2.0 \text{ A}$	T _J = 85°C		0.58		· V	
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V}, d_{ISD}/d_t = 100 \text{ A}/\mu\text{s}, \\ I_S = 1.0 \text{ A}$			14	35	
Charge Time	t _a				8.0		ns
Discharge Time	t _b				6.0		1
Reverse Recovery Time	Q _{RR}				5.0		nC

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^{\circ}C$ unless otherwise noted)

 $V_{DS} \ge 10 \text{ V}$



T_J = 25°C

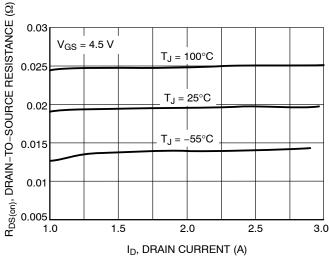
T_J = 25°C

T_J = -55°C

T_J = -55°C

Figure 1. On-Region Characteristics

V_{GS}, GATE-TO-SOURCE VOLTAGE (V) Figure 2. Transfer Characteristics



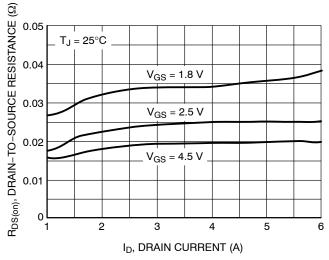


Figure 3. On-Resistance versus Drain Current

Figure 4. On-Resistance versus Drain Current and Gate Voltage

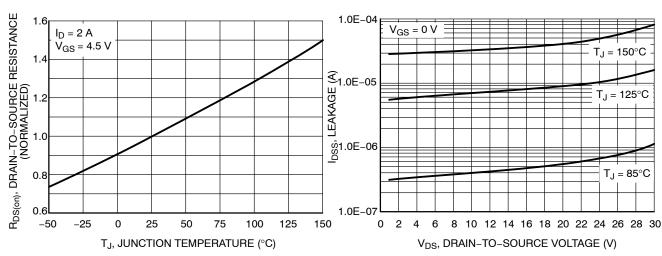
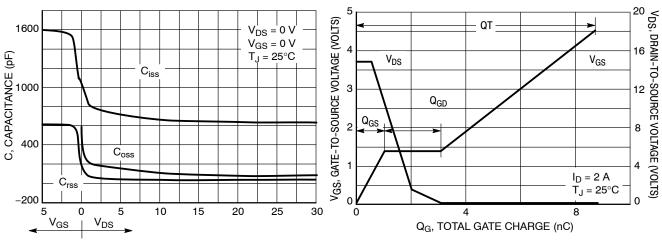


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^{\circ}C$ unless otherwise noted)



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (V)

Figure 7. Capacitance Variation

Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

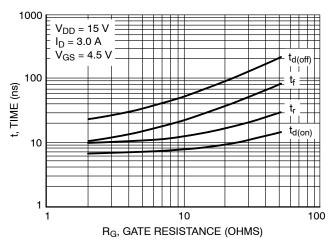


Figure 9. Resistive Switching Time Variation versus Gate Resistance

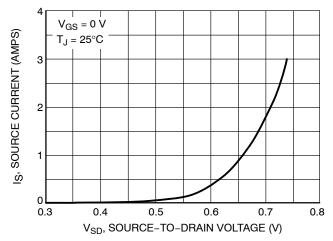


Figure 10. Diode Forward Voltage versus Current

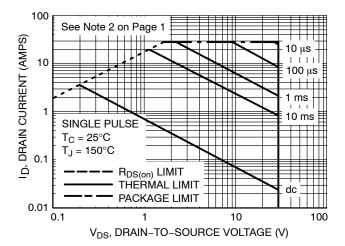


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES ($T_J = 25^{\circ}C$ unless otherwise noted)

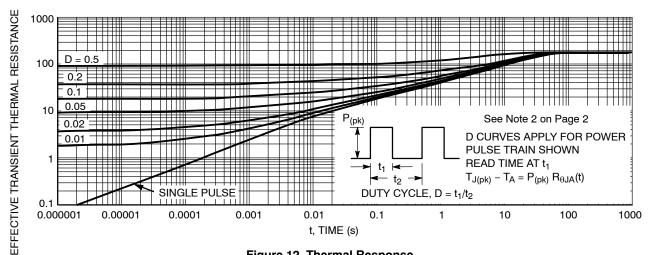
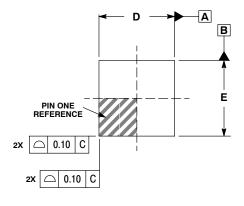


Figure 12. Thermal Response

PACKAGE DIMENSIONS

WDFN6 2x2 CASE 506AP **ISSUE B**



0.10 C



- SOURCE 4. DRAIN 5.
- DRAIN

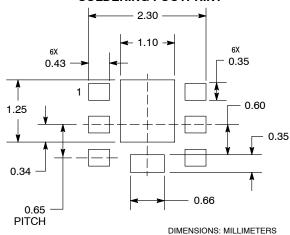
NOTES

- Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION b APPLIES TO PLATED TERMINAL AND
- DIMENSIONING AND TOLERANCING PER ASME
- IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
 COPLANARITY APPLIES TO THE EXPOSED PAD AS
- WELL AS THE TERMINALS.
 CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL
- LEAD IS CONNECTED TO TERMINAL LEAD # 4.
 6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

, _,				
	MILLIMETERS			
DIM	MIN	MAX		
Α	0.70	0.80		
A1	0.00	0.05		
A3	0.20	REF		
b	0.25	0.35		
b1	0.51	0.61		
D	2.00 BSC			
D2	1.00	1.20		
E	2.00 BSC			
E2	1.10	1.30		
е	0.65 BSC			
K	0.15 REF			
L	0.20	0.30		
L2	0.20	0.30		
J	0.27 REF			
J1	0.65 REF			

7X 🗀 0.08 С **A1** C SEATING PLANE D₂ е 6X L L₂ 3 Ш b1 6X 0.10 С A B **E2 #** С 0.05 Ш П NOTE 5 6X С Α В 0.10 Ф 0.05 С

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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