NTLUD3C20CZ

Product Preview

Small Signal MOSFET

12 V, Complementary, 2.0 x 2.0 mm UDFN Package

ON Semiconductor®

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Features

- Advanced Trench Complementary MOSFET
- Low RDS(on)
- Low Profile UDFN 2.0x2.0x0.55mm for Board Space Saving
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Load Switch
- Load Switch with Level Shift
- Optimized for Power Management in Ultra Portable Devices

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
N−Channel 12 V	23 mΩ @ 4.5 V	6.4 A
	26 mΩ @ 3.3 V	
	31 mΩ @ 2.5 V	
	59 mΩ @ 1.8 V	
P−Channel −12 V	44 mΩ @ −4.5 V	−4.6 A
	55 mΩ @ −3.3 V	
	75 mΩ @ −2.5 V	
	175 mΩ @ −1.8 V	

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

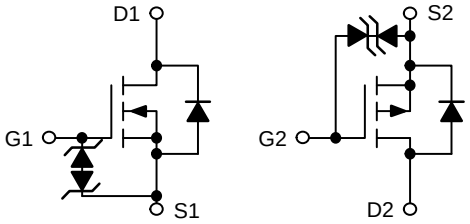
Parameter			Symbol	Value	Unit
Drain−to−Source Voltage		NMOS	V_{DSS}	12	V
		PMOS		12	
Gate−to−Source Voltage		NMOS	V_{GS}	±8.0	V
		PMOS		±8.0	
N−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	6.4	A
		T_A = 85°C		4.6	
	t ≤ 5 s	T_A = 25°C		8.1	
P−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−4.6	A
		T_A = 85°C		−3.3	
	t ≤ 5 s	T_A = 25°C		−5.9	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.40	W
	t ≤ 5 s	T_A = 25°C		2.29	W
Pulsed Drain Current	NMOS	t_p = 10 μs	I_{DM}	21	A
	PMOS			14	
Source Current (Body Diode)			I_S	1.6	A
				−1.6	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

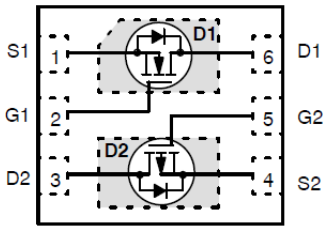
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq), 1 oz. Cu.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

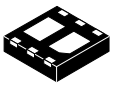
SYMBOLS AND PIN CONNECTIONS





(Top View)

MARKING DIAGRAM



UDFN6
CASE 527AD

AA = Specific Device Code
M = Date Code
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTLUD3C20CZTAG	UDFN6 (Pb−Free)	3000 / Tape & Reel
NTLUD3C20CZTBG		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Ambient – Steady State, Minimum Pad (Note 1)	$R_{\theta JA}$	89.3	°C/W
Junction−to−Ambient – t ≤ 5 s (Note 1)		54.6	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	FET	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	12			V
		P		I_D = −250 μA	−12			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ / T_J	N				TBD		mV/°C
		P				TBD		
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 9.6 V	T_J = 25°C			1	μA
				T_J = 125°C			10	
		P	V_{GS} = 0 V, V_{DS} = −9.6 V	T_J = 25°C			−1	μA
				T_J = 125°C			−10	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	nA
		P					±100	
ON CHARACTERISTICS (Note 2)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 250 μA	0.4		1.0	V
		P		I_D = −250 μA	−0.4		−1.0	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}$ / T_J	N				TBD		mV/°C
		P				TBD		
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V	I_D = 5 A		18	23	mΩ
			V_{GS} = 3.3 V	I_D = 5 A		21	26	
			V_{GS} = 2.5 V	I_D = 4.6 A		25	31	
			V_{GS} = 1.8 V	I_D = 4 A		47	59	
		P	V_{GS} = −4.5 V,	I_D = −4 A		35	44	
			V_{GS} = −3.3 V	I_D = −4 A		44	55	
			V_{GS} = −2.5 V,	I_D = −3 A		60	75	
			V_{GS} = −1.8 V	I_D = −1 A		140	175	
Forward Transconductance	g_{FS}	N	V_{DS} = 5 V	I_D = 5 A		TBD		S
		P	V_{DS} = −5 V	I_D = −4 A		TBD		
CAPACITANCES								
Input Capacitance	C_{ISS}	N	f = 1 MHz, V_{GS} = 0 V V_{DS} = 9.6 V			1074		pF
Output Capacitance	C_{OSS}					147		
Reverse Capacitance	C_{RSS}					139		
Input Capacitance	C_{ISS}	P	f = 1 MHz, V_{GS} = 0 V V_{DS} = −9.6 V			1201		
Output Capacitance	C_{OSS}					150		
Reverse Capacitance	C_{RSS}					145		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Switching characteristics are independent of operating junction temperatures

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	FET	Test Condition		Min	Typ	Max	Unit
CHARGES								
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 9.6 V, I_D = 5 A			10.8		nC
Threshold Gate Charge	$Q_{G(TH)}$					0.8		
Gate−to−Source Charge	Q_{GS}					1.9		
Gate−to−Drain Charge	Q_{GD}					2.4		
Total Gate Charge	$Q_{G(TOT)}$	P	V_{GS} = −4.5 V, V_{DS} = −9.6 V, I_D = −4 A			12.6		
Threshold Gate Charge	$Q_{G(TH)}$					0.9		
Gate−to−Source Charge	Q_{GS}					1.7		
Gate−to−Drain Charge	Q_{GD}					2.8		
SWITCHING CHARACTERISTICS (Note 2)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DS} = 9.6 V, R_G = 1.0 Ω			7.6		ns
Rise Time	t_r					22		
Turn−Off Delay Time	$t_{d(OFF)}$					22		
Fall Time	t_f					4.0		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −9.6 V, R_G = 1.0 Ω			6.8		
Rise Time	t_r					18		
Turn−Off Delay Time	$t_{d(OFF)}$					33		
Fall Time	t_f					9.9		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, I_S = 1.0 mA	T_J = 25°C		0.8	1.1	V
				T_J = 125°C		TBD		
		P	V_{GS} = 0 V, I_S = −1.0 mA	T_J = 25°C		−0.8	−1.1	
				T_J = 125°C		TBD		

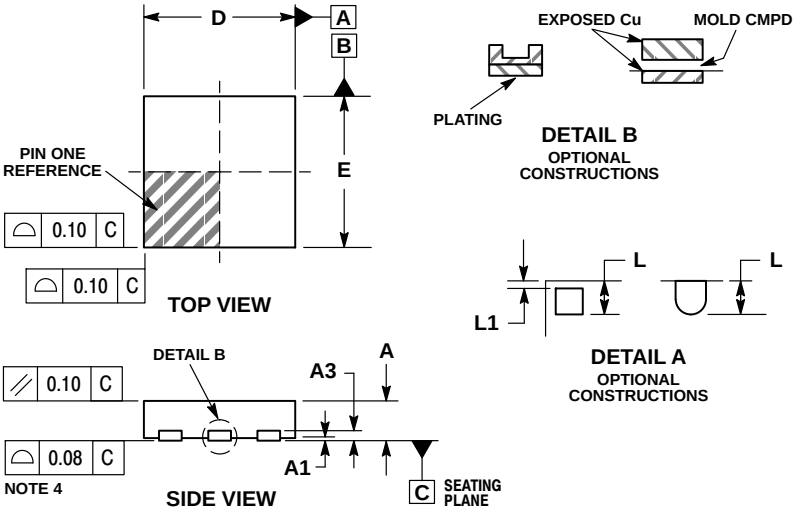
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

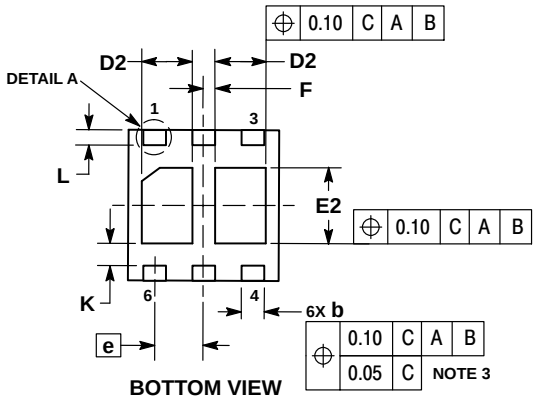
2. Switching characteristics are independent of operating junction temperatures

NTLUD3C20CZ

PACKAGE DIMENSIONS

UDFN6 2x2, 0.65P
CASE 517BF
ISSUE B





NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.15 BSC	
K	0.25 REF	
L	0.20	0.30
L1	---	0.10

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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