

# NTLUS029N06T6

## Power MOSFET 60 V, 7 A, 29 mΩ, Single N-Channel

### Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 1.6 x 1.6 x 0.55 mm for Board Space Saving
- Ultra Low  $R_{DS(on)}$
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Power Load Switch
- Battery Management
- Power Management
- Reverse Polarity Protection

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	60	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	5.4	A
			$T_A = 85^\circ\text{C}$	3.9	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	7		
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	1.5	W
			$t \leq 5$ s	$T_A = 25^\circ\text{C}$	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	3.5	A
		$T_A = 85^\circ\text{C}$	2.6		
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	$P_D$	0.6	W
Pulsed Drain Current		$t_p = 10 \mu\text{s}$	$I_{DM}$	28	A
MOSFET Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode) (Note 1)		$I_S$	2.0	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size, 2 oz. Cu.
3. The device does not have an ESD protection diode.

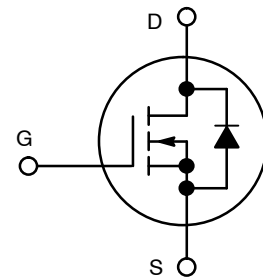


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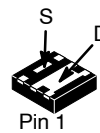
### MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
60 V	29 mΩ @ 10 V	7 A
	42 mΩ @ 4.5 V	



N-CHANNEL MOSFET

### MARKING DIAGRAM



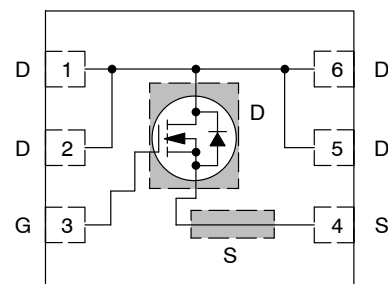
UDFN6  
( $\mu\text{COOL}^{\text{TM}}$ )  
CASE 517AU

1  $\circ$   
AJM▪  
▪

AJ = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# NTLUS029N06T6

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	81.7	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 4)	$R_{\theta JA}$	52.8	
Junction-to-Ambient – Steady State min Pad (Note 5)	$R_{\theta JA}$	193.6	

4. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).  
 5. Surface-mounted on FR4 board using the minimum recommended pad size, 2 oz. Cu.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250$ $\mu\text{A}$ , ref to $25^\circ\text{C}$		25		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = 20$ V			100	nA

### ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 15$ $\mu\text{A}$	1		2	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$			6		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 7$ A		24.5	29	m $\Omega$
		$V_{GS} = 4.5$ V, $I_D = 6$ A		32	42	

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 30$ V		410		pF
Output Capacitance	$C_{OSS}$			190		
Reverse Transfer Capacitance	$C_{RSS}$			3.4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10$ V, $V_{DS} = 30$ V; $I_D = 7$ A		7		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.6		
Gate-to-Source Charge	$Q_{GS}$			1.3		
Gate-to-Drain Charge	$Q_{GD}$			1.0		

### SWITCHING CHARACTERISTICS, $V_{GS} = 4.5$ V (Note 7)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10$ V, $V_{DD} = 30$ V, $I_D = 7$ A, $R_G = 6$ $\Omega$		5.4		ns
Rise Time	$t_r$			2.8		
Turn-Off Delay Time	$t_{d(OFF)}$			14.9		
Fall Time	$t_f$			1.4		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0$ V, $I_S = 2.0$ A	$T_J = 25^\circ\text{C}$		0.79	1.2	V
			$T_J = 125^\circ\text{C}$		0.63		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0$ V, $di/dt = 100$ A/ $\mu\text{s}$ , $I_S = 2.0$ A			20.4		ns
Charge Time	$t_a$				10.4		
Discharge Time	$t_b$				10		
Reverse Recovery Charge	$Q_{RR}$					10.5	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width  $\leq 300$   $\mu\text{s}$ , duty cycle  $\leq 2\%$ .

7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

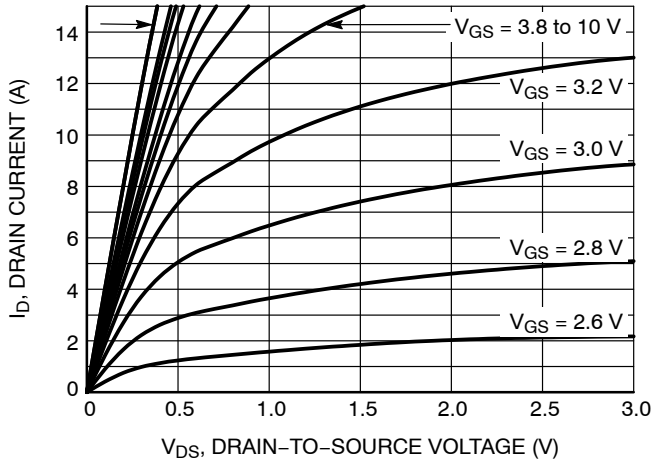


Figure 1. On-Region Characteristics

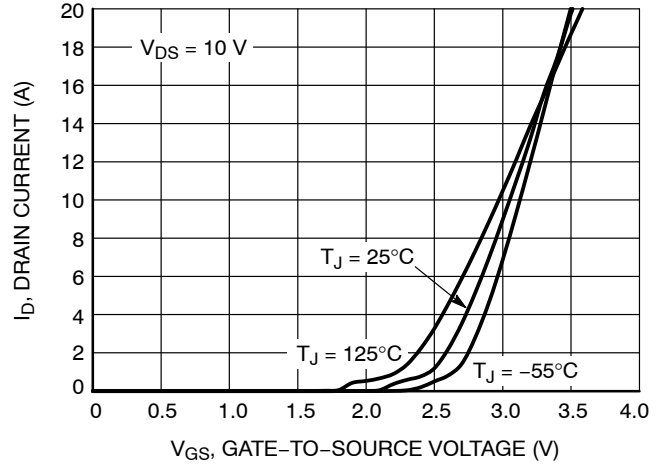


Figure 2. Transfer Characteristics

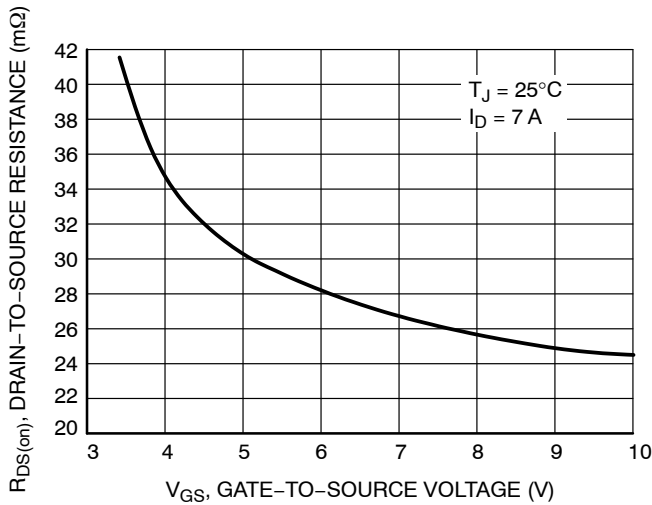


Figure 3. On-Resistance vs. Gate-to-Source Voltage

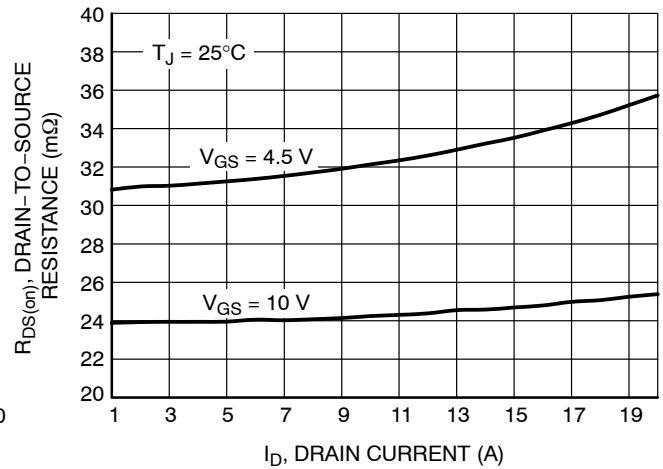


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

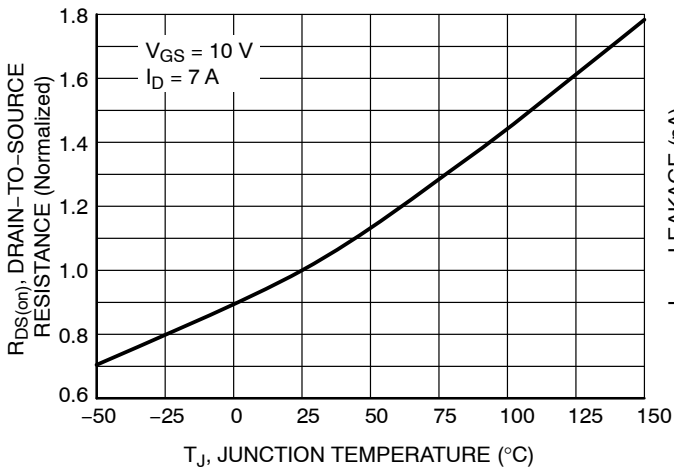


Figure 5. On-Resistance Variation with Temperature

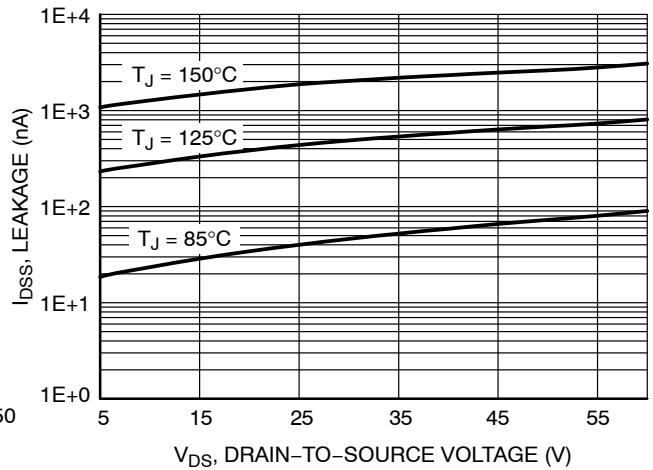


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

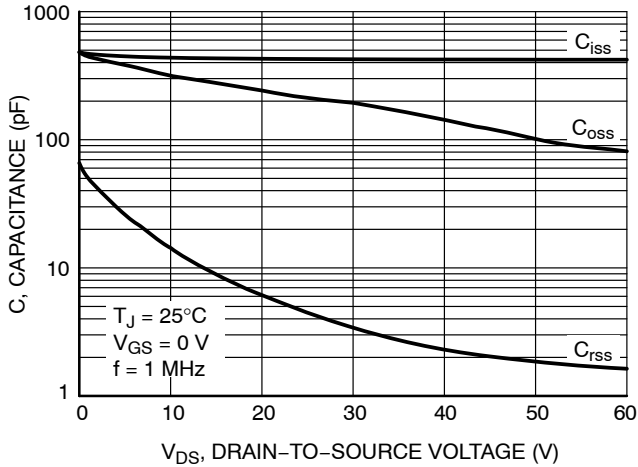


Figure 7. Capacitance Variation

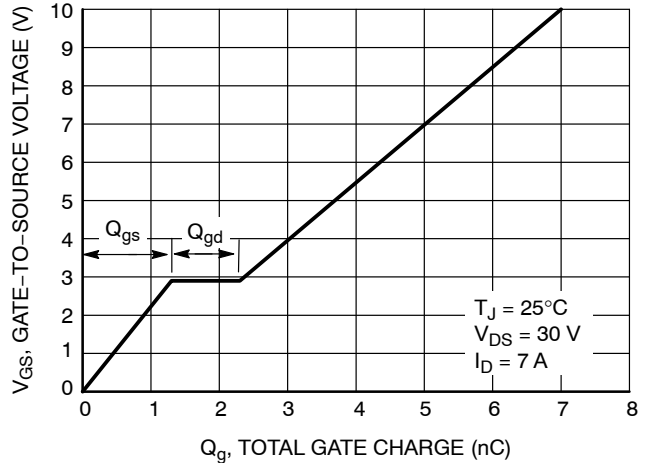


Figure 8. Gate-to-Source Voltage vs. Total Charge

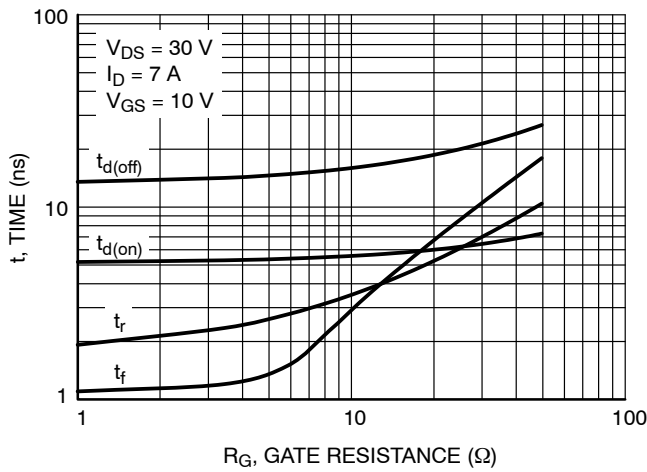


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

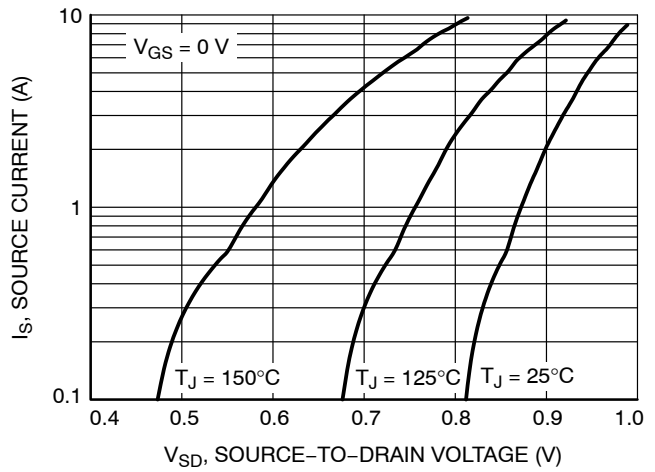


Figure 10. Diode Forward Voltage vs. Current

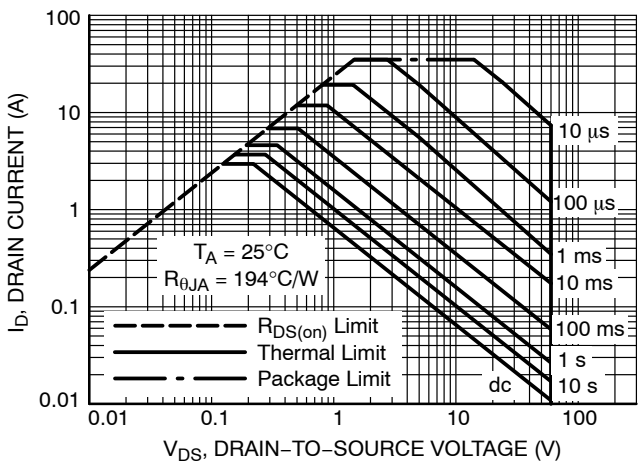


Figure 11. Maximum Rated Forward Biased Safe Operating Area

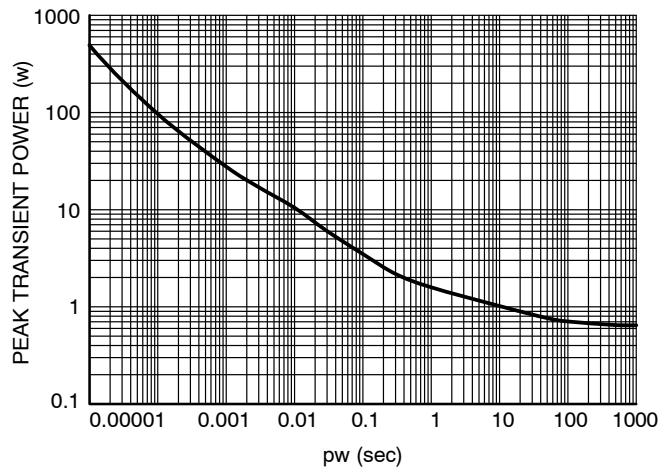
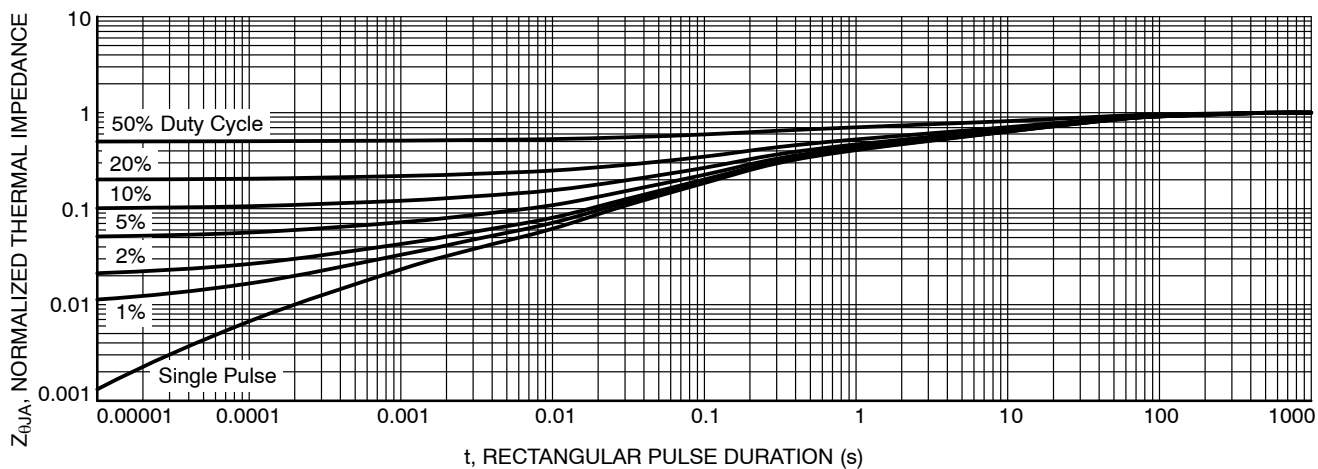


Figure 12. Peak Power

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## TYPICAL CHARACTERISTICS



**Figure 13. Transient Thermal Impedance**

### DEVICE ORDERING INFORMATION

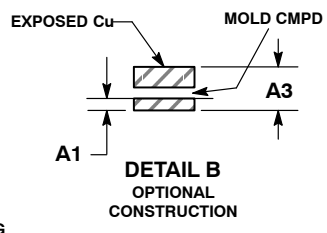
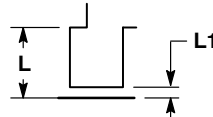
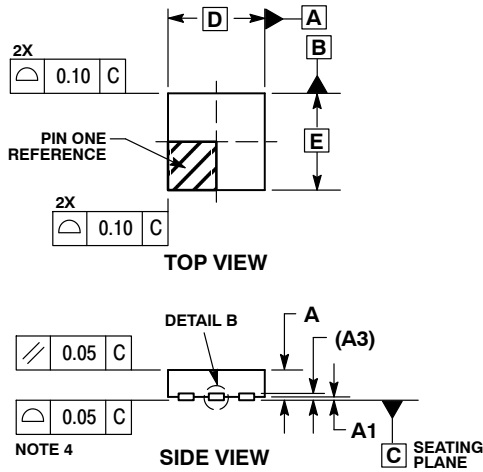
Device	Package	Shipping <sup>†</sup>
NTLUS029N06T6TAG	UDFN6 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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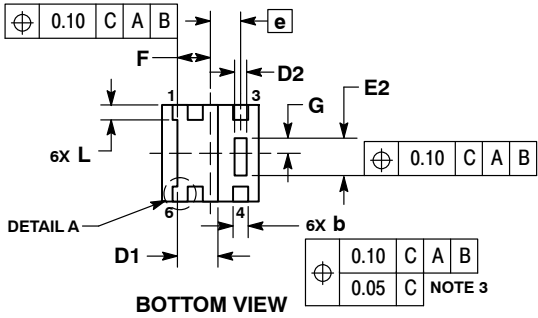
## PACKAGE DIMENSIONS

### UDFN6 1.6x1.6, 0.5P CASE 517AU ISSUE O

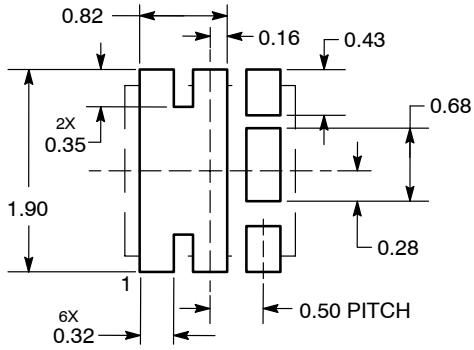


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
D1	0.62	0.72
D2	0.15	0.25
E2	0.57	0.67
F	0.55	BSC
G	0.25	BSC
L	0.20	0.30
L1	---	0.15



### SOLDERMASK DEFINED MOUNTING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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