NTMFD001N03P9

MOSFET – Power, Dual, N-Channel, Trench, Power Clip, Asymmetric

30 V

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

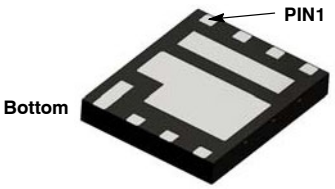
Typical Applications

- DC−DC Converters
- System Voltage Rails

ON Semiconductor®

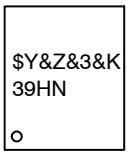
www.onsemi.com

FET	$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
Q1	30 V	5.0 mΩ @ 10 V	53 A
		6.5 mΩ @ 4.5 V	
Q2	30 V	1.0 mΩ @ 10 V	128 A
		1.2 mΩ @ 4.5 V	



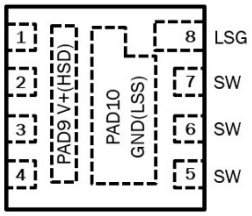
PQFN8
POWER CLIP
CASE 483AR

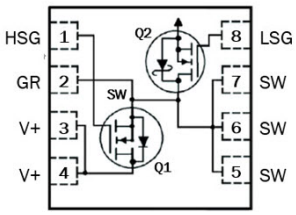
MARKING DIAGRAM



$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
39HN = Specific Device Code

ELECTRICAL CONNECTION





ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

Table 1. MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Q1	Q2	Unit
Drain−to−Source Voltage			V_{DSS}	30	30	V
Gate−to−Source Voltage			V_{GS}	±20	+16 V −12 V	V
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	T_C = 25°C	I_D	53	128	A
		T_C = 85°C		38	92	
Power Dissipation $R_{\theta JC}$ (Note 3)		T_A = 25°C	P_D	22	25	W
Continuous Drain Current $R_{\theta JA}$ (Note 1, 3)	Steady State	T_A = 25°C	I_D	16	38	A
		T_A = 85°C		12	27	
Power Dissipation $R_{\theta JA}$ (Note 1, 3)		T_A = 25°C	P_D	2.1	2.3	W
Continuous Drain Current $R_{\theta JA}$ (Note 2, 3)	Steady State	T_A = 25°C	I_D	11	25	A
		T_A = 85°C		8	18	
Power Dissipation $R_{\theta JA}$ (Note 2, 3)		T_A = 25°C	P_D	0.96	1.04	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	300	500	A
Single Pulse Drain−to−Source Avalanche Energy Q1: I_L = 5.3 A_{pk}, L = 3 mH (Note 4) Q2: I_L = 8.35 A_{pk}, L = 3 mH (Note 4)			E_{AS}	42	104	mJ
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 150		°C
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Q1 Max	Q2 Max	Units
Junction−to−Case − Steady State (Note 1, 3)	$R_{\theta JC}$	5.6	4.9	°C/W
Junction−to−Ambient − Steady State (Note 1, 3)	$R_{\theta JA}$	60	55	
Junction−to−Ambient − Steady State (Note 2, 3)	$R_{\theta JA}$	130	120	

1. Surface−mounted on FR4 board using 1 in^2 pad size, 2 oz Cu pad.
2. Surface−mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro−mechanical application board design. $R_{\Theta CA}$ is determined by the user's board design.
4. Q1 100% UIS tested at L = 0.1 mH, I_{AS} = 20 A.
   Q2 100% UIS tested at L = 0.1 mH, I_{AS} = 47 A.

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		FET	Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		Q1	30			V
		V_{GS} = 0 V, I_D = 1 mA		Q2	30			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ / T_J	I_D = 250 μA, ref to 25°C		Q1		15		mV/°C
		I_D = 50 mA, ref to 25°C		Q2		16		
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C	Q1			1	μA
				Q2			500	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V		Q1			100	nA
		V_{DS} = 0 V, V_{GS} = 16 V		Q2			100	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		Q1	1.0		3.0	V
		V_{GS} = V_{DS}, I_D = 1 mA		Q2	1.0		3.0	
Threshold Temperature Coefficient	$V_{GS(TH)}$ / T_J	I_D = 250 μA, ref to 25°C		Q1		−5		mV/°C
		I_D = 50 mA, ref to 25°C		Q2		−3		
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 17 A		Q1		4.5	5.0	mΩ
		V_{GS} = 4.5 V, I_D = 14 A				5.4	6.5	
		V_{GS} = 10 V, I_D = 40 A		Q2		0.75	1.0	
		V_{GS} = 4.5 V, I_D = 37 A				0.9	1.2	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 14 A		Q1		93		S
		V_{DS} = 5 V, I_D = 37 A		Q2		248		
Gate Resistance	R_G	T_A = 25°C		Q1		1		Ω
				Q2		1		
CHARGES & CAPACITANCES								
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		Q1		1224		pF
				Q2		6575		
Output Capacitance	C_{OSS}			Q1		397		pF
				Q2		2086		
Reverse Capacitance	C_{RSS}			Q1		42		pF
				Q2		138		
Total Gate Charge	$Q_{G(TOT)}$	Q1: V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 14 A Q2: V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 37 A		Q1		7.9		nC
				Q2		43		
Gate−to−Drain Charge	Q_{GD}			Q1		2.0		nC
				Q2		9.5		
Gate−to−Source Charge	Q_{GS}			Q1		3.1		nC
				Q2		15.8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 14 A		Q1		17		nC
		V_{GS} = 10 V, V_{DS} = 15 V, I_D = 37 A		Q2		93		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		FET	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS, VGS = 4.5 V (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V Q1: I_D = 14 A, V_{DD} = 15 V, R_G = 6 Ω Q2: I_D = 37 A, V_{DD} = 15 V, R_G = 6 Ω		Q1		36		ns
				Q2		12.6		
Rise Time	$t_{r(ON)}$			Q1		30.7		ns
				Q2		21.5		
Turn−Off Delay Time	$t_{d(OFF)}$			Q1		64.7		ns
				Q2		17.5		
Fall Time	t_f			Q1		23.5		ns
				Q2		7.3		
SWITCHING CHARACTERISTICS, VGS = 10 V (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V Q1: I_D = 17 A, V_{DD} = 15 V, R_G = 6 Ω Q2: I_D = 40 A, V_{DD} = 15 V, R_G = 6 Ω		Q1		8.0		ns
				Q2		8.6		
Rise Time	$t_{r(ON)}$			Q1		2.0		ns
				Q2		18.2		
Turn−Off Delay Time	$t_{d(OFF)}$			Q1		23.5		ns
				Q2		4.5		
Fall Time	t_f			Q1		2.0		ns
				Q2		4.5		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 14 A	T_J = 25°C	Q1		0.79	1.2	V
			T_J = 125°C			0.66		
		V_{GS} = 0 V, I_S = 37 A	T_J = 25°C	Q2		0.77	1.2	
			T_J = 125°C			0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V Q1: I_S = 14 A, dI/dt = 100 A/μs Q2: I_S = 37 A, dI/dt = 240 A/μs		Q1		23		ns
				Q2		4.6		
Reverse Recovery Charge	Q_{RR}			Q1		8.0		nC
				Q2		68.3		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS – Q1

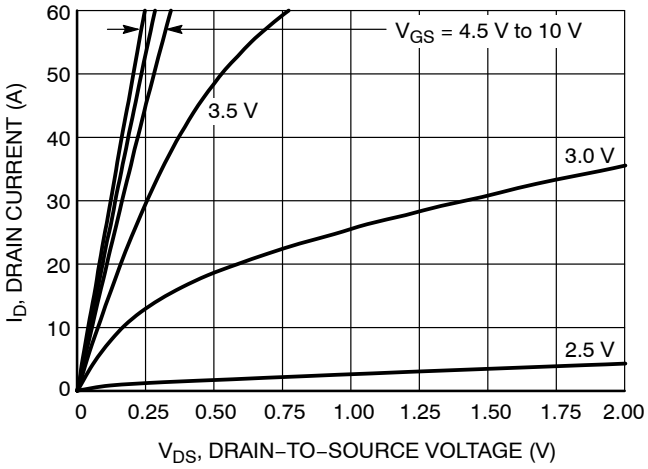


Figure 1. On−Region Characteristics

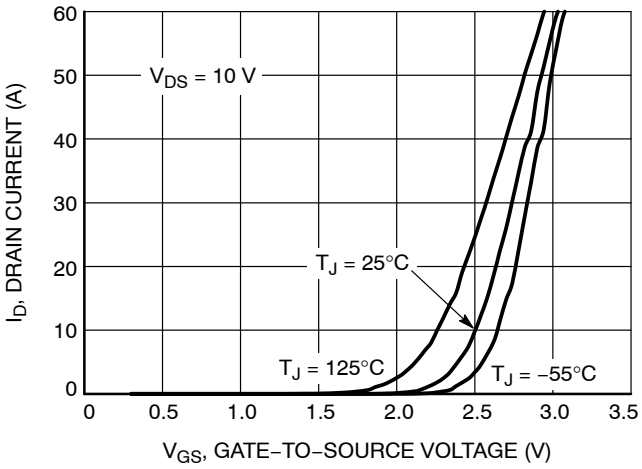


Figure 2. Transfer Characteristics

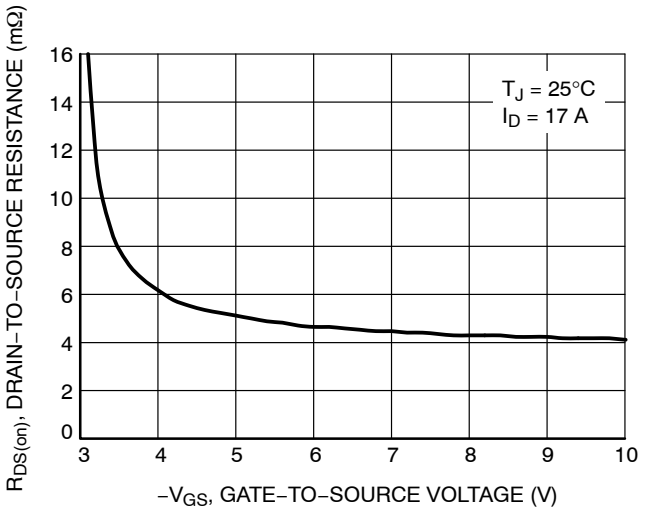


Figure 3. On−Resistance vs. Gate−to−Source Voltage

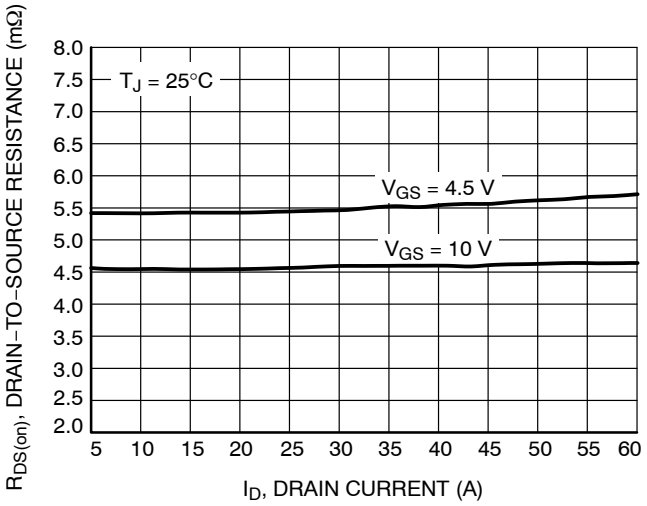


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

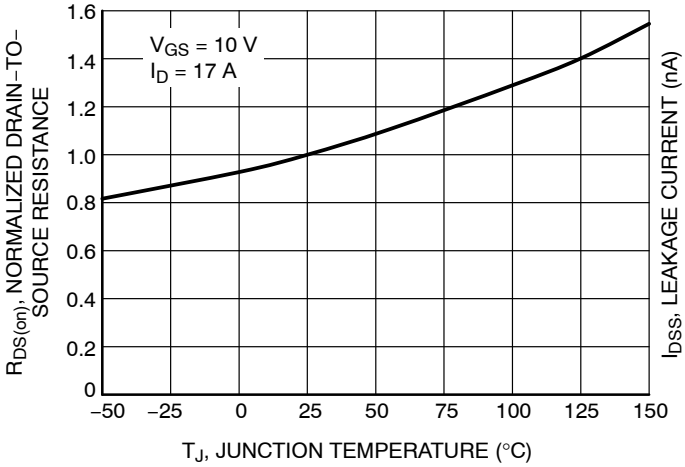


Figure 5. On−Resistance Variation with Temperature

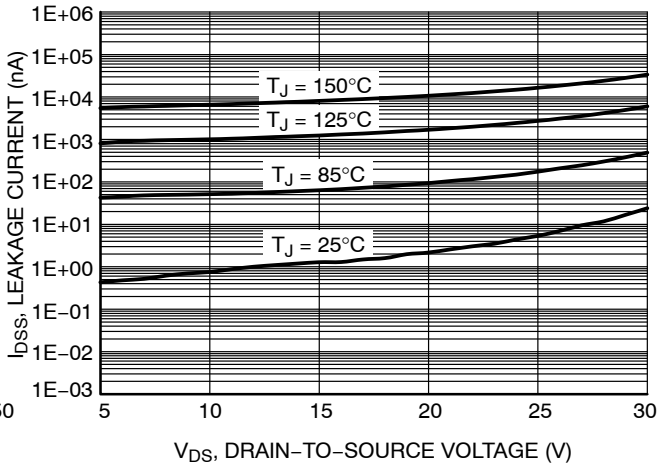


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q1

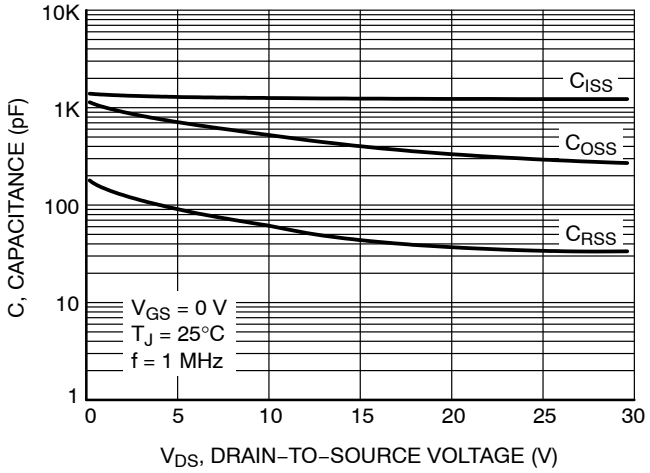


Figure 7. Capacitance Variation

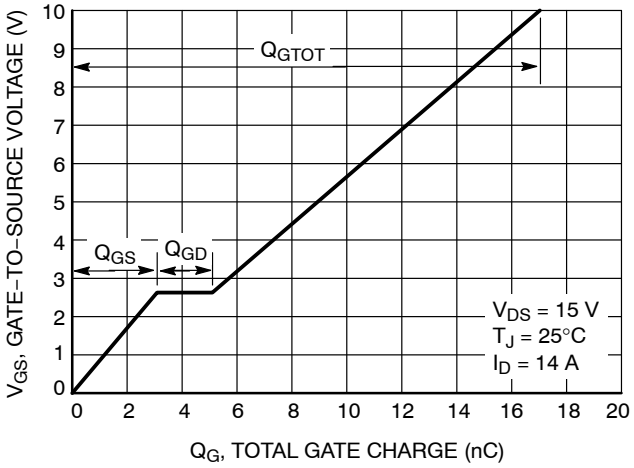


Figure 8. Gate−to−Source Voltage vs. Total Charge

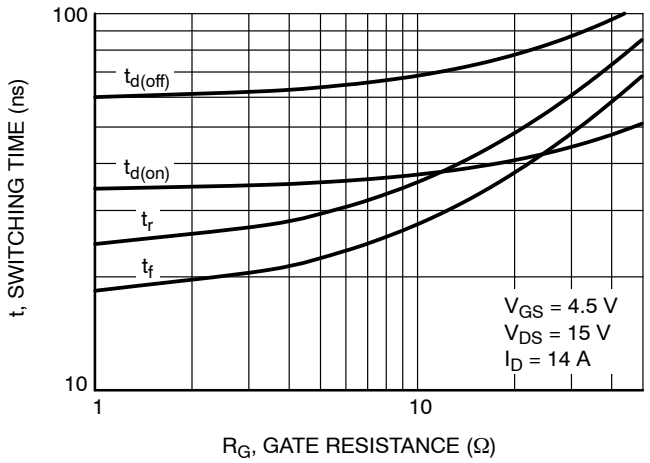


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

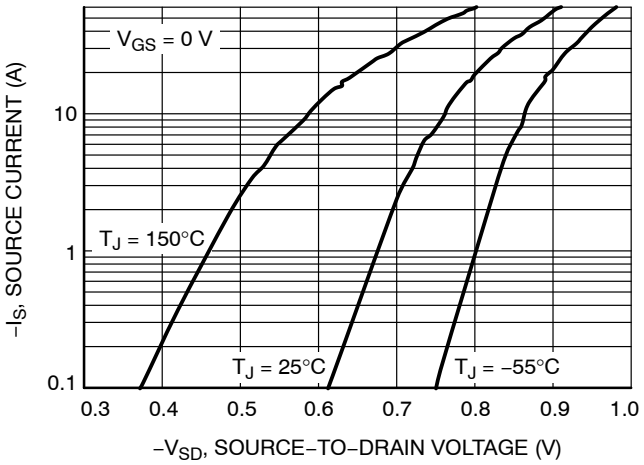


Figure 10. Diode Forward Voltage vs. Current

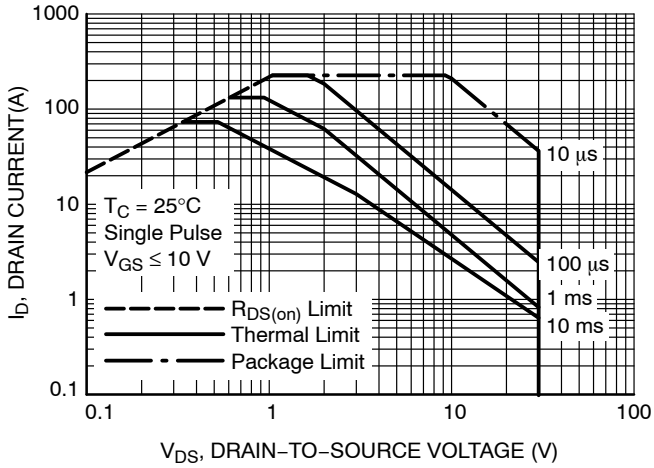


Figure 11. Maximum Rated Forward Biased Safe Operating Area

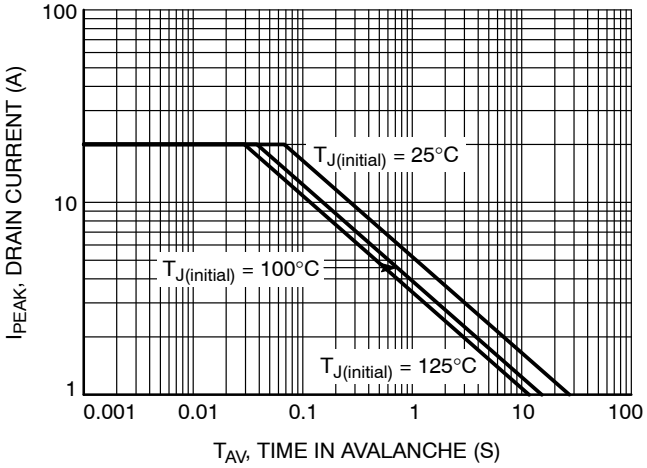


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS – Q1

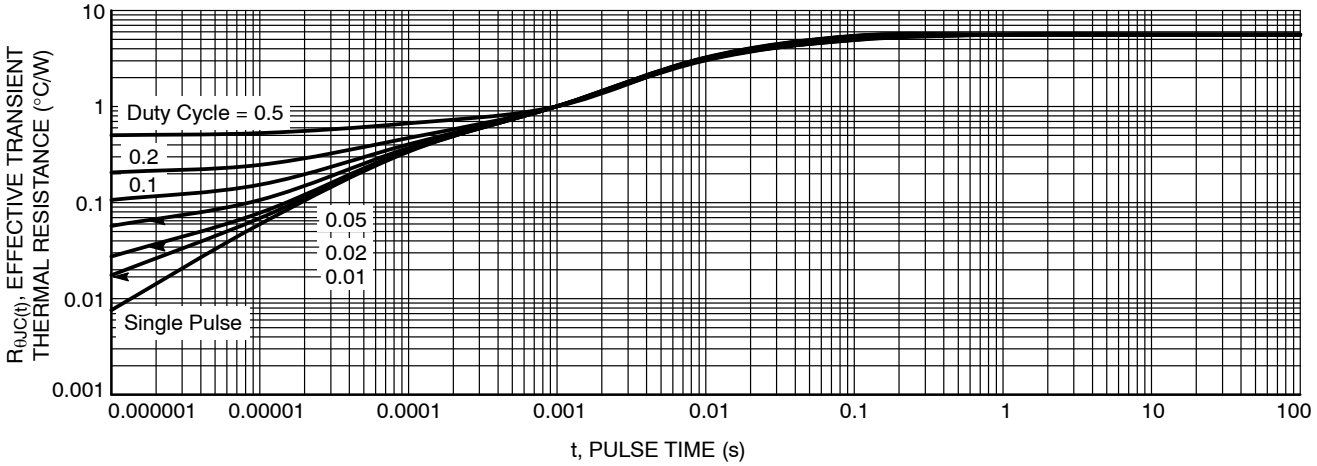


Figure 13. Thermal Response

TYPICAL CHARACTERISTICS – Q2

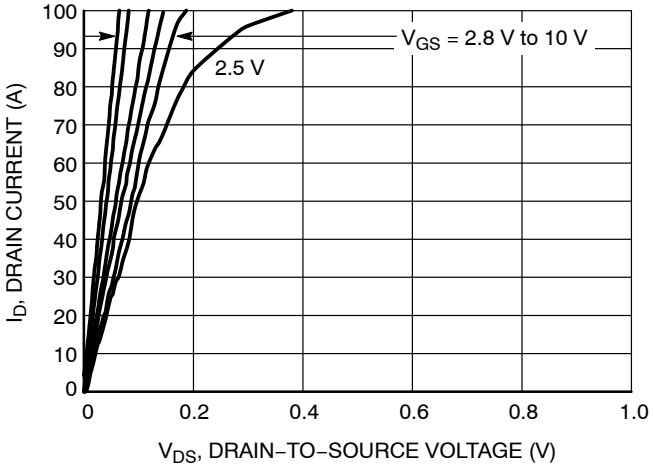


Figure 14. On−Region Characteristics

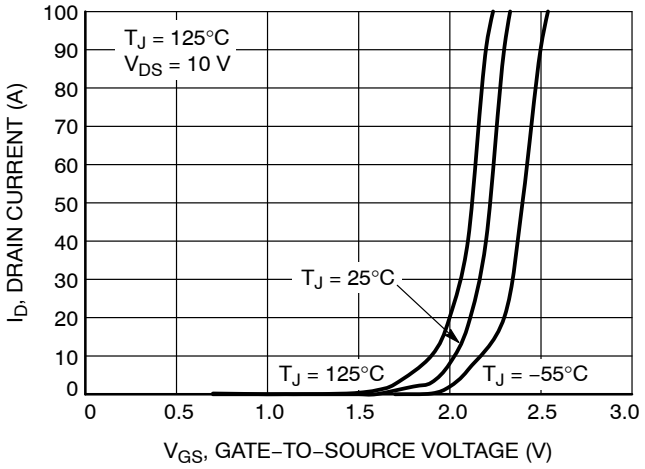


Figure 15. Transfer Characteristics

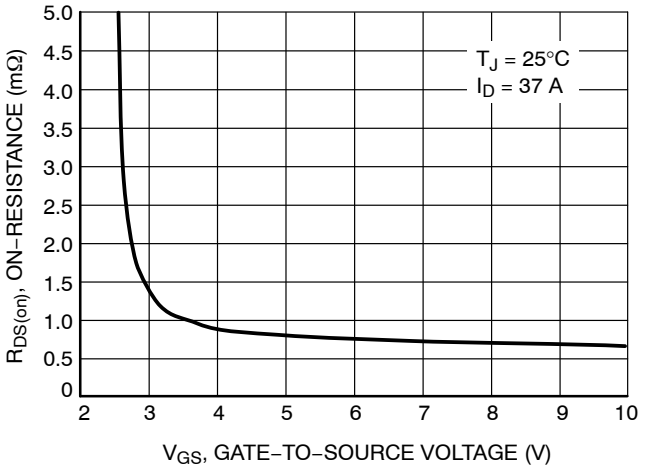


Figure 16. On−Resistance vs. Gate−to−Source Voltage

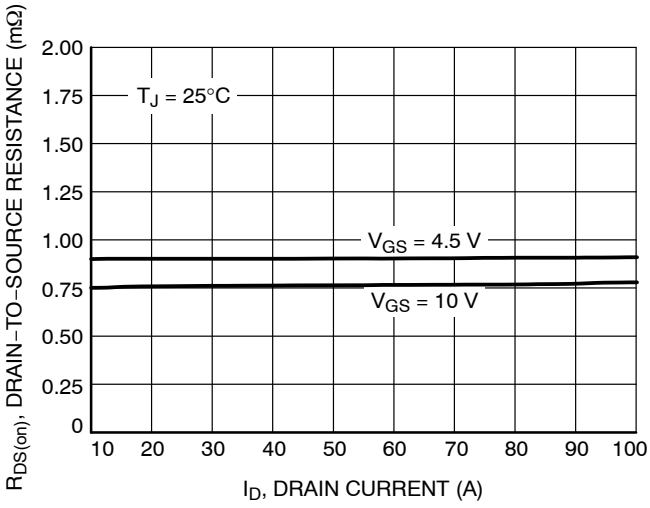


Figure 17. On−Resistance vs. Drain Current and Gate Voltage

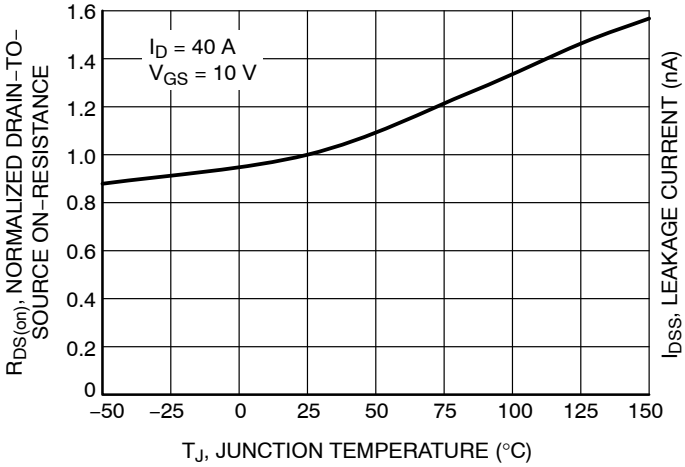


Figure 18. On−Resistance Variation with Temperature

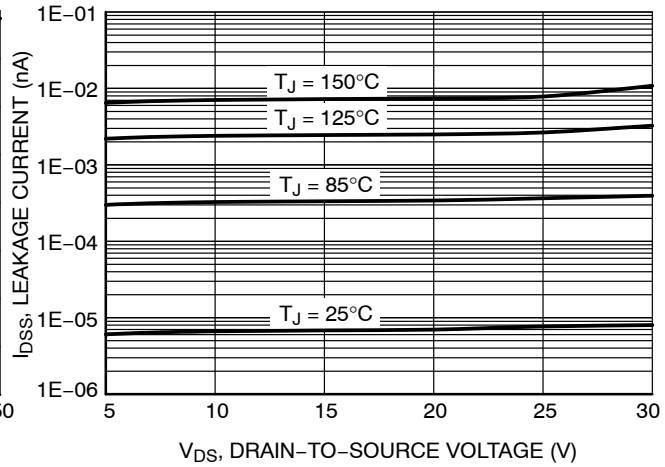


Figure 19. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q2

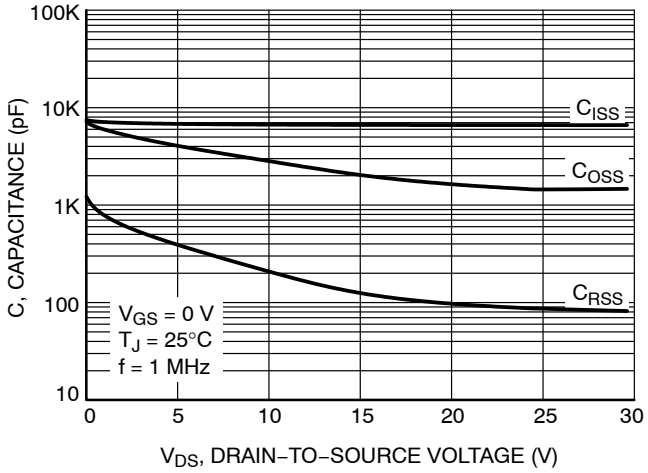


Figure 20. Capacitance Variation

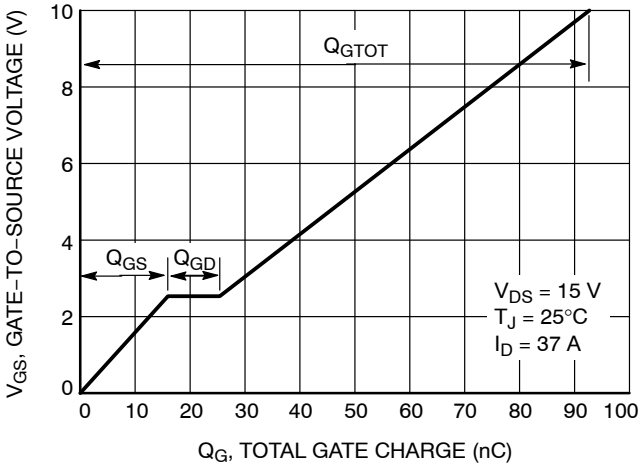


Figure 21. Gate−to−Source Voltage vs. Total Charge

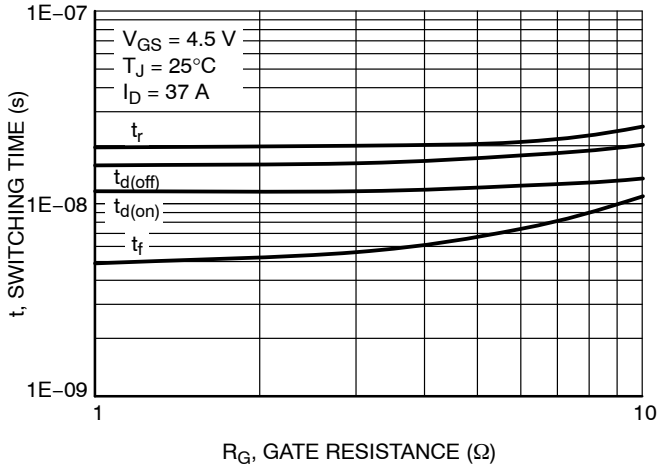


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

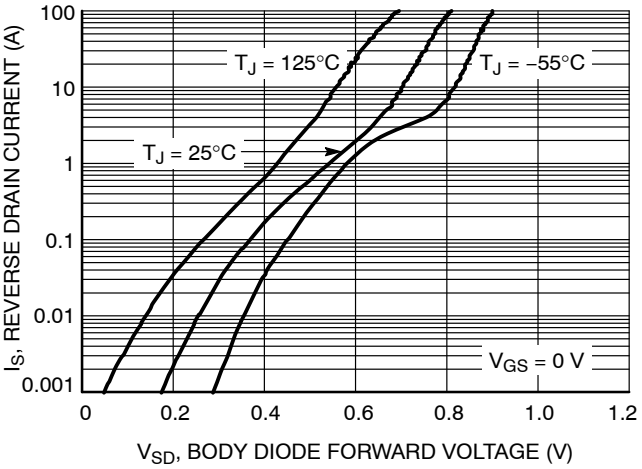


Figure 23. Diode Forward Voltage vs. Current

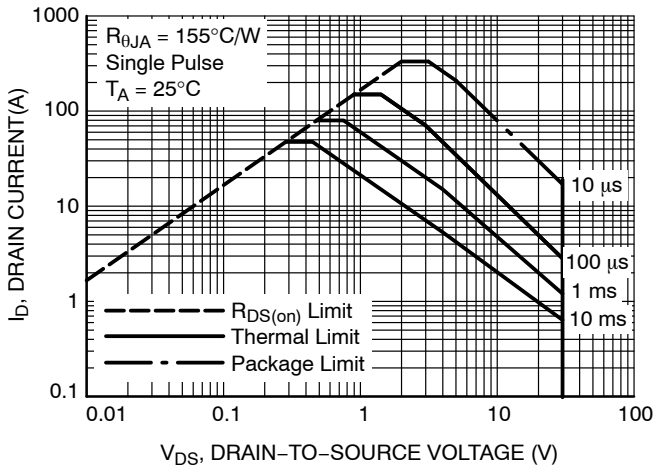


Figure 24. Maximum Rated Forward Biased Safe Operating Area

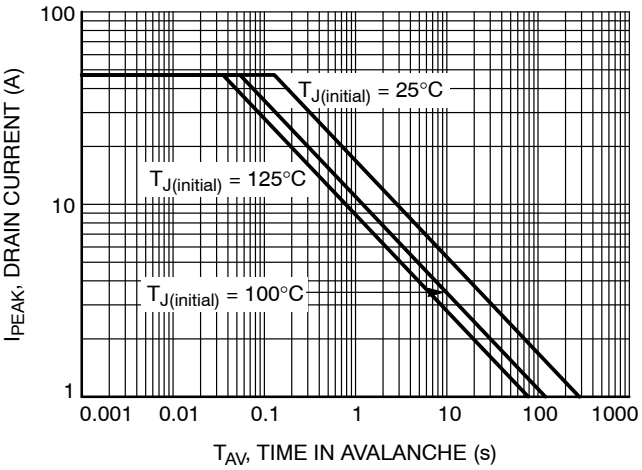


Figure 25. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS – Q2

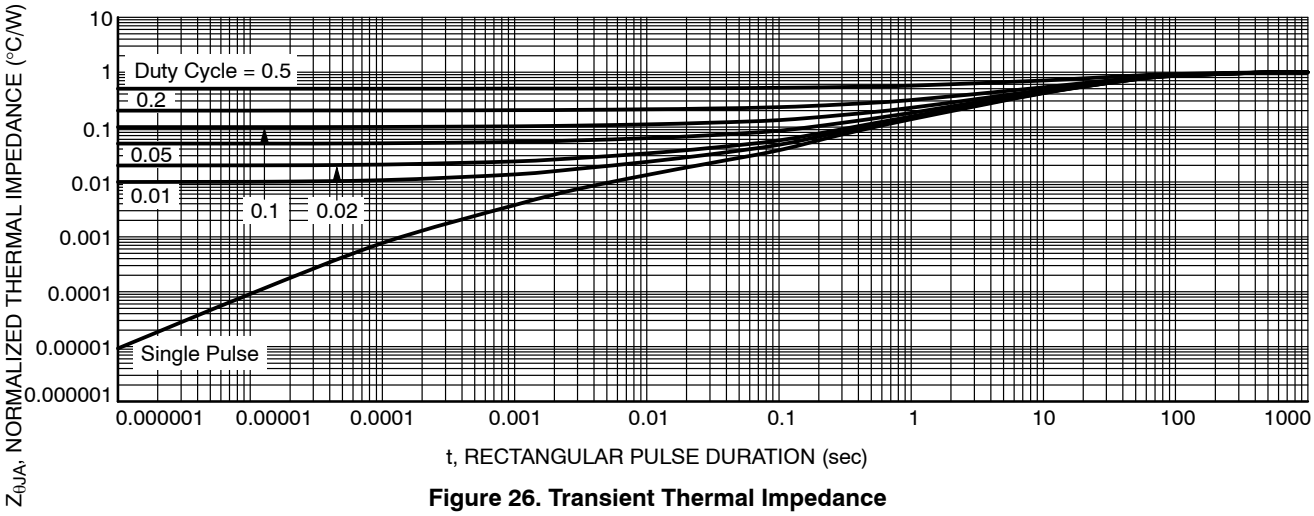


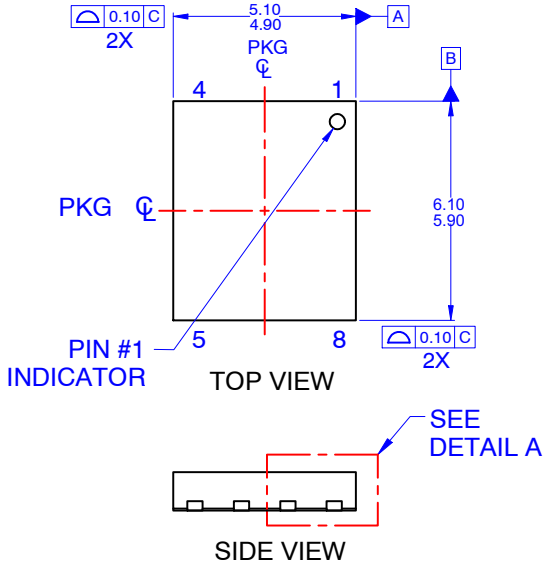
Figure 26. Transient Thermal Impedance

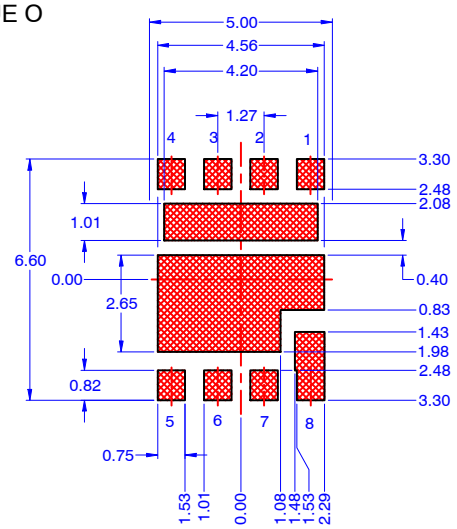
ORDERING INFORMATION

Device	Package	Shipping
NTMFD001N03P9	DFN8 (Pb−Free)	3000 / Tape & Reel

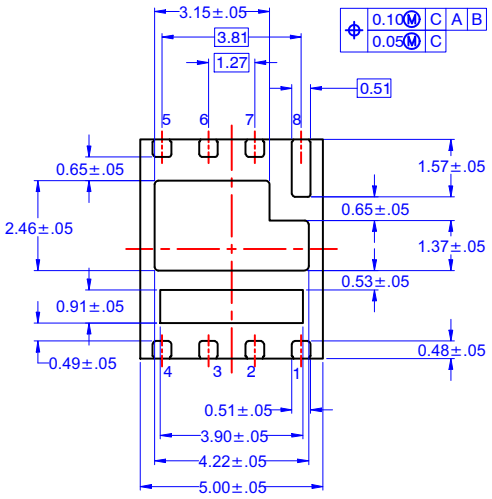
PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P
CASE 483AR
ISSUE O





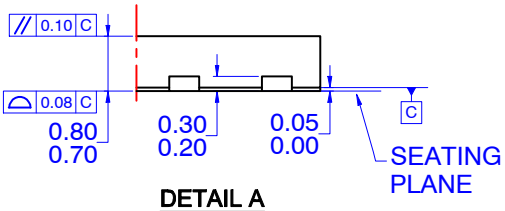
RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO−229, DATED 11/2001.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.



DETAIL A
(SCALE: 2X)

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