

NTMFD1D6N03P8

MOSFET - PowerTrench® Power Clip, 30 V, Asymmetric, Dual N-Channel

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 5.0 m Ω at V_{GS} = 10 V, I_D = 17 A
- Max $r_{DS(on)}$ = 6.5 m Ω at V_{GS} = 4.5 V, I_D = 14 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 1.6 m Ω at V_{GS} = 10 V, I_D = 32 A
- Max $r_{DS(on)}$ = 2.0 m Ω at V_{GS} = 4.5 V, I_D = 28 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

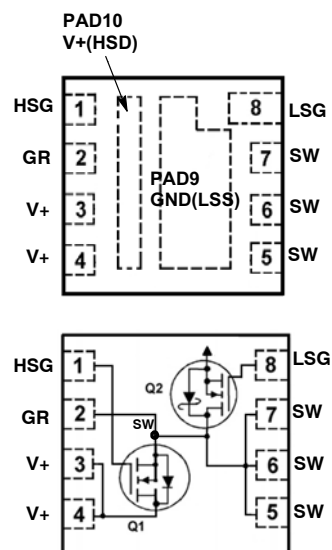
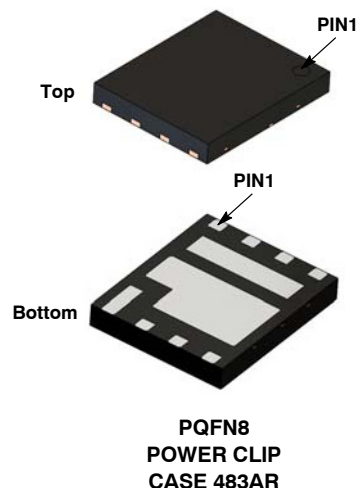
- Computing
- Communications
- General Purpose Point of Load

| Pin | Name | Description |
|----------|----------|--------------------------------|
| 1 | HSG | High Side Gate |
| 2 | GR | Gate Return |
| 3, 4, 10 | V+(HSD) | High Side Drain |
| 5, 6, 7 | SW | Switching Node, Low Side Drain |
| 8 | LSG | Low Side Gate |
| 9 | GND(LSS) | Low Side Source |



ON Semiconductor®

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ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

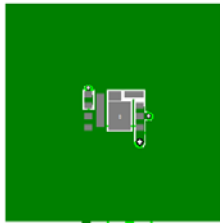
NTMFD1D6N03P8

Table 1. MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted.

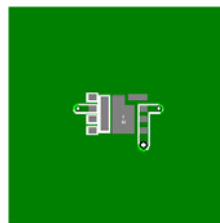
| Symbol | Parameter | Q1 | Q2 | Units | |
|----------------|--|------------------------------------|--------------|------------------|---|
| V_{DS} | Drain to Source Voltage | 30 | 30 | V | |
| B_{VDDST} | B_{VDDST} (transient) < 100 ns | 32.5 | 32.5 | V | |
| V_{GS} | Gate to Source Voltage | ± 20 | ± 12 | V | |
| I_D | Drain Current – Continuous | $T_C = 25^\circ\text{C}$ (Note 1) | 56 | 109 | A |
| | – Continuous | $T_C = 100^\circ\text{C}$ (Note 1) | 35 | 69 | |
| | – Continuous | $T_A = 25^\circ\text{C}$ | 17 (Note 4) | 32 (Note 5) | |
| | – Pulsed | $T_A = 25^\circ\text{C}$ (Note 2) | 227 | 704 | |
| E_{AS} | Single Pulse Avalanche Energy (Note 3) | 54 | 181 | mJ | |
| P_D | Power Dissipation for Single Operation | $T_C = 25^\circ\text{C}$ | 23 | 29 | W |
| | Power Dissipation for Single Operation | $T_A = 25^\circ\text{C}$ | 2.1 (Note 4) | 2.3 (Note 5) | |
| | Power Dissipation for Single Operation | $T_A = 25^\circ\text{C}$ | 1.0 (Note 6) | 1.1 (Note 7) | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | –55 to +150 | | $^\circ\text{C}$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

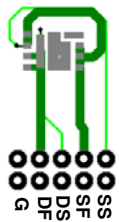
1. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.
2. Pulsed I_D refer to Figure 11 and Figure 24 SOA curve for more details.
3. Q1 :EAS of 54 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 3$ mH, $I_{AS} = 6$ A, $V_{DD} = 30$ V, $V_{GS} = 10$ V. 100% tested at $L = 0.1$ mH, $I_{AS} = 20$ A.
Q2: EAS of 181 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 3$ mH, $I_{AS} = 11$ A, $V_{DD} = 30$ V, $V_{GS} = 10$ V. 100% tested at $L = 0.1$ mH, $I_{AS} = 36$ A.



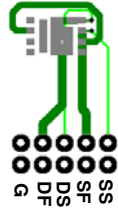
4. $60^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



5. $55^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



6. $130^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



7. $120^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper

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Table 2. PACKAGE MARKING AND ORDERING INFORMATION

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|---------------|---------------|-----------|------------|------------|
| D1D6 | NTMFD1D6N03P8 | Power Clip 56 | 13" | 12 mm | 3000 units |

Table 3. THERMAL CHARACTERISTICS

| Parameter | Description | Q1 | Q2 | Units |
|-----------------|---|--------------|--------------|-------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 5.6 | 4.3 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 60 (Note 8) | 55 (Note 8) | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 130 (Note 8) | 120 (Note 8) | |

8. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material, $R_{\theta CA}$ is determined by the user's board design.

Table 4. ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|--------|-----------|-----------------|------|-----|-----|-----|-------|
|--------|-----------|-----------------|------|-----|-----|-----|-------|

OFF CHARACTERISTICS

| | | | | | | | |
|--------------------------------|---|--|----------|----------|----------|------------|--------------------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$ $I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$ | Q1 Q2 | 30 30 | | | V |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$, referenced to 25°C $I_D = 10 \text{ mA}$, referenced to 25°C | Q1 Q2 | | 15 19 | | mV/°C |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ | Q1 Q2 | | | 1 500 | μA μA |
| I_{GSS} | Gate to Source Leakage Current, Forward | $V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$ $V_{GS} = 12 \text{ V}, V_{DS} = 0 \text{ V}$ | Q1 Q2 | | | 100 100 | nA nA |

ON CHARACTERISTICS

| | | | | | | | |
|----------------------------------|--|---|----------|------------|-------------------|-------------------|------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ $V_{GS} = V_{DS}, I_D = 1 \text{ mA}$ | Q1 Q2 | 1.0 1.0 | 1.7 1.6 | 3.0 3.0 | V |
| $\Delta V_{GS(th)} / \Delta T_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$, referenced to 25°C $I_D = 10 \text{ mA}$, referenced to 25°C | Q1 Q2 | | -5 -3 | | mV/°C |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS} = 10 \text{ V}, I_D = 17 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 14 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 17 \text{ A}, T_J = 125^\circ\text{C}$ | Q1 | | 4.1 5.4 5.7 | 5.0 6.5 7.0 | m Ω |
| | | $V_{GS} = 10 \text{ V}, I_D = 32 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 28 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 32 \text{ A}, T_J = 125^\circ\text{C}$ | Q2 | | 1.4 1.7 2.1 | 1.6 2.0 2.4 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 5 \text{ V}, I_D = 17 \text{ A}$ $V_{DS} = 5 \text{ V}, I_D = 32 \text{ A}$ | Q1 Q2 | | 93 188 | | S |

DYNAMIC CHARACTERISTICS

| | | | | | | | |
|------------|------------------------------|--|----------|------------|--------------|--------------|----|
| C_{iss} | Input Capacitance | Q1: $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ Q2: $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ | Q1 Q2 | | 1224 4593 | 1715 6430 | pF |
| C_{oss} | Output Capacitance | | Q1 Q2 | | 397 1210 | 560 1695 | |
| C_{riss} | Reverse Transfer Capacitance | | Q1 Q2 | | 42 80 | 60 115 | pF |
| R_g | Gate Resistance | | Q1 Q2 | 0.1 0.1 | 0.5 0.8 | 1.5 2.4 | |

SWITCHING CHARACTERISTICS

| | | | | | | | |
|--------------|---------------------|--|----------|--|----------|----------|----|
| $t_{d(on)}$ | Turn-On Delay Time | Q1: $V_{DD} = 15 \text{ V}, I_D = 17 \text{ A}, R_{GEN} = 6 \Omega$ Q2: $V_{DD} = 15 \text{ V}, I_D = 32 \text{ A}, R_{GEN} = 6 \Omega$ | Q1 Q2 | | 8 14 | 16 25 | ns |
| t_r | Rise Time | | Q1 Q2 | | 2 5 | 10 10 | |
| $t_{d(off)}$ | Turn-Off Delay Time | | Q1 Q2 | | 18 38 | 33 61 | ns |
| t_f | Fall Time | | Q1 Q2 | | 2 4 | 10 10 | |

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Table 4. ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units | |
|----------------------------------|-------------------------------|---------------------------------------|--|-----|-----|-----|-------|----|
| SWITCHING CHARACTERISTICS | | | | | | | | |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{ V to }10\text{ V}$ | Q1 $V_{DD} = 15\text{ V},$ $I_D = 17\text{ A}$ Q2 $V_{DD} = 15\text{ V},$ $I_D = 32\text{ A}$ | Q1 | | 17 | 24 | nC |
| | | | | Q2 | | 62 | 87 | |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{ V to }4.5\text{ V}$ | | Q1 | | 8 | 11 | nC |
| | | | | Q2 | | 28 | 40 | |
| Q_{gs} | Gate to Source Gate Charge | | Q1 | | 3.1 | | nC | |
| | | | Q2 | | 11 | | | |
| Q_{gd} | Gate to Drain "Miller" Charge | | Q1 | | 2.0 | | nC | |
| | | | Q2 | | 5.3 | | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|----------|---------------------------------------|--|----|--|-----|-----|----|
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 17\text{ A}$ (Note 9) $V_{GS} = 0\text{ V}, I_S = 32\text{ A}$ (Note 9) | Q1 | | 0.8 | 1.2 | V |
| | | | Q2 | | 0.8 | 1.2 | |
| t_{rr} | Reverse Recovery Time | Q1 $I_F = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | Q1 | | 23 | 37 | ns |
| | | | Q2 | | 32 | 51 | |
| Q_{rr} | Reverse Recovery Charge | Q2 $I_F = 32\text{ A}, di/dt = 240\text{ A}/\mu\text{s}$ | Q1 | | 8 | 16 | nC |
| | | | Q2 | | 40 | 64 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

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Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

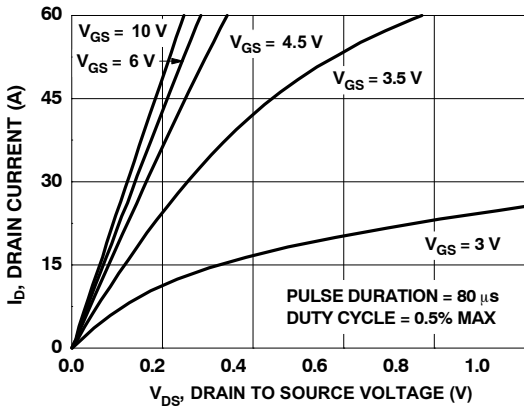


Figure 1. On Region Characteristics

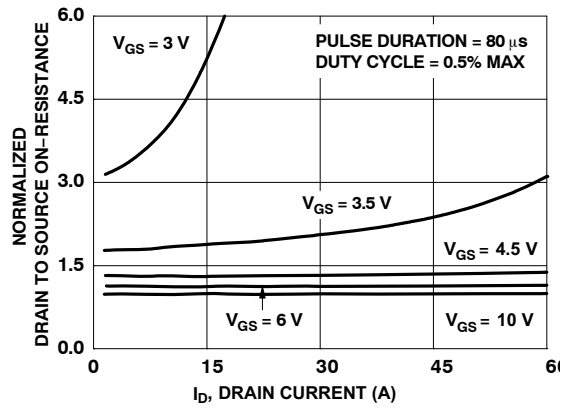


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

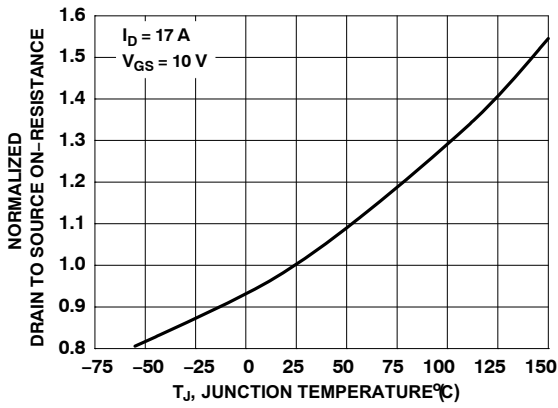


Figure 3. Normalized On-Resistance vs. Junction Temperature

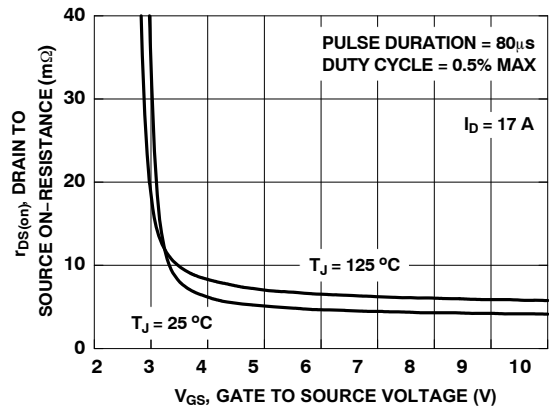


Figure 4. On-Resistance vs. Gate to Source Voltage

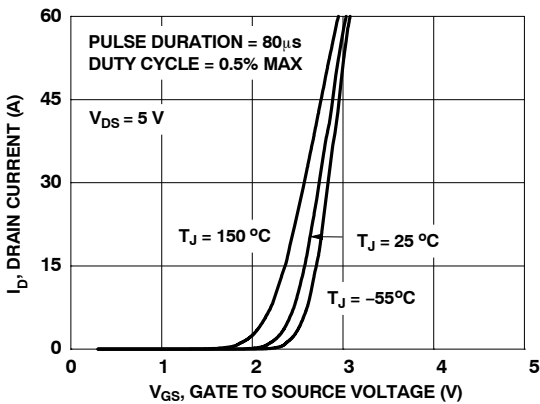


Figure 5. Transfer Characteristics

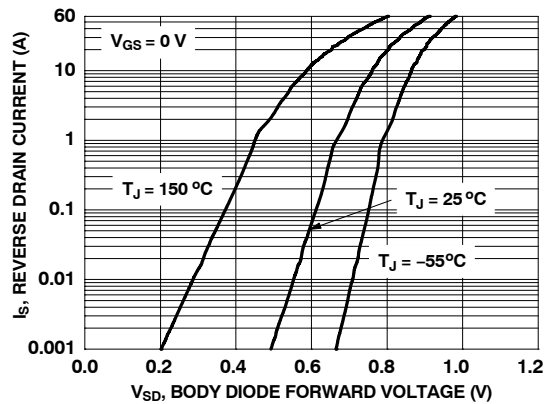


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

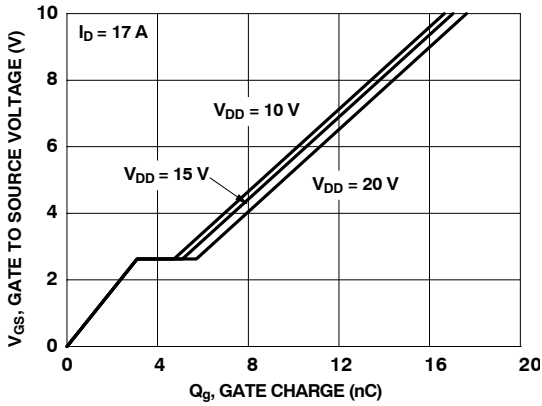


Figure 7. Gate Charge Characteristics

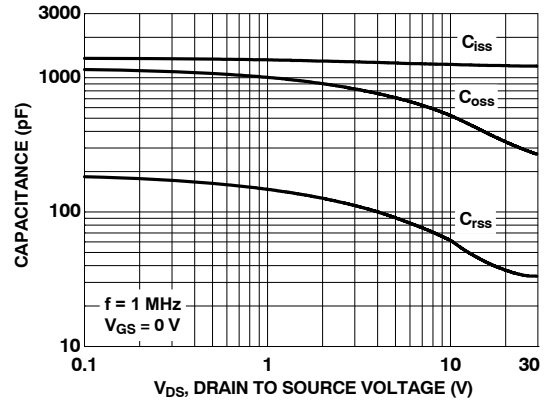


Figure 8. Capacitance vs. Drain to Source Voltage

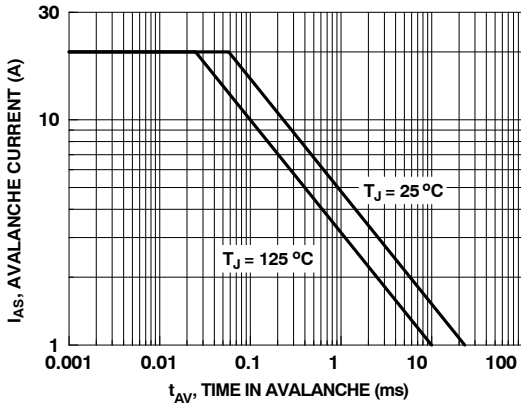


Figure 9. Unclamped Inductive Switching Capability

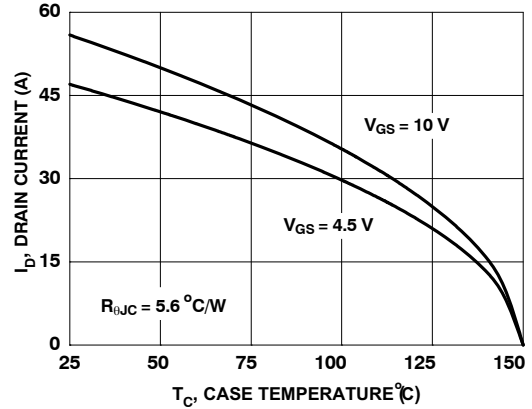


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

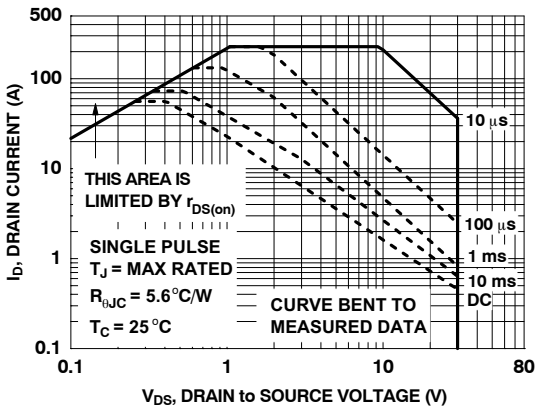


Figure 11. Forward Bias Safe Operating Area

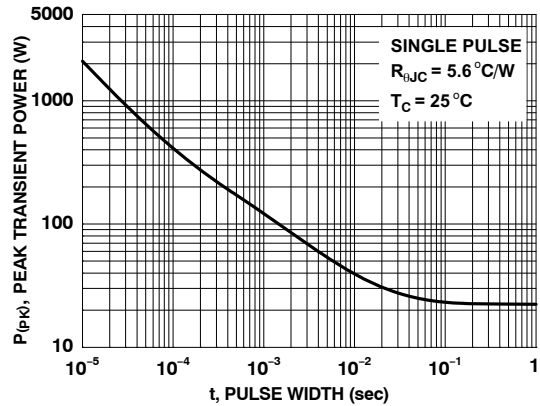


Figure 12. Single Pulse Maximum Power Dissipation

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Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

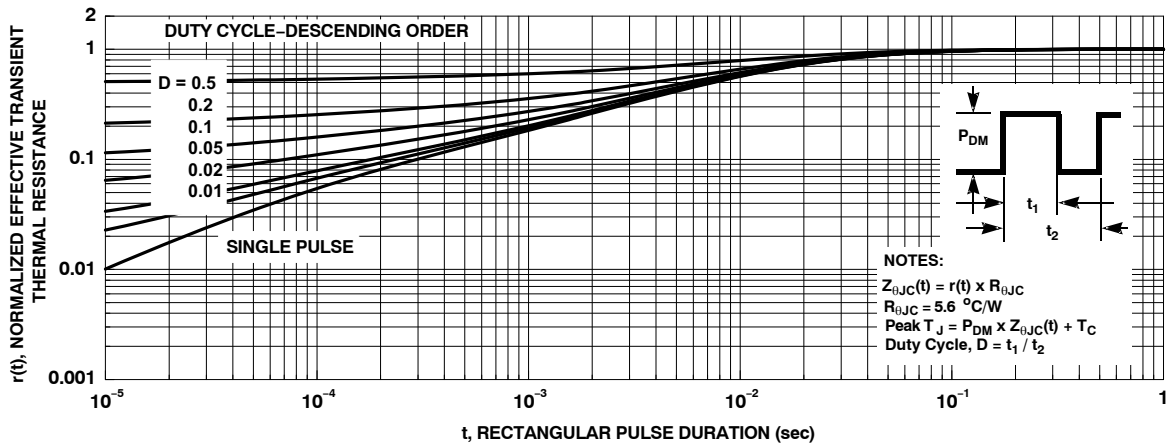


Figure 13. Junction-to-Case Transient Thermal Response Curve

NTMFD1D6N03P8

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

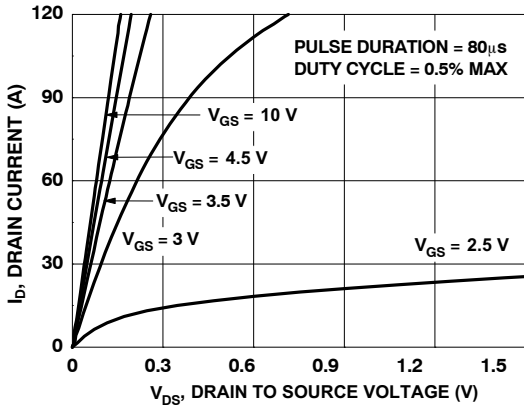


Figure 14. On Region Characteristics

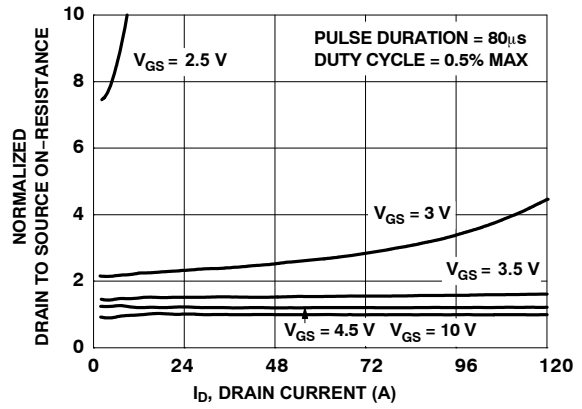


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

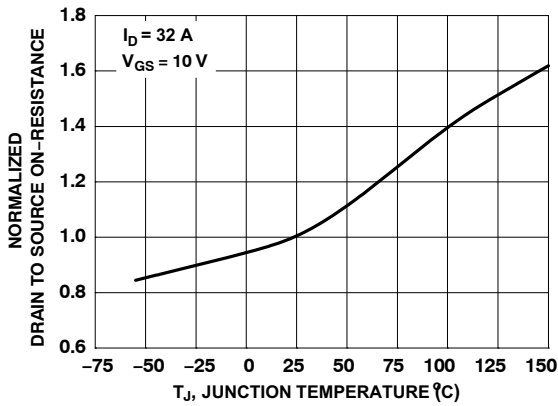


Figure 16. Normalized On-Resistance vs. Junction Temperature

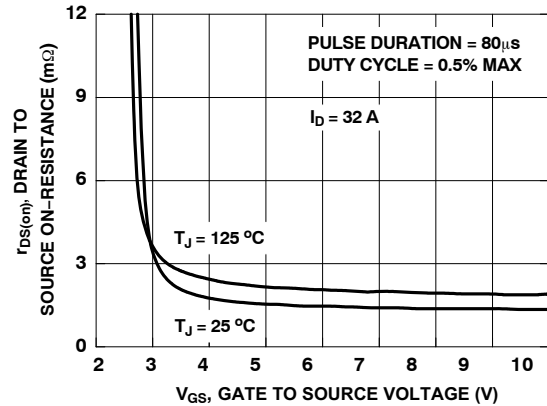


Figure 17. On-Resistance vs. Gate to Source Voltage

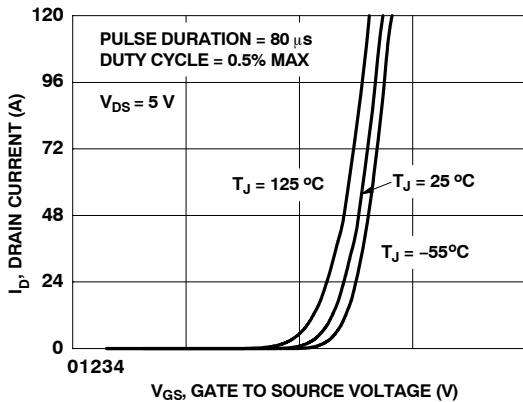


Figure 18. Transfer Characteristics

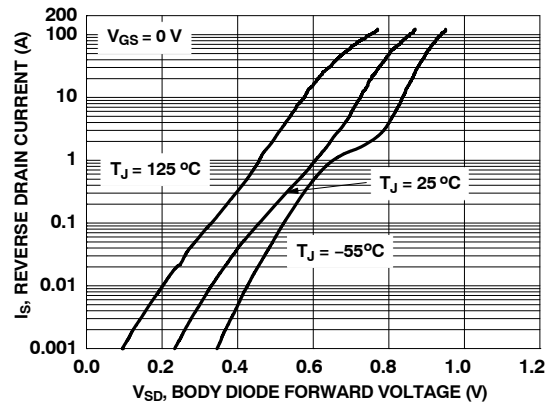


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

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Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

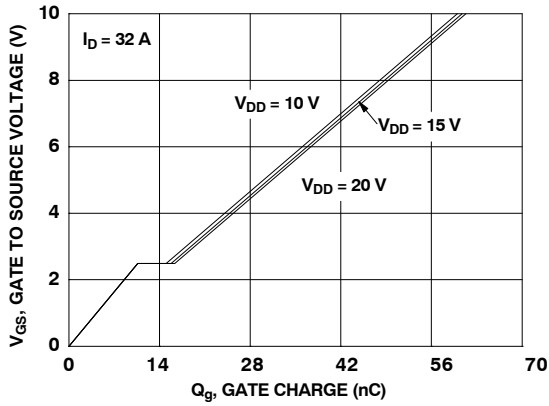


Figure 20. Gate Charge Characteristics

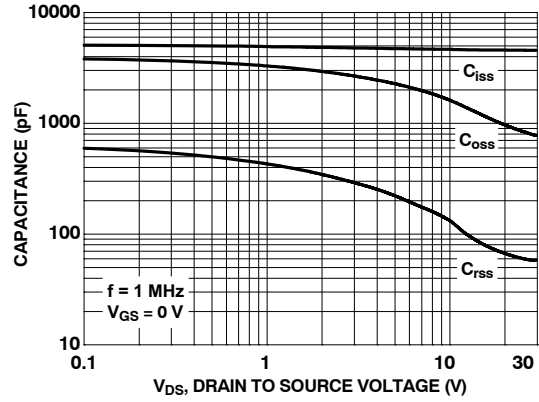


Figure 21. Capacitance vs. Drain to Source Voltage

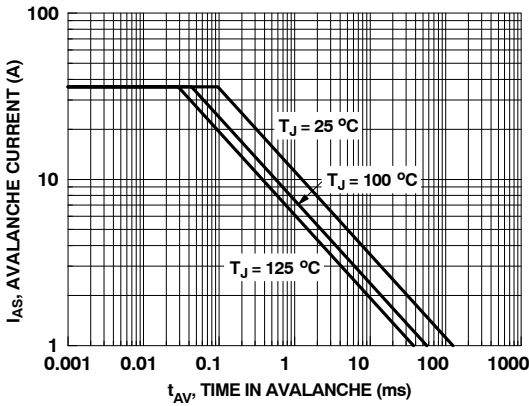


Figure 22. Unclamped Inductive Switching Capability

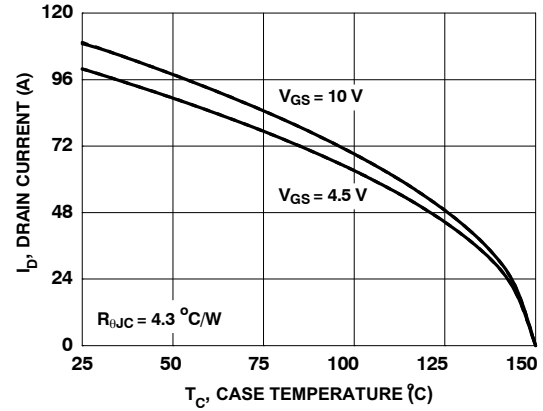


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

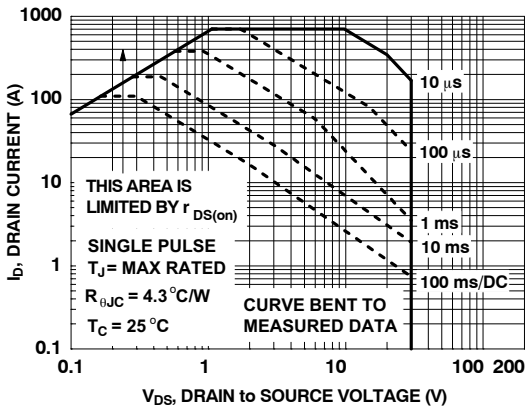


Figure 24. Forward Bias Safe Operating Area

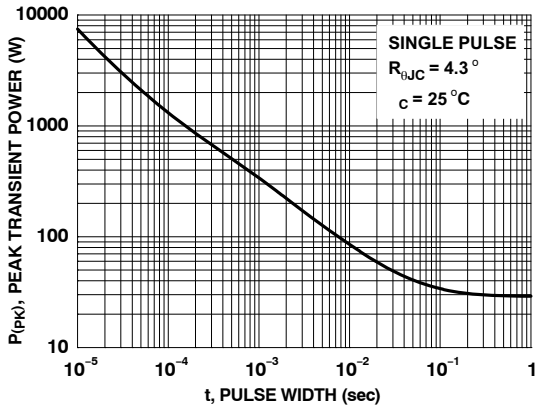


Figure 25. Single Pulse Maximum Power Dissipation

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Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

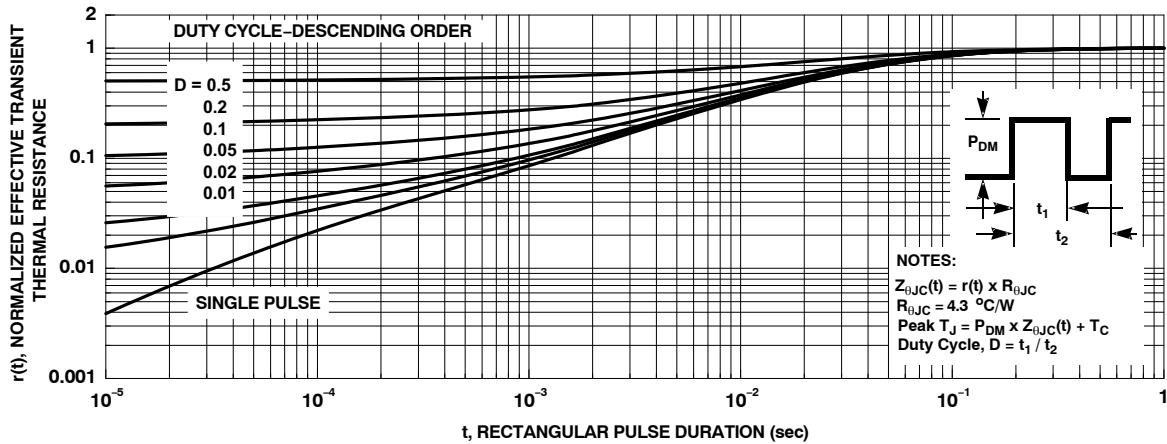


Figure 26. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics

SyncFET Schottky Body Diode Characteristics

ON Semiconductor's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC5018SG.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

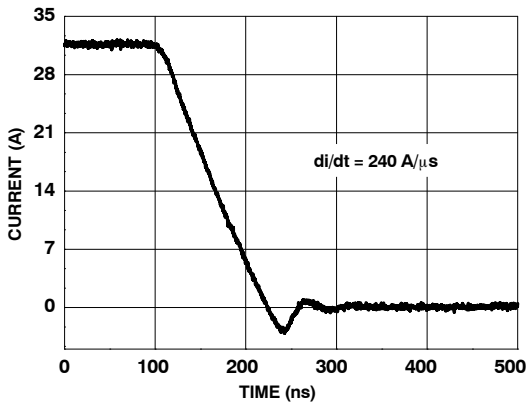


Figure 27. SyncFET Body Diode Reverse Recovery Characteristic

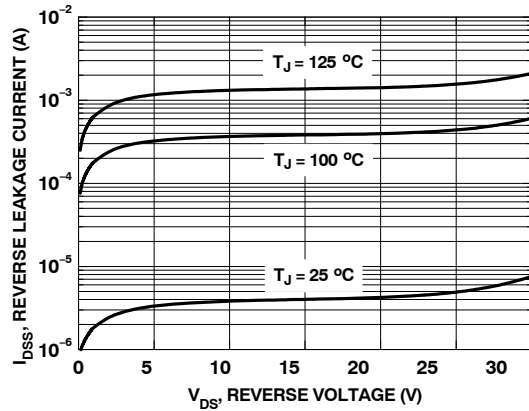
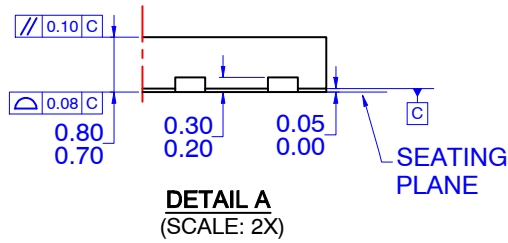
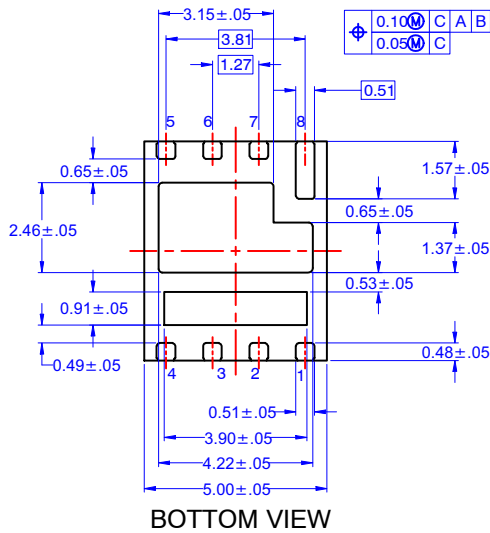
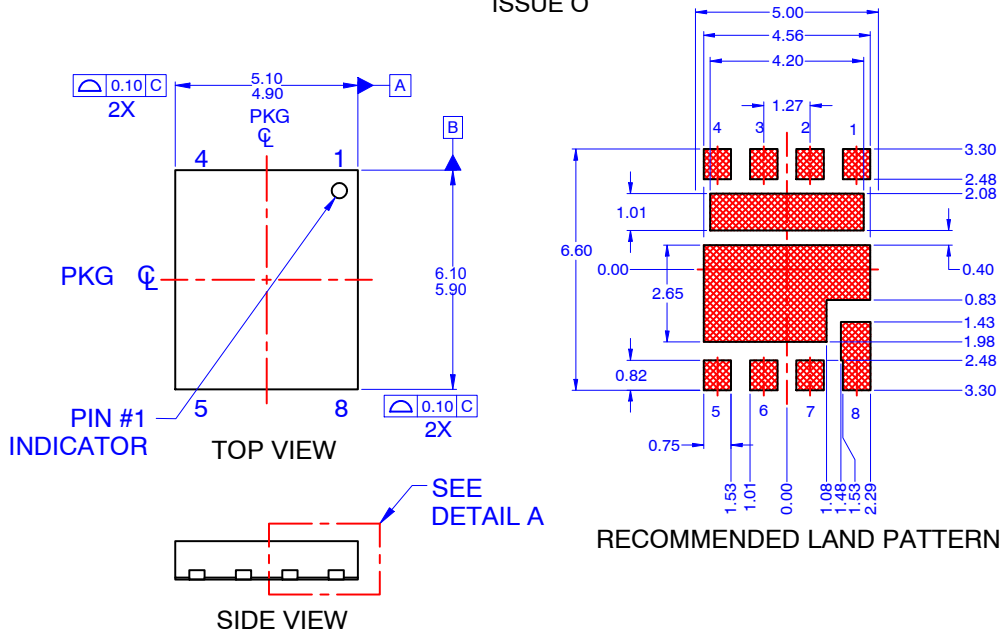


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

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PACKAGE DIMENSIONS


PQFN8 5X6, 1.27P
CASE 483AR
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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