

# NTMFD4H088NF

## PowerPhase, Dual N-Channel SO8FL 30 V, High Side 20 A / Low Side 42 A

### Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- Low Side MOSFET with Integrated Schottky
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- DC-DC Converters
- System Voltage Rails
- Point of Load

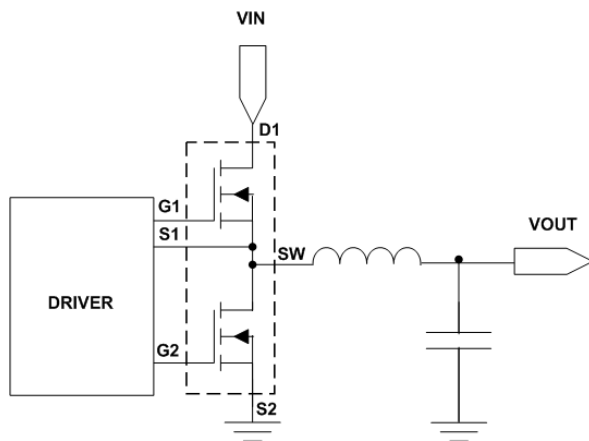


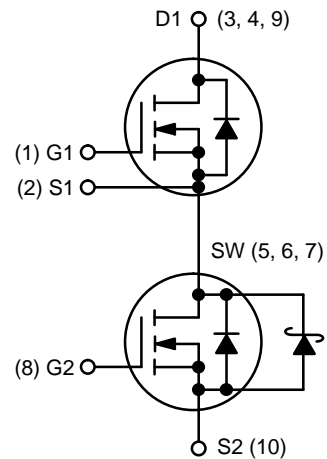
Figure 1. Typical Application Circuit



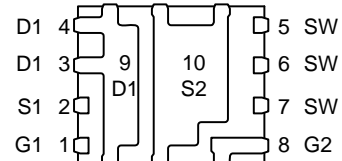
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
Q1 Top FET 30 V	7.2 mΩ @ 10 V	20 A
	11.3 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	1.5 mΩ @ 10 V	42 A
	2 mΩ @ 4.5 V	

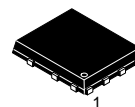


### PIN CONNECTIONS



(Bottom View)

### MARKING DIAGRAM



DFN8  
CASE 506CR



4H088N = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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**Table 1. MAXIMUM RATINGS** (T<sub>J</sub>=25°C unless otherwise stated)

Parameter			Symbol	Value	Units	
Drain-to-Source Voltage	Q1		V <sub>DSS</sub>	30	V	
	Q2					
Gate-to-Source Voltage	Q1		V <sub>GS</sub>	±12	V	
	Q2					
Continuous Drain Current R <sub>θJA</sub> (Note 1)	Q1	Steady State	I <sub>D</sub>	T <sub>A</sub> = 25°C	13.6	A
				T <sub>A</sub> = 85°C	9.8	
	Q2			T <sub>A</sub> = 25°C	28.2	
				T <sub>A</sub> = 85°C	20.3	
Power Dissipation R <sub>θJA</sub> (Note 1)	Q1		P <sub>D</sub>	2.32	W	
	Q2					
Continuous Drain Current R <sub>θJA</sub> ≤ 10 s (Note 1)	Q1	Steady State	I <sub>D</sub>	T <sub>A</sub> = 25°C	20.5	A
				T <sub>A</sub> = 85°C	15.9	
	Q2			T <sub>A</sub> = 25°C	42.3	
				T <sub>A</sub> = 85°C	28.2	
Power Dissipation R <sub>θJA</sub> ≤ 10 s (Note 1)	Q1		P <sub>D</sub>	5.2	W	
	Q2					
Continuous Drain Current R <sub>θJA</sub> (Note 2)	Q1	Steady State	I <sub>D</sub>	T <sub>A</sub> = 25°C	10.3	A
				T <sub>A</sub> = 85°C	7.5	
	Q2			T <sub>A</sub> = 25°C	21.4	
				T <sub>A</sub> = 85°C	15.4	
Power Dissipation R <sub>θJA</sub> (Note 2)	Q1		P <sub>D</sub>	1.33	W	
	Q2					
Pulsed Drain Current	Q1		I <sub>DM</sub>	186	A	
	Q2			491		
Operating Junction and Storage Temperature	Q1		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C	
	Q2					
Source Current (Body Diode)	Q1		I <sub>S</sub>	10	A	
	Q2			10		
Drain to Source DV/DT			dV/dt	7	V/ns	
Single Pulse Drain-to-Source Avalanche Energy	I <sub>L</sub> = 18 A <sub>pk</sub>	Q1	EAS	16	mJ	
	I <sub>L</sub> = 44 A <sub>pk</sub>	Q2	EAS	97		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm<sup>2</sup>.

**Table 2. THERMAL RESISTANCE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Junction-to-Ambient – Steady State (Note 3)	R <sub>θJA</sub>	53.9	°C/W
Junction-to-Ambient – Steady State (Note 4)		93.6	
Junction-to-Ambient – (t ≤ 10 s) (Note 3)		23.9	

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu
4. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm<sup>2</sup>

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**Table 3. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	FET	Test Condition	Min	Typ	Max	Units		
<b>OFF CHARACTERISTICS</b>									
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	Q1	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V		
		Q2	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	30					
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	Q1			17		mV/°C		
		Q2			26				
Zero Gate Voltage Drain Current	$I_{DSS}$	Q1	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$		
				$T_J = 125^\circ\text{C}$		20			
		Q2		$T_J = 25^\circ\text{C}$		50		500	
Gate-to-Source Leakage Current	$I_{GSS}$	Q1	$V_{DS} = 0\text{ V}, V_{GS} = 12\text{ V}$			100	nA		
		Q2				100			
<b>ON CHARACTERISTICS</b> (Note 5)									
Gate Threshold Voltage	$V_{GS(TH)}$	Q1	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3		2.3	V		
		Q2	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$	1.3		2.3			
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	Q1			4.4		mV/°C		
		Q2			3.6				
Drain-to-Source On Resistance	$R_{DS(on)}$	Q1	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$		6	7.2	m $\Omega$	
			$V_{GS} = 4.5\text{ V}$	$I_D = 15\text{ A}$		9	11.3		
		Q2	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$		1.2	1.5		
			$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$		1.6	2		
<b>CAPACITANCES</b>									
Input Capacitance	$C_{ISS}$	Q1	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		612		pF		
		Q2			3500				
Output Capacitance	$C_{OSS}$	Q1			280				
		Q2			1530				
Reverse Capacitance	$C_{RSS}$	Q1			12				
		Q2			70				
<b>CHARGES &amp; GATE RESISTANCE</b>									
Total Gate Charge	$Q_{G(TOT)}$	Q1	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 15\text{ A}$		4.5		nC		
		Q2			21				
Threshold Gate Charge	$Q_{G(TH)}$	Q1			3				
		Q2			2.8				
Gate-to-Source Charge	$Q_{GS}$	Q1			2				
		Q2			9				
Gate-to-Drain Charge	$Q_{GD}$	Q1			0.9				
		Q2			4				
Total Gate Charge	$Q_{G(TOT)}$	Q1		$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 15\text{ A}$		10			nC
		Q2				48			
Gate Resistance	$R_G$	Q1	$T_A = 25^\circ\text{C}$		1.3		$\Omega$		
		Q2			0.6				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

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**Table 3. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	FET	Test Condition	Min	Typ	Max	Units
<b>SWITCHING CHARACTERISTICS</b> (Note 6)							
Turn-On Delay Time	$t_{d(\text{ON})}$	Q1	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 20\text{ A}, R_G = 3.0\ \Omega$		7.76		ns
		Q2			15.5		
Rise Time	$t_r$	Q1			36		
		Q2			19		
Turn-Off Delay Time	$t_{d(\text{OFF})}$	Q1			11		
		Q2			26.5		
Fall Time	$t_f$	Q1			1.8		
		Q2			5.4		

**SWITCHING CHARACTERISTICS** (Note 6)

Turn-On Delay Time	$t_{d(\text{ON})}$	Q1	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 20\text{ A}, R_G = 3.0\ \Omega$		5		ns
		Q2			11		
Rise Time	$t_r$	Q1			34		
		Q2			16.7		
Turn-Off Delay Time	$t_{d(\text{OFF})}$	Q1			14		
		Q2			34		
Fall Time	$t_f$	Q1			1.5		
		Q2			3.8		

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Forward Voltage	$V_{SD}$	Q1	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.0	V
				$T_J = 125^\circ\text{C}$		0.7		
		Q2		$T_J = 25^\circ\text{C}$		0.5	0.8	
				$T_J = 125^\circ\text{C}$		0.4		

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Reverse Recovery Time	$t_{RR}$	Q1	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 2\text{ A}$		20		ns	
		Q2			51			
Charge Time	$t_a$	Q1			11.6			
		Q2			27			
Discharge Time	$t_b$	Q1			8.4			
		Q2			24			
Reverse Recovery Charge	$Q_{RR}$	Q1			10			nC
		Q2			70			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

6. Switching characteristics are independent of operating junction temperatures

**Table 4. ORDERING INFORMATION**

Device	Package	Shipping†
NTMFD4H088NFT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NTMFD4H088NFT3G	DFN8 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## TYPICAL CHARACTERISTICS – Q1

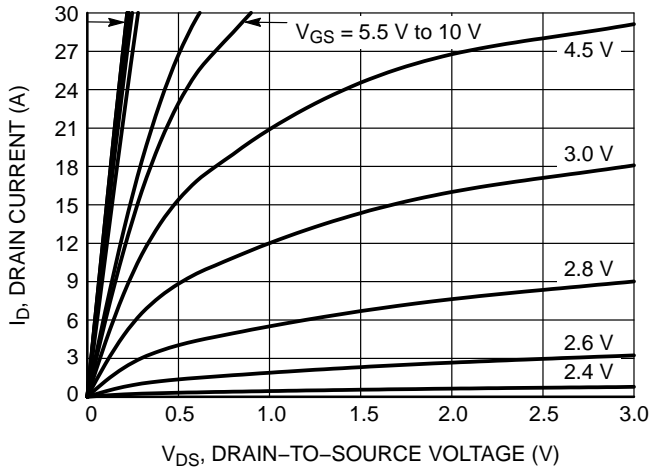


Figure 2. On-Region Characteristics

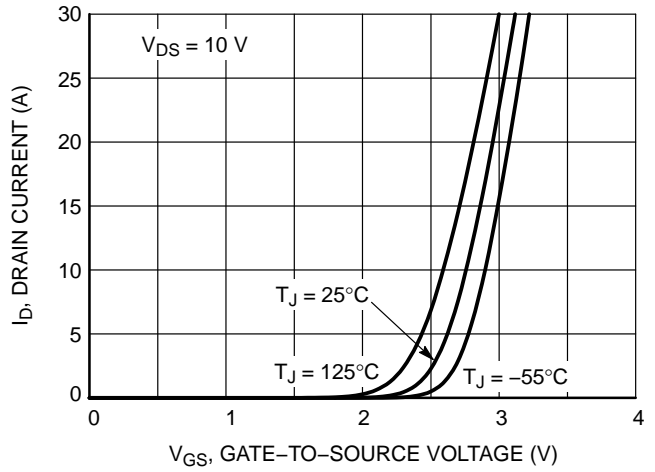


Figure 3. Transfer Characteristics

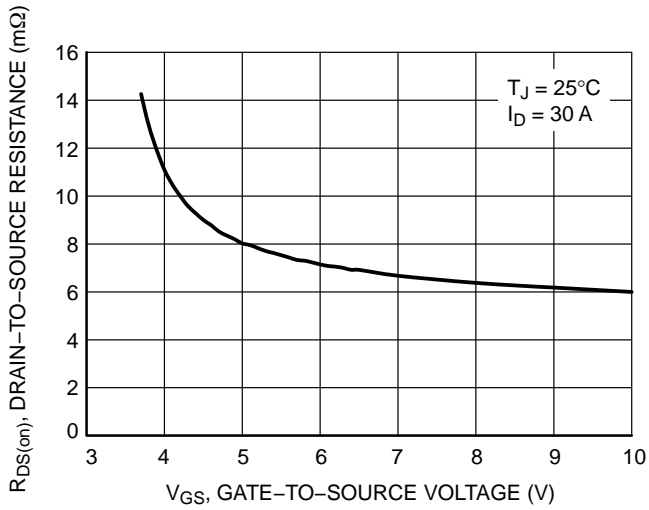


Figure 4. On-Resistance vs. Gate-to-Source Voltage

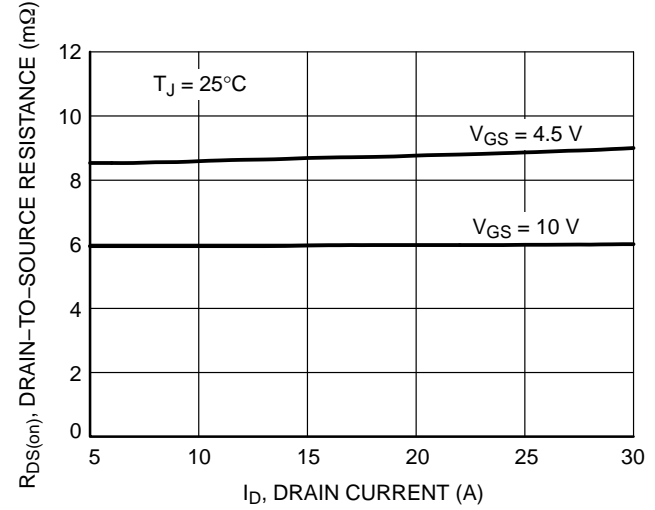


Figure 5. On-Resistance vs. Drain Current and Gate Voltage

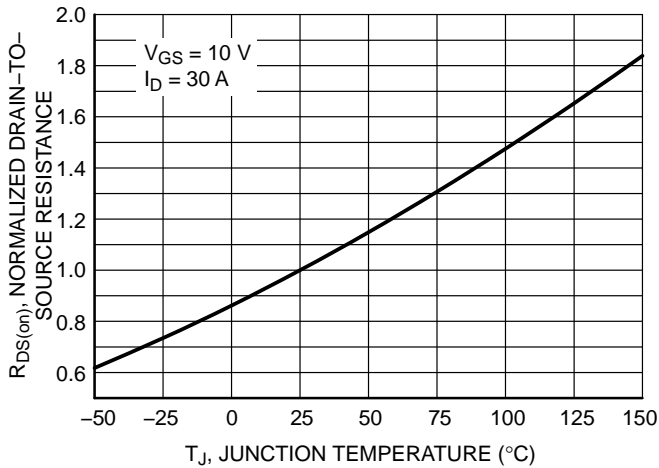


Figure 6. On-Resistance Variation with Temperature

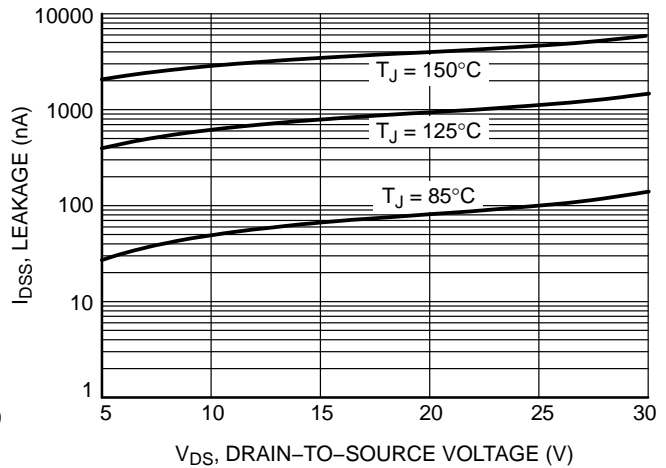


Figure 7. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS – Q1

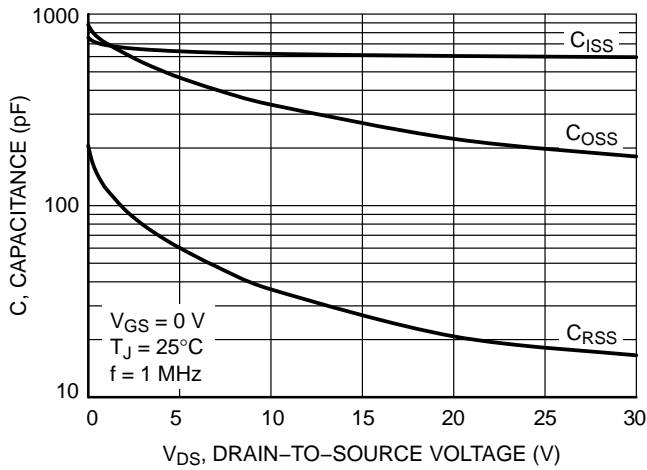


Figure 8. Capacitance Variation

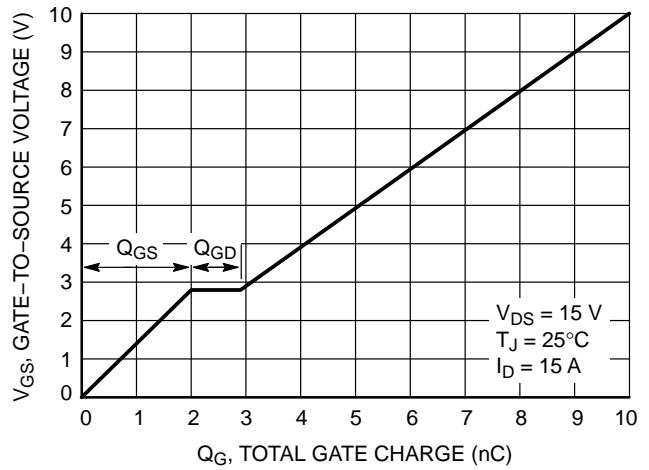


Figure 9. Gate-to-Source vs. Total Charge

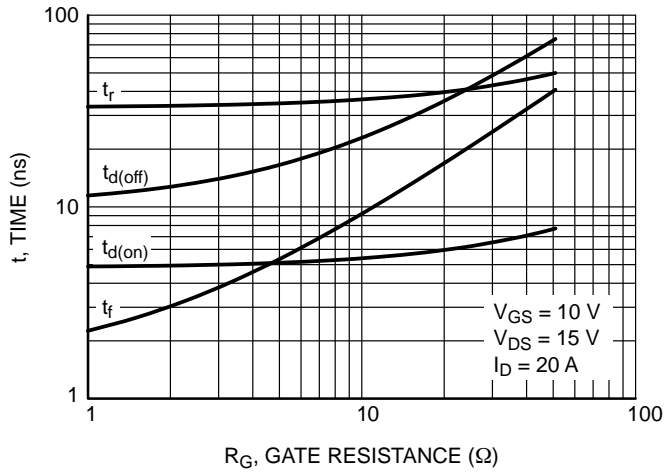


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

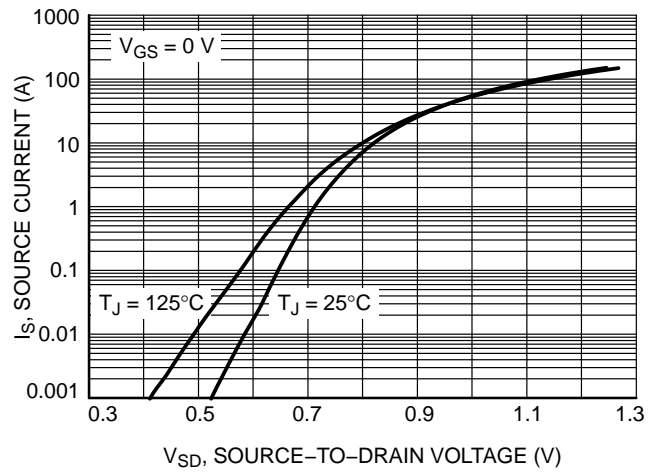


Figure 11. Diode Forward Voltage vs. Current

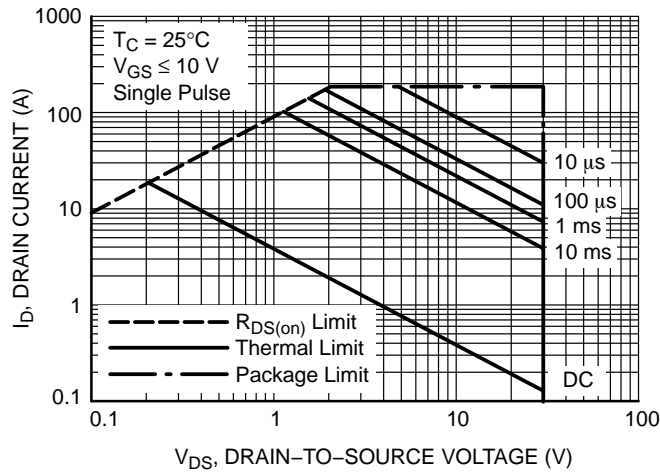


Figure 12. Maximum Rated Forward Biased Safe Operating Area

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## TYPICAL CHARACTERISTICS – Q1

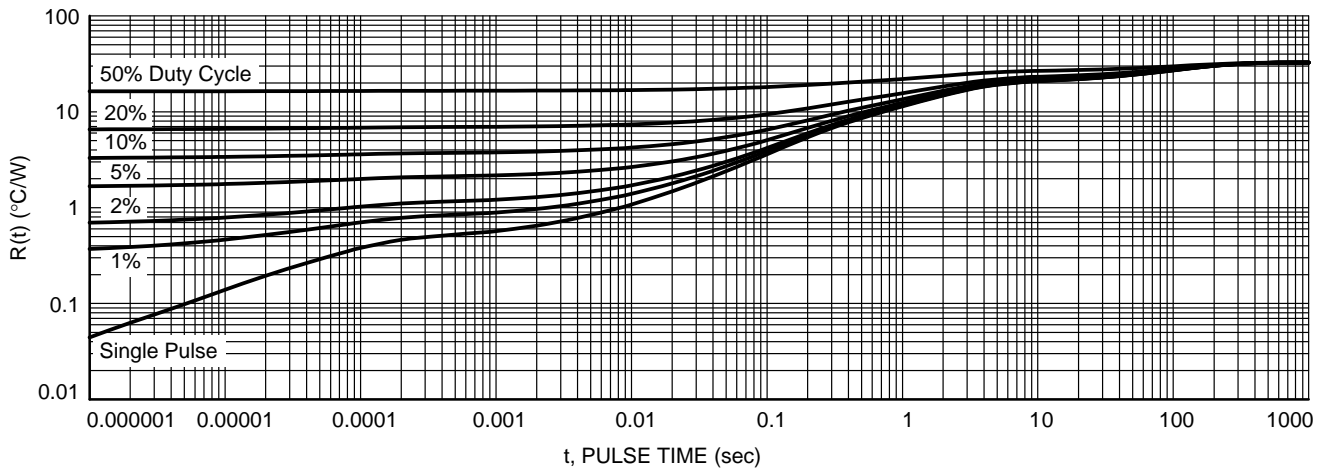


Figure 13. Thermal Response

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## TYPICAL CHARACTERISTICS – Q2

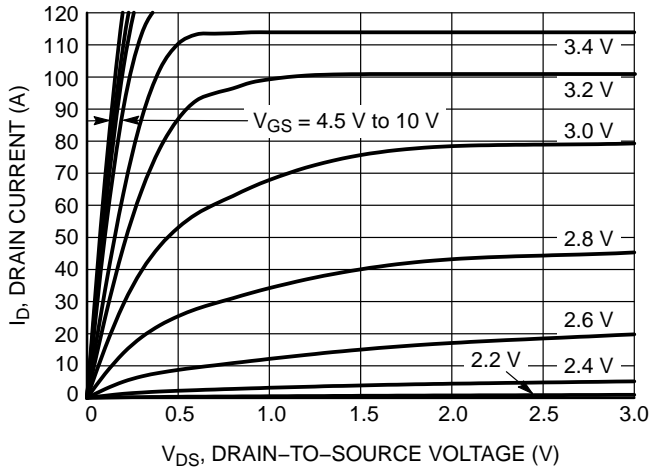


Figure 14. On-Region Characteristics

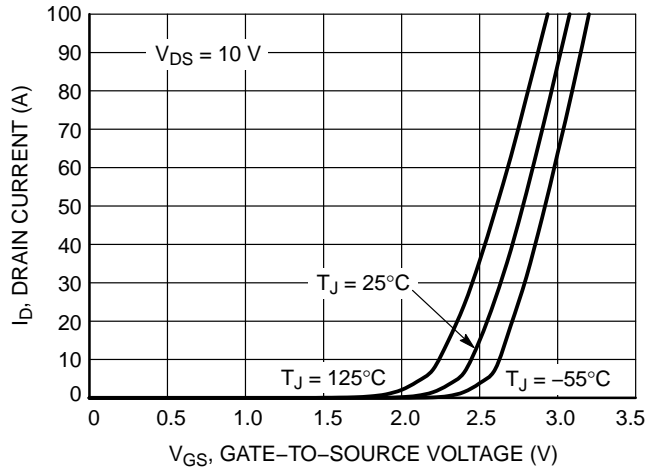


Figure 15. Transfer Characteristics

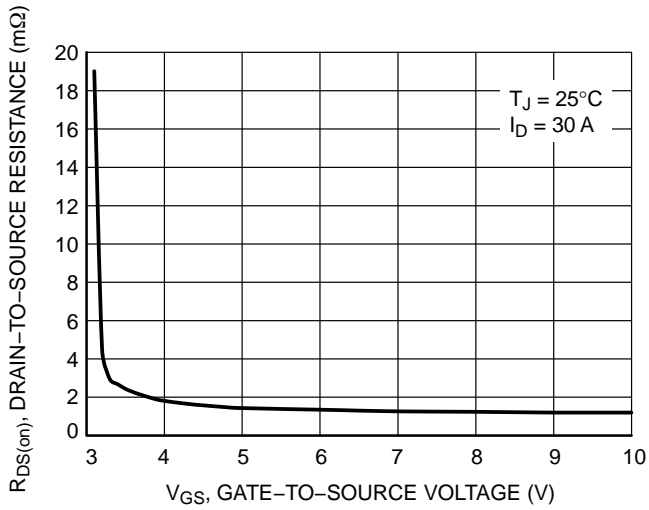


Figure 16. On-Resistance vs. Gate-to-Source Voltage

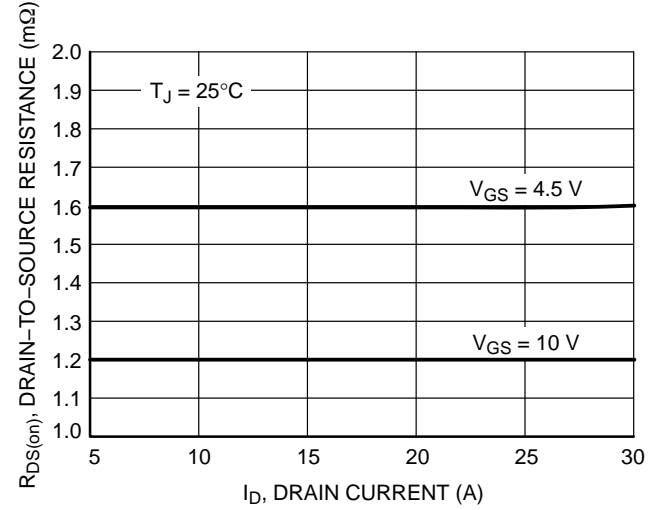


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

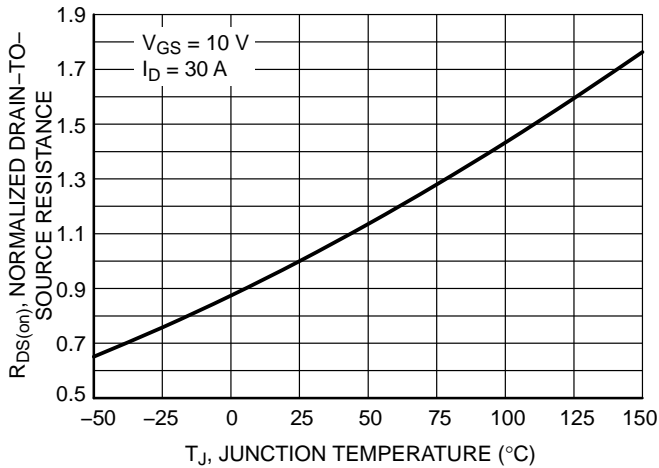


Figure 18. On-Resistance Variation with Temperature

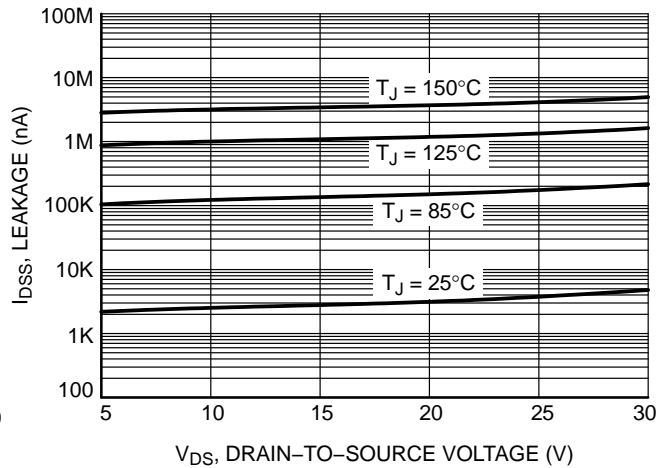


Figure 19. Drain-to-Source Leakage Current vs. Voltage



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## TYPICAL CHARACTERISTICS – Q2

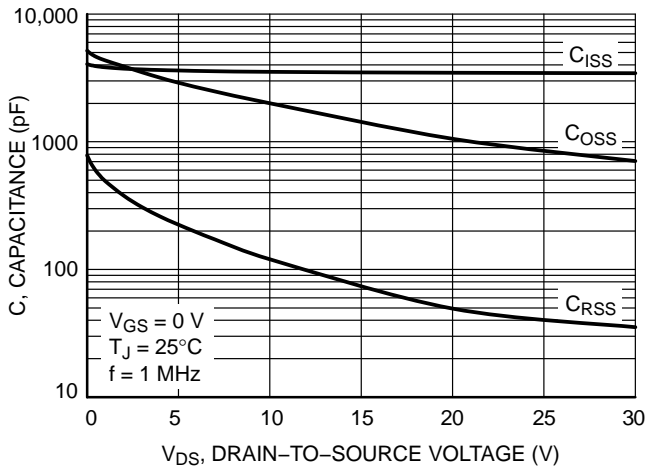


Figure 20. Capacitance Variation

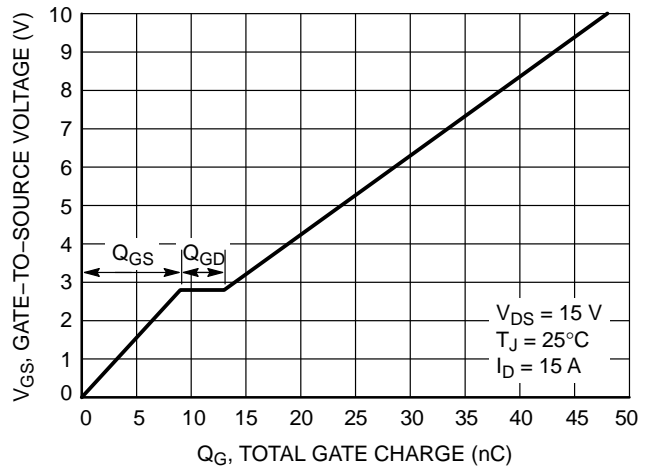


Figure 21. Gate-to-Source vs. Total Charge

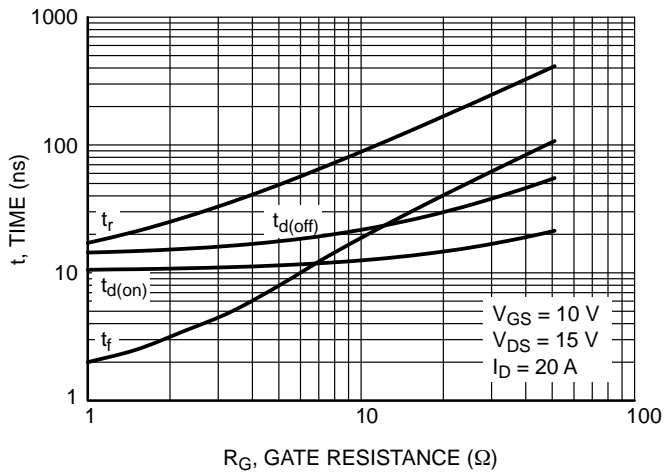


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

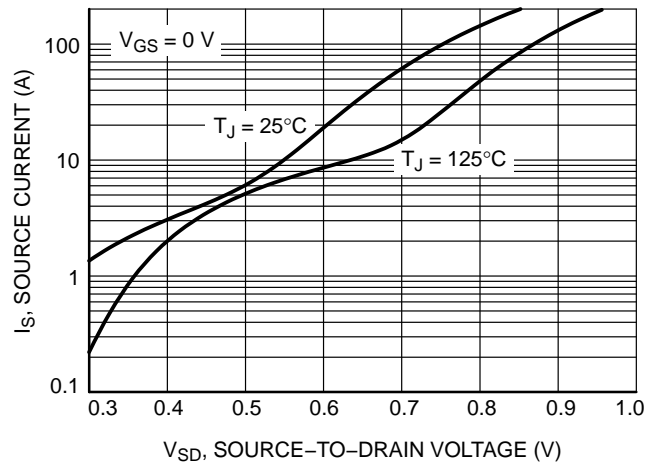


Figure 23. Diode Forward Voltage vs. Current

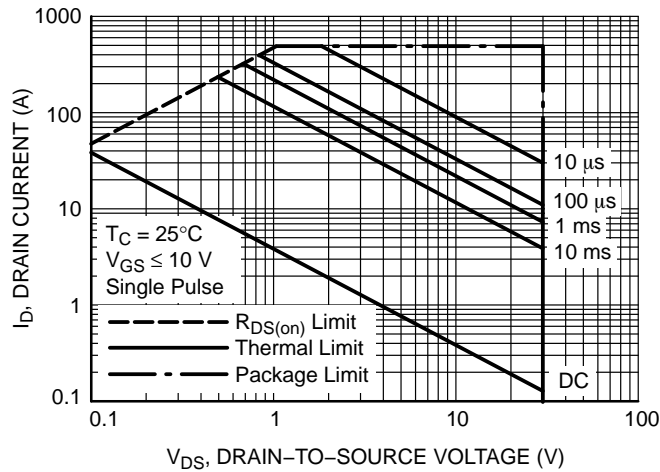


Figure 24. Maximum Rated Forward Biased Safe Operating Area

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## TYPICAL CHARACTERISTICS – Q2

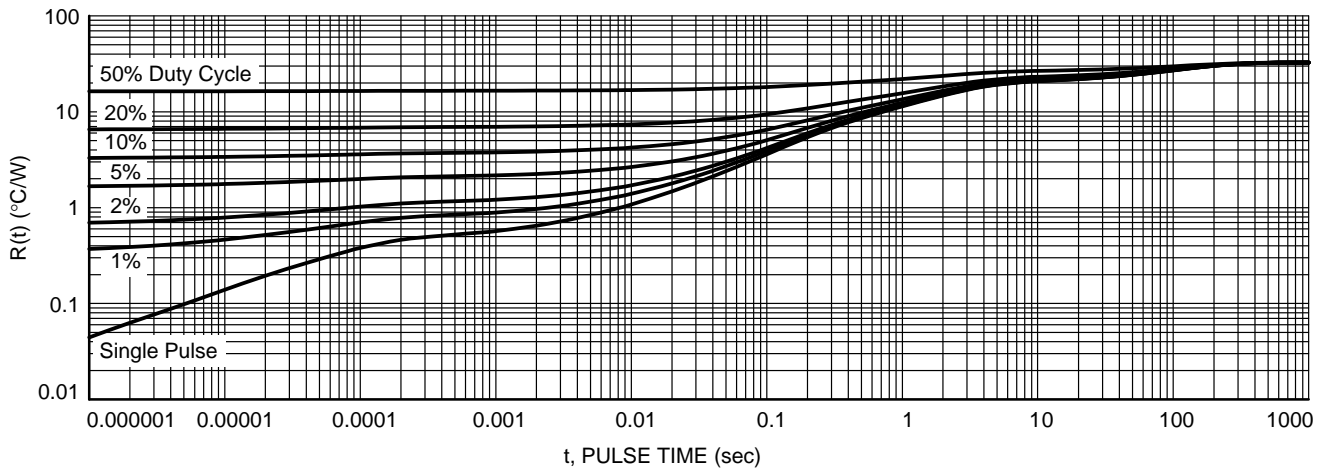
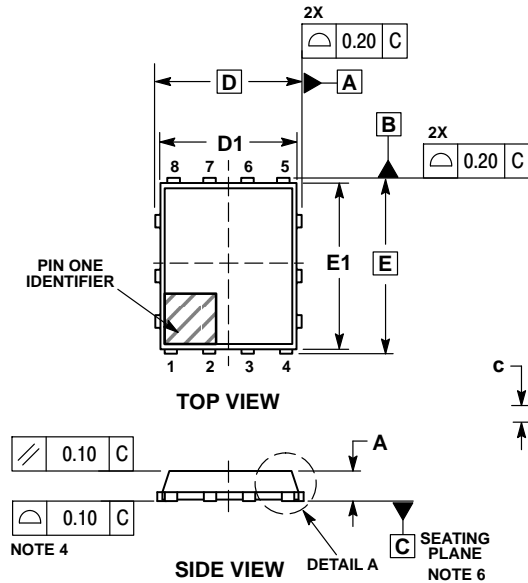


Figure 25. Thermal Response

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## PACKAGE DIMENSIONS

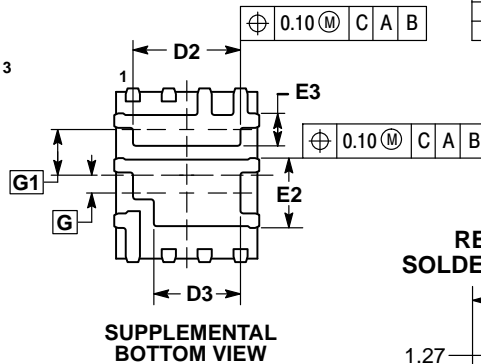
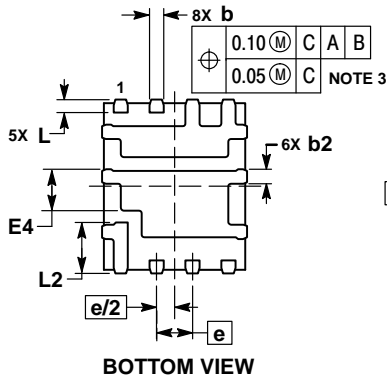
DFN8 5x6, 1.27P PowerPhase FET  
CASE 506CR  
ISSUE C



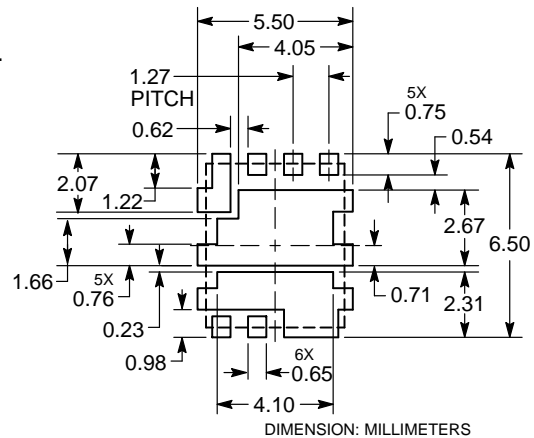
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND b1 APPLY TO PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
A1	0.00	0.05
b	0.40	0.60
b2	0.40	0.60
c	0.20	0.30
D	5.15 BSC	
D1	4.90	5.10
D2	3.70	3.90
D3	2.96	3.16
E	6.15 BSC	
E1	5.80	6.00
E2	2.37	2.57
E3	1.05	1.25
E4	1.36	1.56
e	1.27 BSC	
G	0.625 BSC	
G1	1.615 BSC	
h	12 °	
L	0.34	0.59
L2	1.68	1.93




**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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