

NTMFS006N12MC

Product Preview

Power MOSFET

120 V, 6.0 mΩ, TBD A, Single N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Soft Body Diode Reduces Voltage Ringing
- These Devices are Pb-Free, Halogen-Free / BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	120	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	I_D	TBD
		$T_C = 25^\circ\text{C}$	P_D	TBD
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	TBD
		$T_A = 25^\circ\text{C}$	P_D	TBD
Pulsed Drain Current		$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	TBD
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	TBD	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{AV} = \text{TBD A}, L = \text{TBD mH}$)		E_{AS}	TBD	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		T_L	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{\theta JC}$	TBD	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	TBD	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 1 in² pad size, 2 oz. Cu pad.

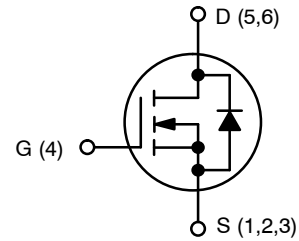
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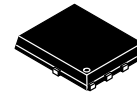
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
120 V	6.0 mΩ @ 10 V	TBD A
	TBD mΩ @ 6 V	

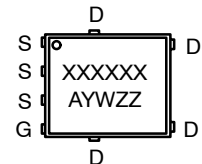


N-CHANNEL MOSFET



SO-8
FLAT LEAD
CASE 488AA

MARKING DIAGRAM



XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS006N12MC	PQFN56 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	120			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		TBD		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = \text{TBD V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = \text{TBD}\ \mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		TBD		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = \text{TBD A}$		TBD	6.0	m Ω
		$V_{GS} = 6\text{ V}, I_D = \text{TBD A}$		TBD	TBD	
Forward Transconductance	g_{FS}	$V_{DS} = \text{TBD V}, I_D = \text{TBD A}$		TBD		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		TBD		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 60\text{ V}$		2678		pF
Output Capacitance	C_{OSS}			1347		
Reverse Transfer Capacitance	C_{RSS}			28		
Total Gate Charge	$Q_G(\text{TOT})$	$V_{GS} = 10\text{ V}, V_{DS} = 60\text{ V}, I_D = \text{TBD A}$		44		nC
Total Gate Charge	$Q_G(\text{TOT})$	$V_{GS} = 6\text{ V}, V_{DS} = 60\text{ V}, I_D = \text{TBD A}$		TBD		
Gate-to-Source Charge	Q_{GS}			11		
Gate-to-Drain Charge	Q_{GD}			14		
Plateau Voltage	V_{GP}			TBD		V

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 60\text{ V}, I_D = \text{TBD A}, R_G = \text{TBD}\ \Omega$		TBD		ns
Rise Time	t_r			TBD		
Turn-Off Delay Time	$t_{d(OFF)}$			TBD		
Fall Time	t_f			TBD		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = \text{TBD A}$	$T_J = 25^\circ\text{C}$		0.9		V
			$T_J = 125^\circ\text{C}$		TBD		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 300\text{ A}/\mu\text{s}, I_S = \text{TBD A}$		TBD		ns	
Reverse Recovery Charge	Q_{RR}			TBD		nC	
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = \text{TBD A}$		TBD		ns	
Reverse Recovery Charge	Q_{RR}			TBD		nC	

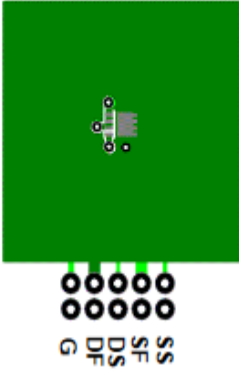
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

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NOTES:

4. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

5. Pulse Test: Pulse Width < TBD. Duty cycle < TBD.
6. E_{AS} of TBD is based on started $T_J = 25^\circ\text{C}$, $L = \text{TBD}$, $I_{AS} = \text{TBD}$, $V_{DD} = \text{TBD}$, $V_{GS} = \text{TBD}$. 100% test at $L = \text{TBD}$, $I_{AS} = \text{TBD}$.
7. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

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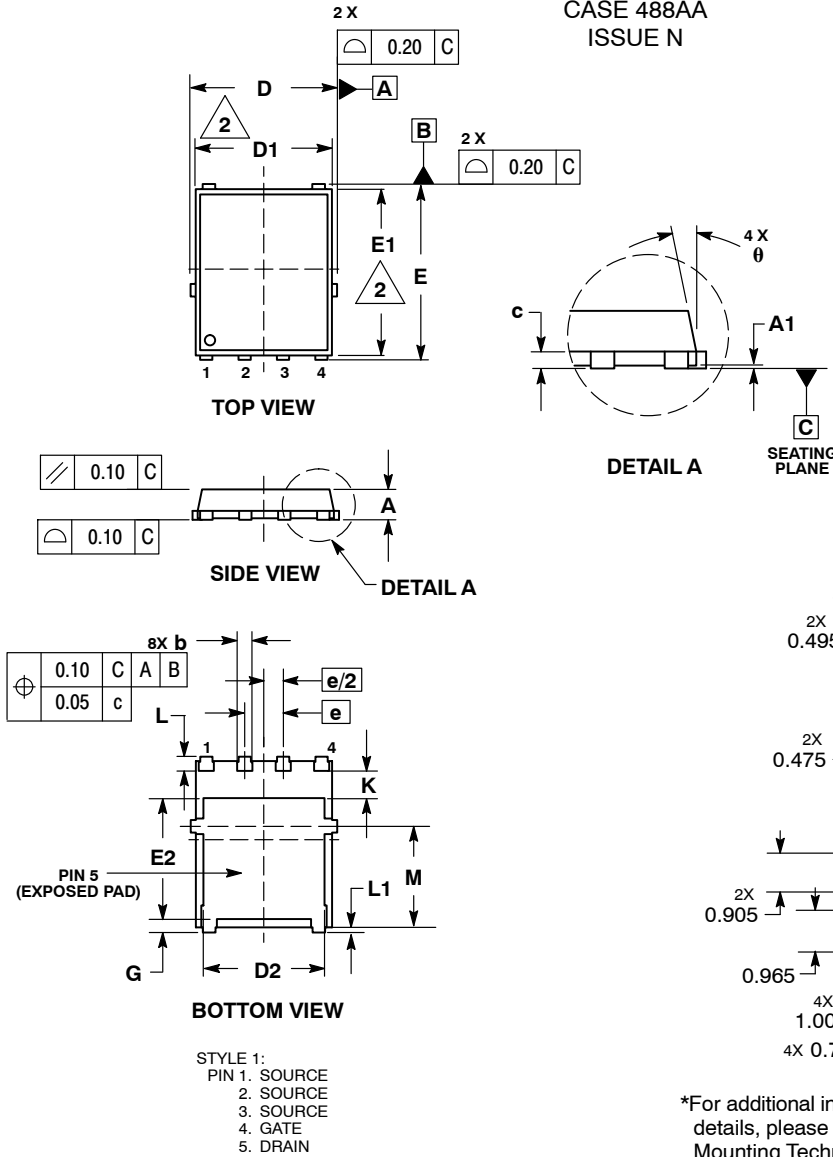
PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

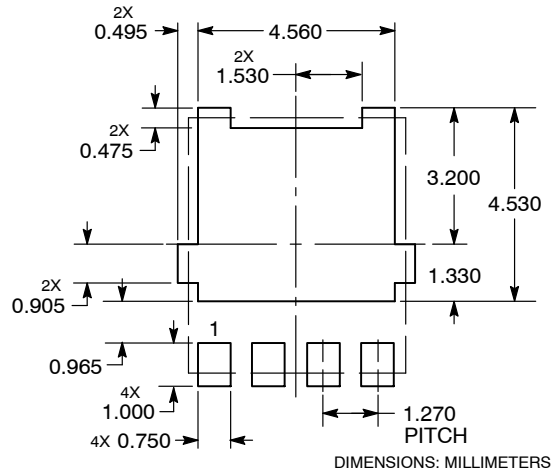
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	---	12 °



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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