# Product Preview

# **Power MOSFET**

# 120 V, 8.0 m $\Omega$ , TBD A, Single N-Channel

### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- Soft Body Diode Reduces Voltage Ringing
- These Devices are Pb-Free, Halogen-Free / BFR Free and are RoHS Compliant

## **Typical Applications**

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	120	V
Gate-to-Source Voltage	€		V <sub>GS</sub>	±20	٧
Continuous Drain Current R <sub>θJC</sub> (Note 2)			I <sub>D</sub>	TBD	Α
Power Dissipation $R_{\theta JC}$ (Note 2)	State	T <sub>C</sub> = 25°C	P <sub>D</sub>	TBD	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady	T <sub>A</sub> = 25°C	Ι <sub>D</sub>	TBD	Α
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)	State	T <sub>A</sub> = 25°C	P <sub>D</sub>	TBD	W
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \ \mu s$		I <sub>DM</sub>	TBD	Α
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Source Current (Body Diode)			IS	TBD	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>AV</sub> = TBD A, L = TBD mH)			E <sub>AS</sub>	TBD	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			TL	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{\theta JC}$	TBD	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	TBD	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 1 in<sup>2</sup> pad size, 2 oz. Cu pad.

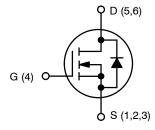
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V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
120 V	8.0 mΩ @ 10 V	TBD A
	TBD mΩ @ 6 V	TODA

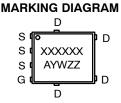


**N-CHANNEL MOSFET** 



SO<sub>-8</sub> **FLAT LEAD** CASE 488AA

Υ



XXXXXX = Specific Device Code Α

= Assembly Location

= Year

W = Work Week 77 = Lot Traceability

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTMFS008N12MC	PQFN56 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

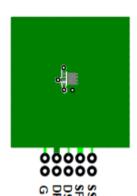
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•	•			•		•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		120			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /	I <sub>D</sub> = 250 μA, ref to 25°C			TBD		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$ ,	T <sub>J</sub> = 25°C			1	μΑ
		V <sub>DS</sub> = TBD V	T <sub>J</sub> = 125°C			100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub>	= ±20 V			±100	nA
ON CHARACTERISTICS (Note 3)	•	•			•	•	•
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D =$	TBD μA	2.0		4.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref	to 25°C		TBD		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> :	= TBD A		TBD	8.0	mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub> =	TBD A		TBD	TBD	
Forward Transconductance	9FS	V <sub>DS</sub> = TBD V, I <sub>D</sub>	= TBD A		TBD		S
Gate Resistance	$R_{G}$	T <sub>A</sub> = 25°	С		TBD		Ω
CHARGES & CAPACITANCES	•					1	
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 60 V			2086		pF
Output Capacitance	C <sub>OSS</sub>				1049		
Reverse Transfer Capacitance	C <sub>RSS</sub>				22		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 60 V, I <sub>D</sub> = TBD A			34		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	$V_{GS} = 6 \text{ V}, V_{DS} = 60 \text{ V}, I_{D} = \text{TBD A}$			TBD		
Gate-to-Source Charge	Q <sub>GS</sub>				11		
Gate-to-Drain Charge	$Q_{GD}$				8		
Plateau Voltage	$V_{GP}$	1			TBD		V
SWITCHING CHARACTERISTICS (Note 3)	•				•	•	•
Turn-On Delay Time	t <sub>d(ON)</sub>	$V_{GS} = 10 \text{ V}, V_{DS}$	s = 60 V,		TBD		ns
Rise Time	t <sub>r</sub>	$I_D = TBD A, R_G = I_D A$	= TBD Ω		TBD		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>				TBD		
Fall Time	t <sub>f</sub>				TBD		
DRAIN-SOURCE DIODE CHARACTERISTIC	s	•				1	
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = TBD A	T <sub>J</sub> = 25°C		0.9		V
			T <sub>J</sub> = 125°C		TBD		1
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } dI_S/dt = 300 \text{ A/}\mu\text{s,}$ $I_S = TBD \text{ A}$			TBD		ns
Reverse Recovery Charge	Q <sub>RR</sub>				TBD		nC
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS}$ = 0 V, $dI_S/dt$ = 1000 A/ $\mu$ s, $I_S$ = TBD A			TBD		ns
Reverse Recovery Charge	Q <sub>RR</sub>				TBD		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

### NOTES:

4.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



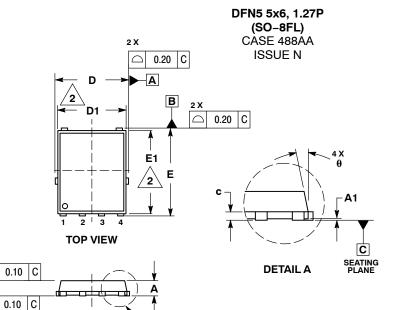
a. 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < TBD. Duty cycle < TBD.</li>
   E<sub>AS</sub> of TBD is based on started T<sub>J</sub> = 25°C, L = TBD, I<sub>AS</sub> = TBD, V<sub>DD</sub> = TBD, V<sub>GS</sub> = TBD. 100% test at L = TBD, I<sub>AS</sub> = TBD.
   As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

#### PACKAGE DIMENSIONS



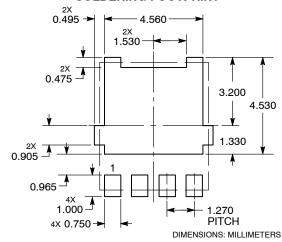
**DETAIL A** 

#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
С	0.23	0.28	0.33	
D	5.00	5.15	5.30	
D1	4.70	4.90	5.10	
D2	3.80	4.00	4.20	
E	6.00	6.15	6.30	
E1	5.70	5.90	6.10	
E2	3.45	3.65	3.85	
е	1.27 BSC			
G	0.51	0.575	0.71	
K	1.20	1.35	1.50	
L	0.51	0.575	0.71	
L1	0.125 REF			
М	3.00	3.40	3.80	
θ	0 °		12 °	

#### RECOMMENDED **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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SIDE VIEW

D2

**BOTTOM VIEW** 

STYLE 1: PIN 1. SOURCE

3. 4. SOURCE

SOURCE

GATE 5 DRAIN e/2

8X b

F2

G

С A B

0.10

PIN 5 (EXPOSED PAD)

Œ 0.05 С

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