

# NTMFS4851N

## MOSFET – Power, Single, N-Channel, SO-8FL 30 V, 66 A

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Thermally Enhanced SO8 Package
- These are Pb-Free Devices

### Applications

- Refer to Application Note AND8195/D
- CPU Power Delivery
- DC-DC Converters
- High Side Switching

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

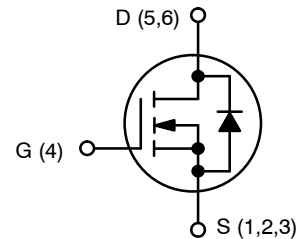
Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 16$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	15	A
		$T_A = 85^\circ\text{C}$	10.8	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	2.16	W	
Continuous Drain Current $R_{\theta JA} \leq 10$ sec	$I_D$	$T_A = 25^\circ\text{C}$	24.3	A
		$T_A = 85^\circ\text{C}$	17.5	
Power Dissipation $R_{\theta JA}, t \leq 10$ sec	$P_D$	5.67	W	
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	9.5	A
		$T_A = 85^\circ\text{C}$	6.9	
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	0.87	W	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	66	A
		$T_C = 85^\circ\text{C}$	47.8	
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	41.7	W	
Pulsed Drain Current	$I_{DM}$	132	A	
Current limited by package	$I_{Dmaxpkg}$	100	A	
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	41.7	A	
Drain to Source dV/dt	dV/dt	6	V/ns	



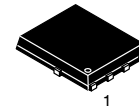
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$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
30 V	5.9 m $\Omega$ @ 10 V	66 A
	8.7 m $\Omega$ @ 4.5 V	

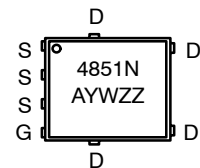


N-CHANNEL MOSFET



SO-8 FLAT LEAD  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4851NT1G	SO-8FL (Pb-Free)	1500 / Tape & Reel
NTMFS4851NT3G	SO-8FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 50\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_L = 27\text{ A}_{pk}$ , $L = 0.3\text{ mH}$ , $R_G = 25\ \Omega$ )	EAS	109	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.0	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	57.8	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	143.5	
Junction-to-Ambient – $t \leq 10$ sec	$R_{\theta JA}$	22.1	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			25		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.45	1.8	2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.6		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V to } 11.5\text{ V}$	$I_D = 30\text{ A}$		4.3	5.9	m $\Omega$
			$I_D = 15\text{ A}$		4.2		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$		6.6	8.7	
			$I_D = 15\text{ A}$		6.5		
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}, I_D = 30\text{ A}$		62		S	

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$		1850		pF
Output Capacitance	$C_{OSS}$			333		
Reverse Transfer Capacitance	$C_{RSS}$			170		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		13.5	20	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.7		
Gate-to-Source Charge	$Q_{GS}$			5.1		
Gate-to-Drain Charge	$Q_{GD}$			4.5		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		32		nC

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		14.4		ns
Rise Time	$t_r$			39.8		
Turn-Off Delay Time	$t_{d(OFF)}$			18.6		
Fall Time	$t_f$			5.2		

- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 4)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		9.5		ns
Rise Time	$t_r$			22		
Turn-Off Delay Time	$t_{d(OFF)}$			25		
Fall Time	$t_f$			4.6		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.84	1.0	V
			$T_J = 125^\circ\text{C}$		0.73		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$			13.2		ns
Charge Time	$t_a$				8.5		
Discharge Time	$t_b$				4.7		
Reverse Recovery Charge	$Q_{RR}$				3.5		

## PACKAGE PARASITIC VALUES

Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		0.93		nH
Drain Inductance	$L_D$			0.005		
Gate Inductance	$L_G$			1.84		
Gate Resistance	$R_G$			0.9		

- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

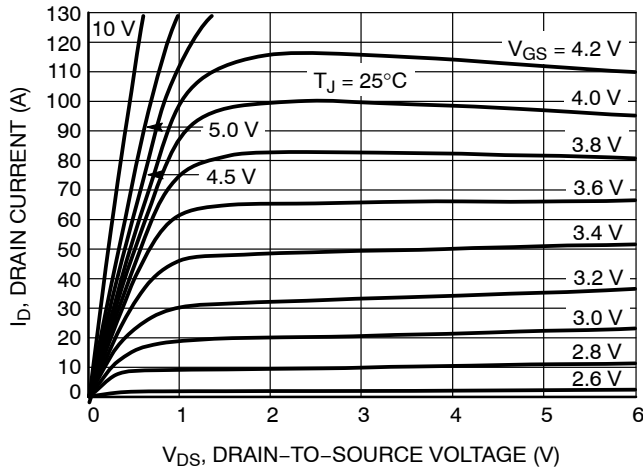


Figure 1. On-Region Characteristics

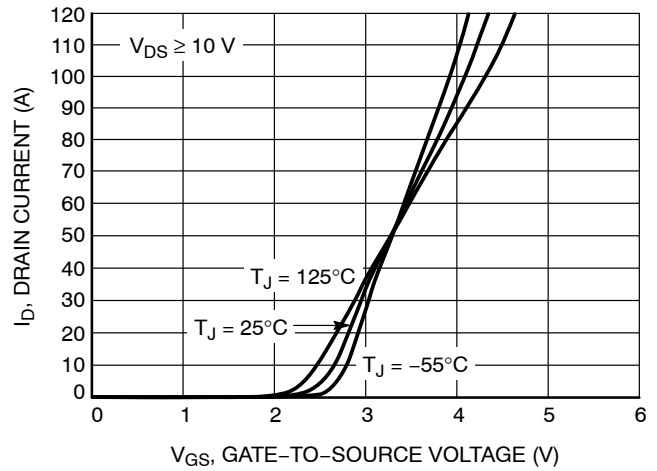
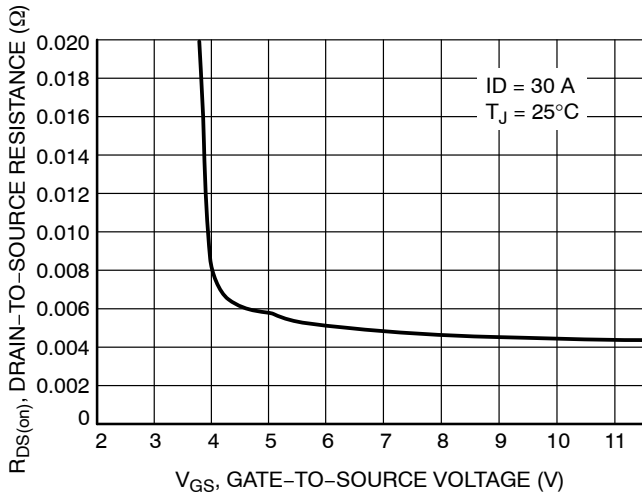


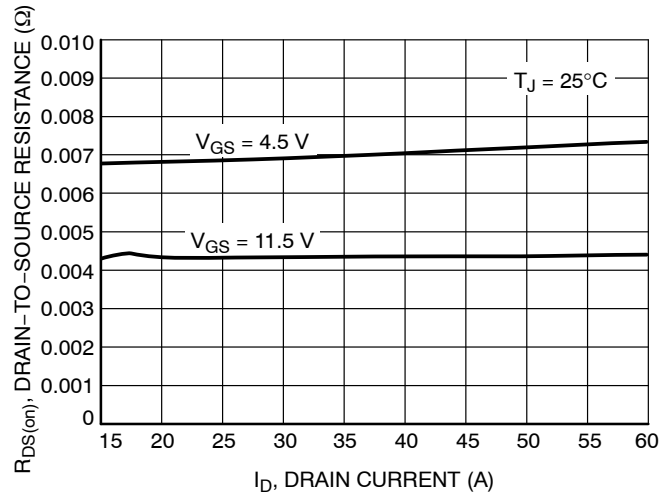
Figure 2. Transfer Characteristics

# NTMFS4851N

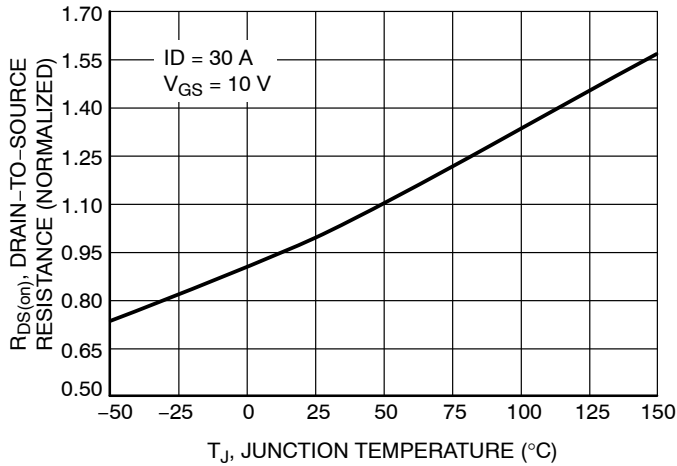
## TYPICAL CHARACTERISTICS



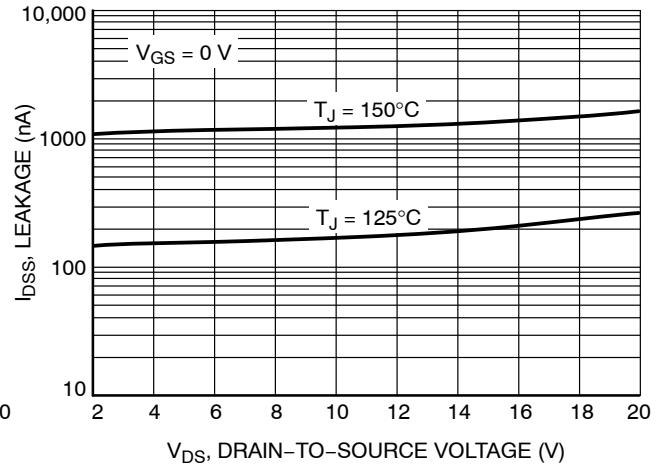
**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



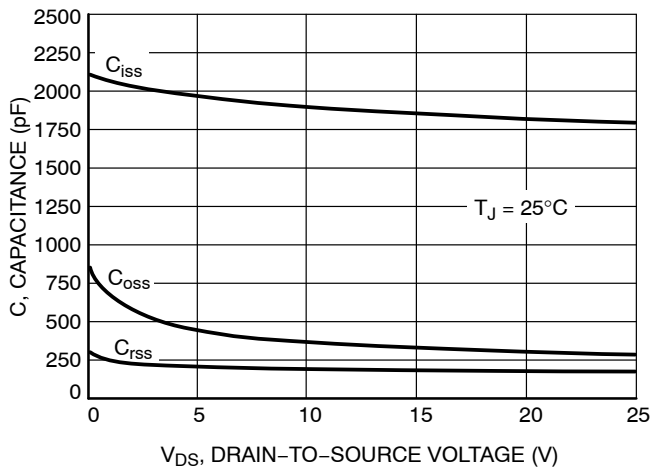
**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



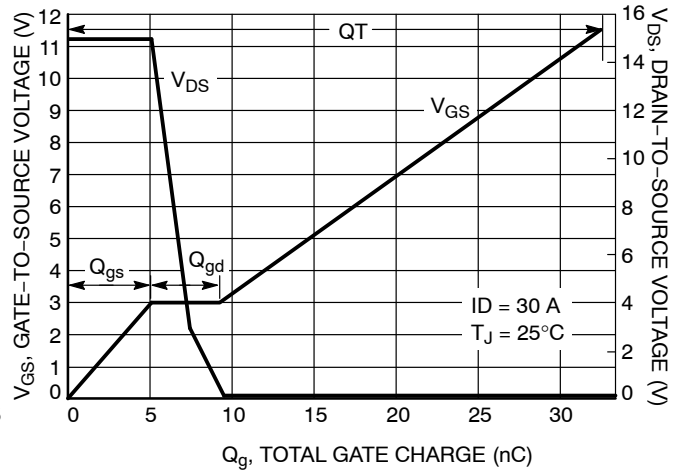
**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**



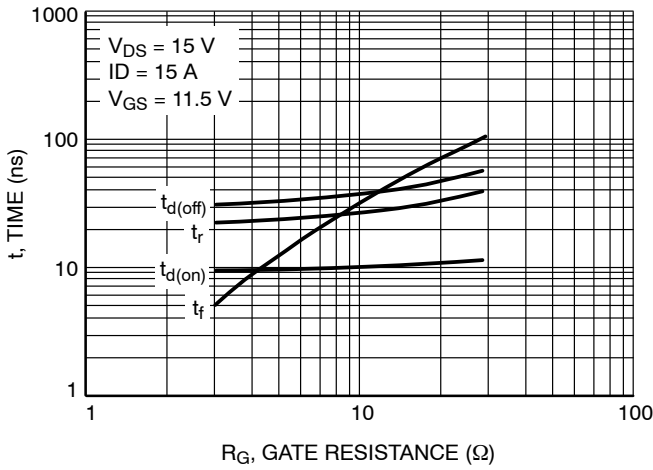
**Figure 7. Capacitance Variation**



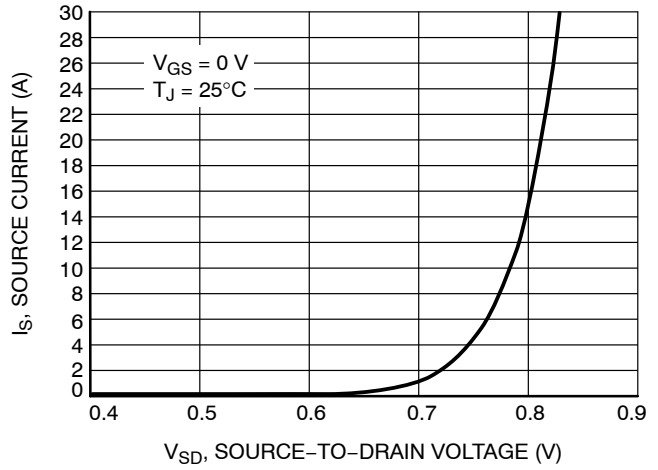
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**

# NTMFS4851N

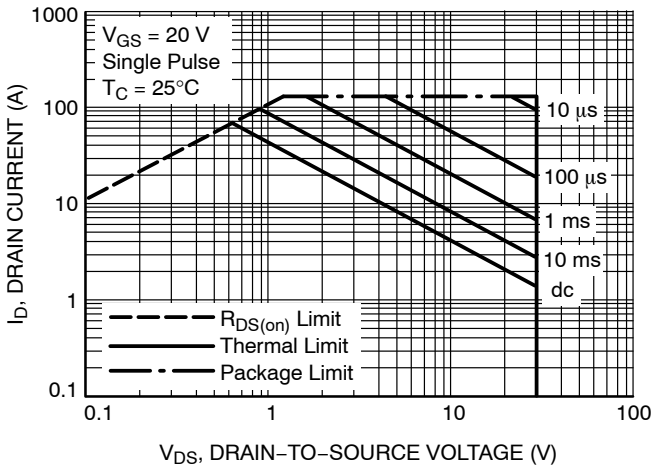
## TYPICAL CHARACTERISTICS



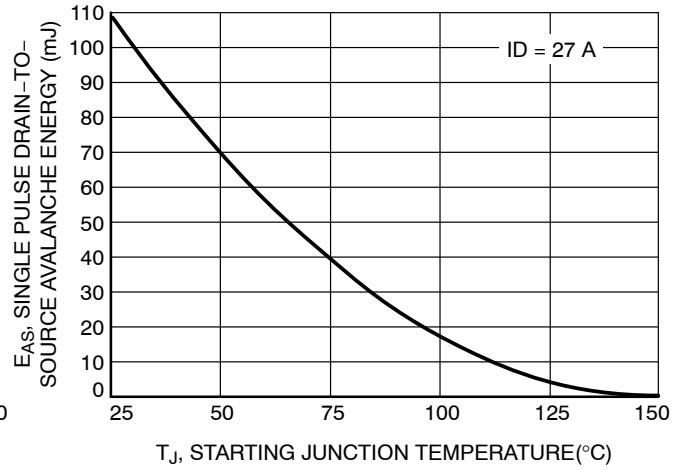
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



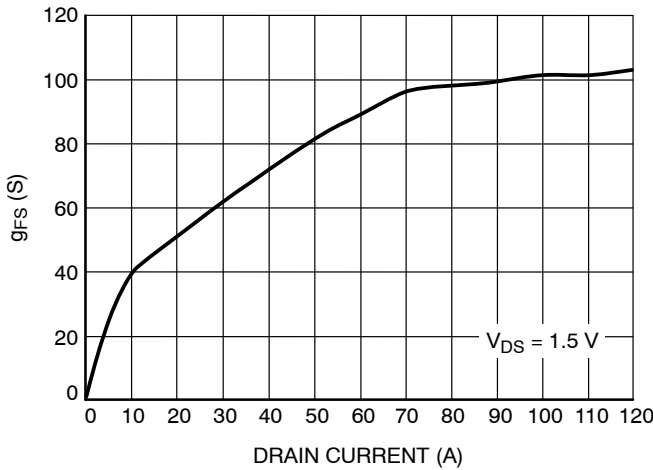
**Figure 10. Diode Forward Voltage vs. Current**



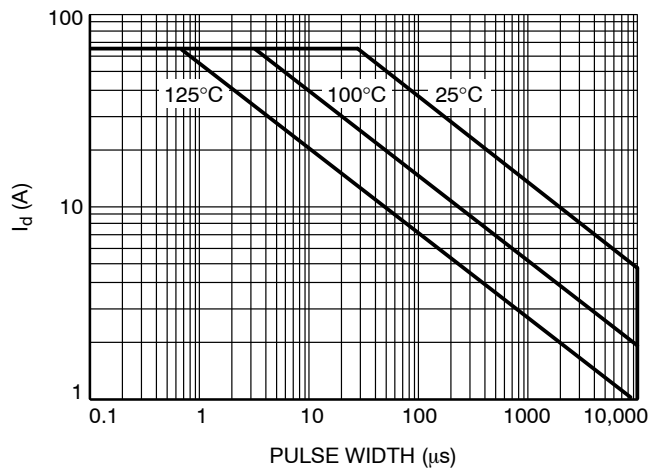
**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**



**Figure 13.  $g_{FS}$  vs. Drain Current**

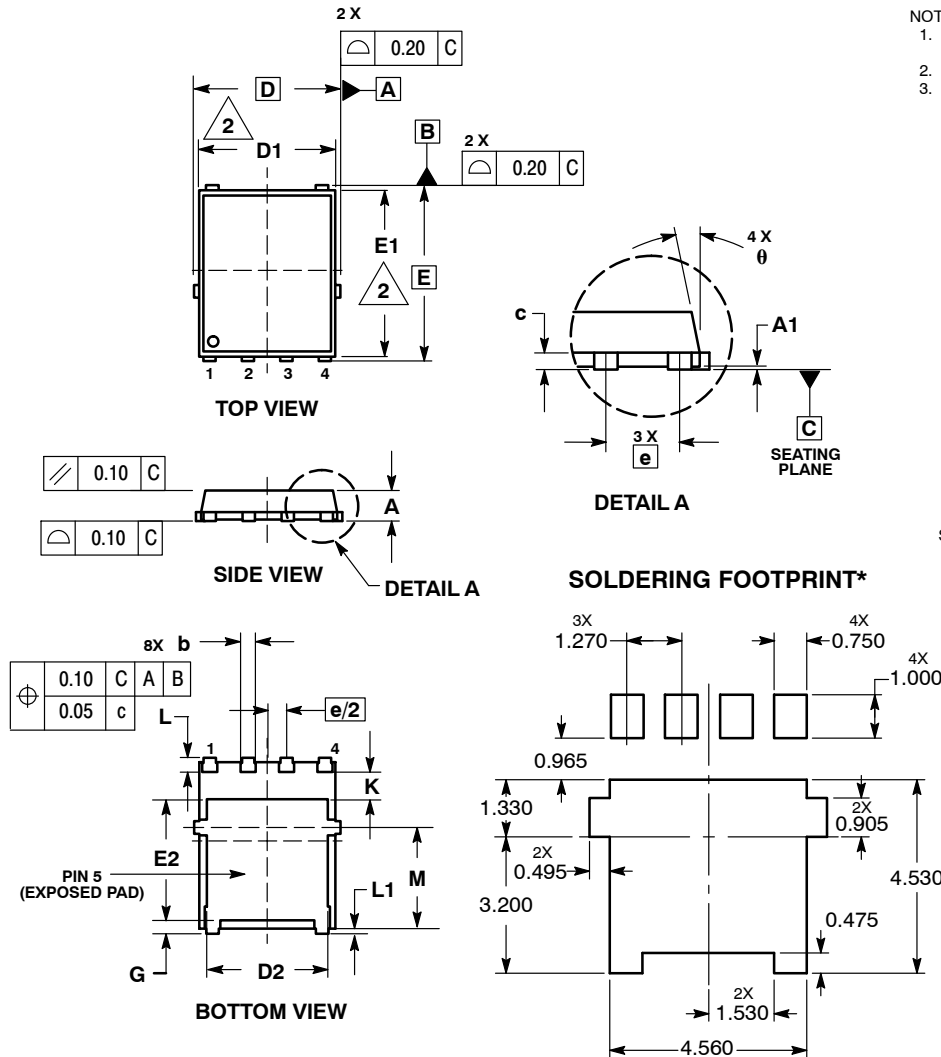


**Figure 14. Avalanche Characteristics**

# NTMFS4851N

## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	---	12°

- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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