

NTMFSC004N08C

Advance Information

Power MOSFET, Single N-Channel, DUAL COOL™, 80 V, 4.0 mΩ, 136 A, PQFN8 5x6



ON Semiconductor®

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Features

- Advanced Dual-Sided Cooled Packaging
- Ultra Low $R_{DS(on)}$ to Minimize Conduction Losses
- MSL1 Robust Packaging Design
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Orring FET/Load Switching
- Synchronous Rectifier
- DC-DC Conversion

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	80	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	136	A
Power Dissipation $R_{\theta JC}$ (Note 2)			
Continuous Drain Current $R_{\theta JA}$ (Note 1, 2)	I_D	86	A
Power Dissipation $R_{\theta JA}$ (Note 1, 2)			
Pulsed Drain Current	I_{DM}	487	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	157	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{AV} = 55$ A, $L = 0.1$ mH)	E_{AS}	152	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	T_L	300	$^\circ\text{C}$

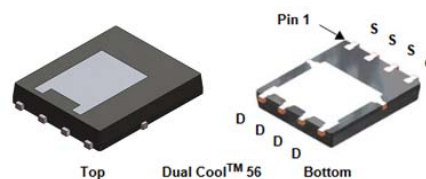
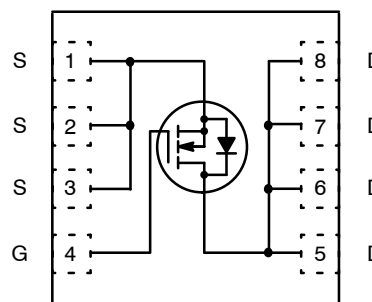
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

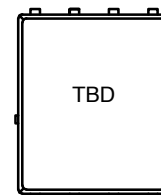
V_{SSS}	$R_{SS(ON)}$ MAX	I_D MAX
80 V	3.8 mΩ @ 10 V	136 A
	7.5 mΩ @ 6 V	

N-Channel MOSFET



PQFN8 5x6
CASE 483BK

MARKING DIAGRAM



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 1)	0.98	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 1)	TBD	

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSC004N08C	TBD	PQFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain – to – Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain – to – Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		0.05		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate – to – Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0	2.9	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		-6.5		mV/°C
Drain – to – Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = \text{TBD A}$		3.1	3.8	m Ω
		$V_{GS} = 6\text{ V}, I_D = \text{TBD A}$		5.0	7.5	
Forward Transconductance	g_{FS}	$V_{DS} = \text{TBD}, I_D = \text{TBD A}$		102		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		1.4		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 40\text{ V}$		2980		pF
Output Capacitance	C_{OSS}			950		
Reverse Transfer Capacitance	C_{RSS}			50		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DS} = 40\text{ V}, I_D = 22\text{ A}$		27.8		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 22\text{ A}$		43.4		
Gate-to-Source Charge	Q_{GS}			15		
Gate-to-Drain Charge	Q_{GD}			7		

SWITCHING CHARACTERISTICS (Note 3)

Turn – On Delay Time	$t_d(ON)$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V},$ $I_D = 45\text{ A}, R_G = 6\ \Omega$		11.7		ns
Rise Time	t_r			11.3		
Turn – Off Delay Time	$t_d(OFF)$			21.1		
Fall Time	t_f			9.55		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 22\text{ A}$	$T_J = 25^\circ\text{C}$	0.8		V
			$T_J = 125^\circ\text{C}$	0.71		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 45\text{ A}$		44		ns
Reverse Recovery Charge	Q_{RR}			12		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

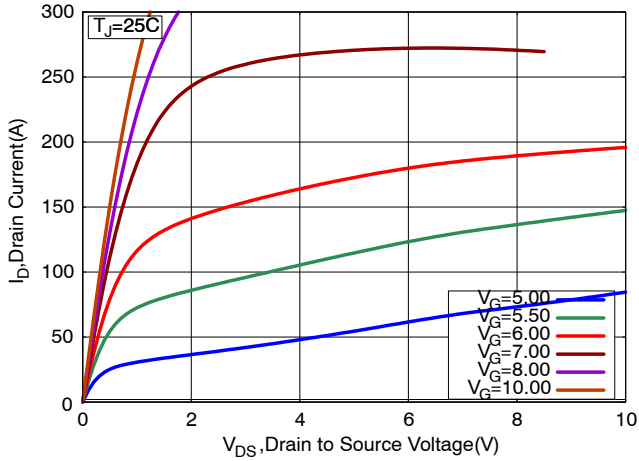


Figure 1. On-Region Characteristics

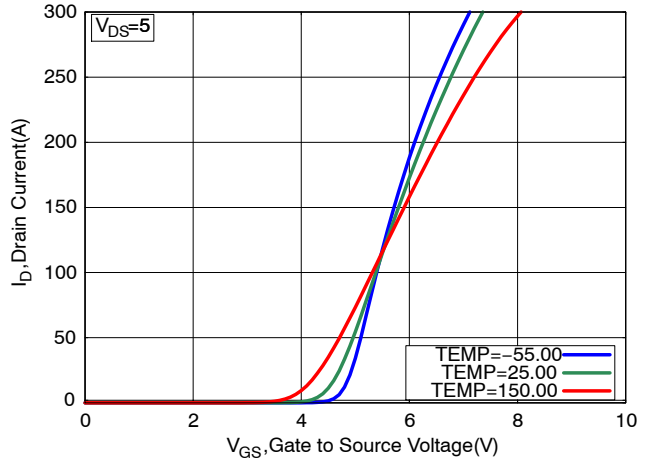


Figure 2. Transfer Characteristics

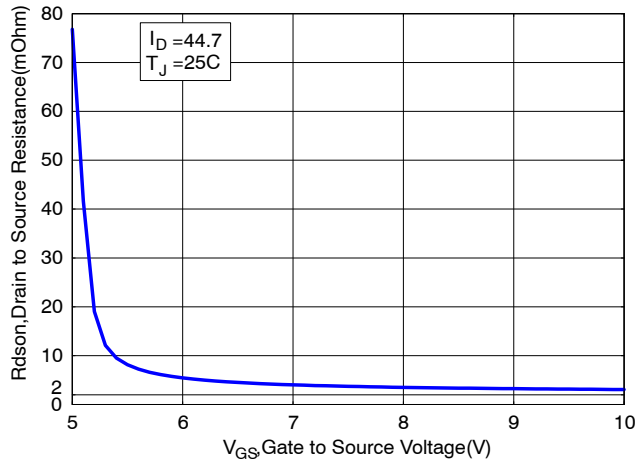


Figure 3. On-Resistance vs. VGS

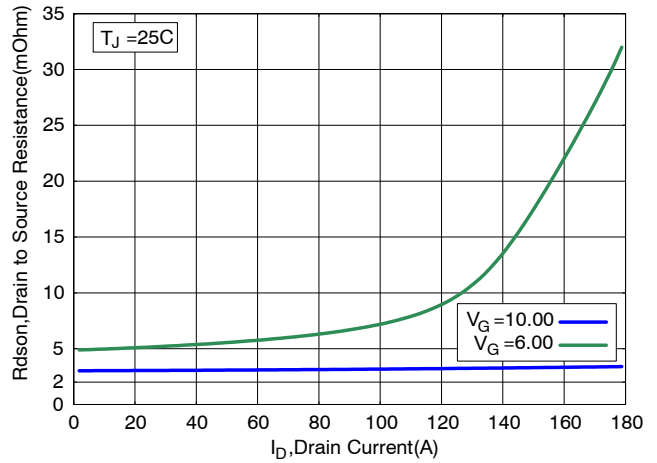


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

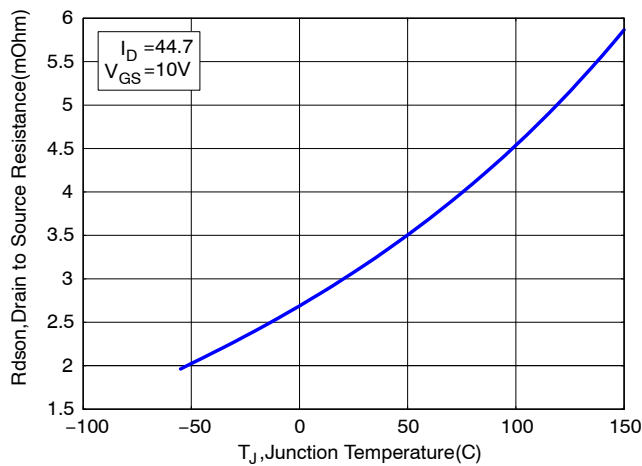


Figure 5. On-Resistance Variation with Temperature

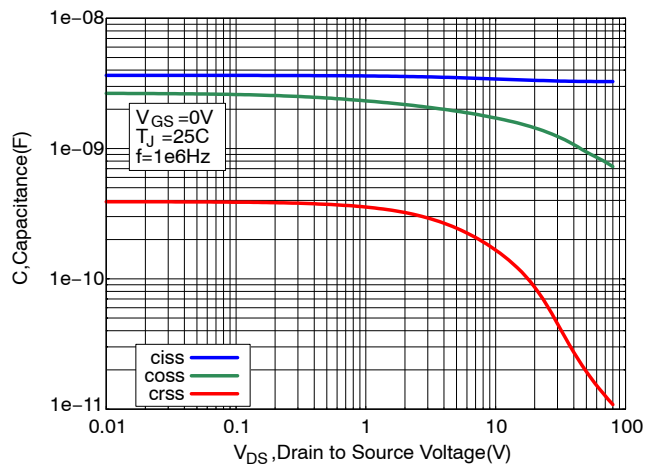


Figure 6. Capacitance Variation

TYPICAL CHARACTERISTICS

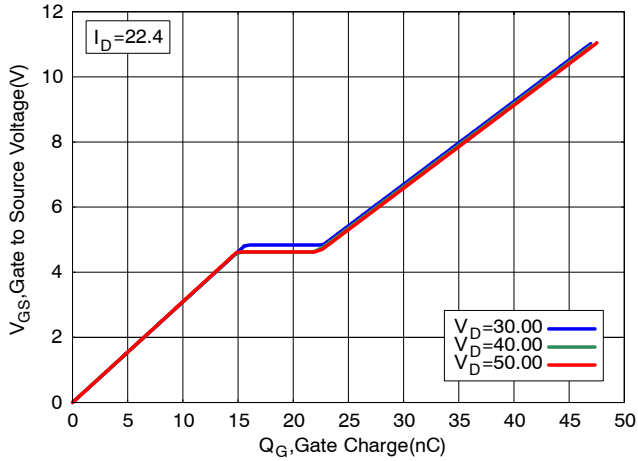


Figure 7. Gate-to-Source Voltage vs. Total Charge

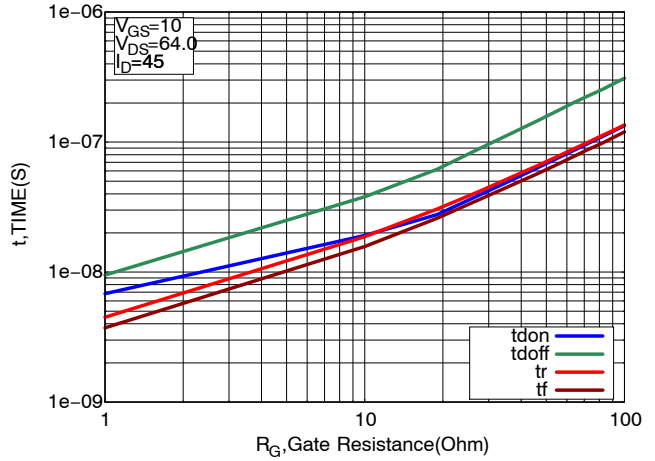


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

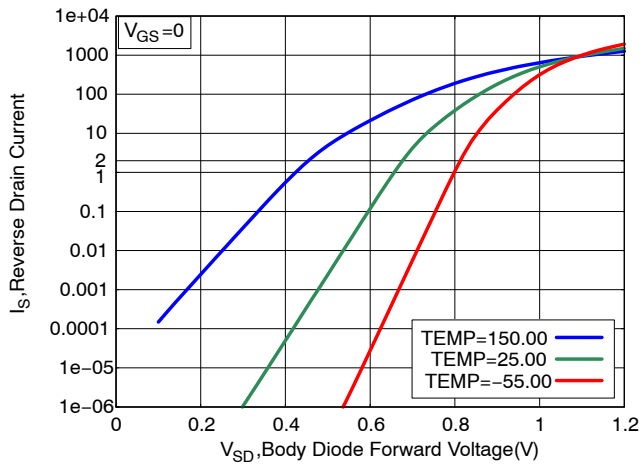


Figure 9. Diode Forward Voltage vs. Current

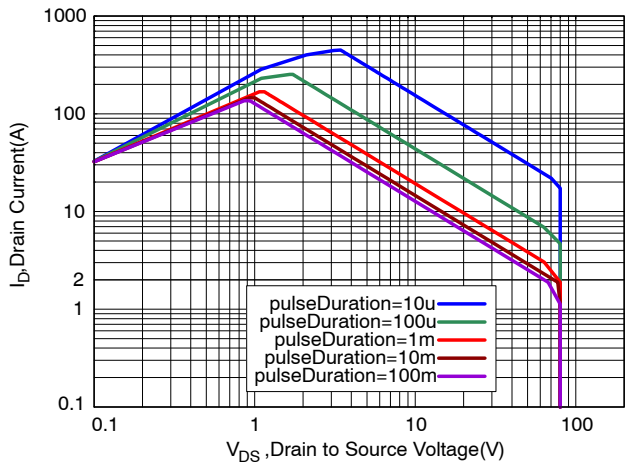


Figure 10. Maximum Rated Forward Biased Safe Operating Area

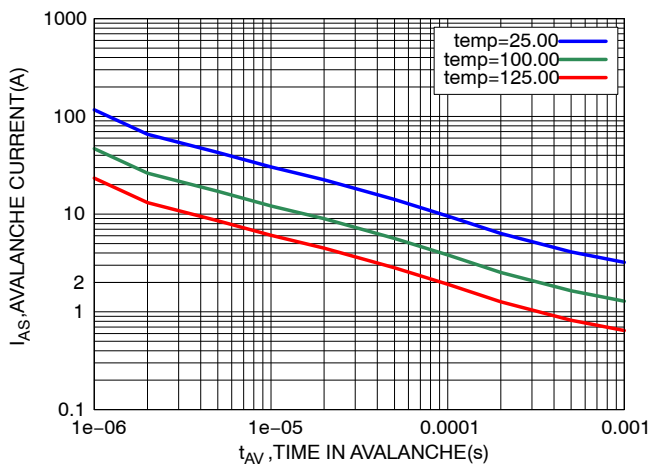


Figure 11. I_{PEAK} vs. Time in Avalanche

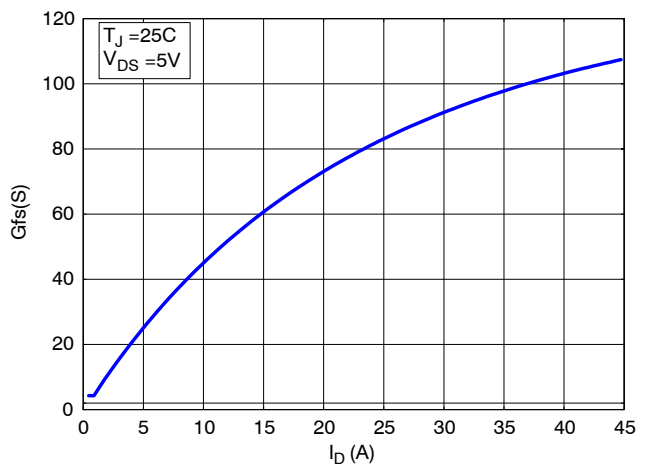


Figure 12. G_{FS} vs. I_D

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TYPICAL CHARACTERISTICS

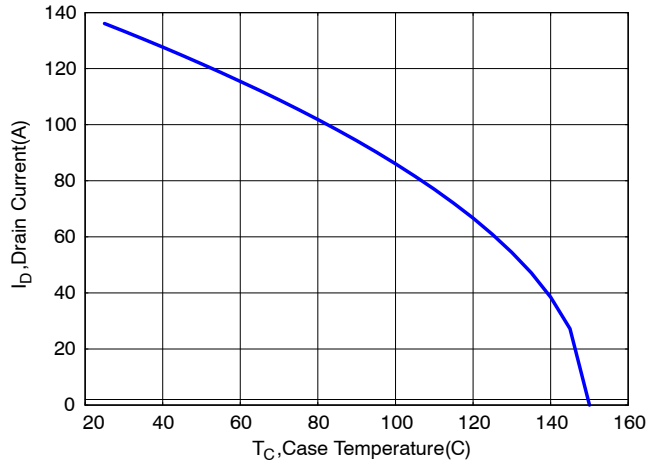


Figure 13. Maximum Current vs. Case Temperature

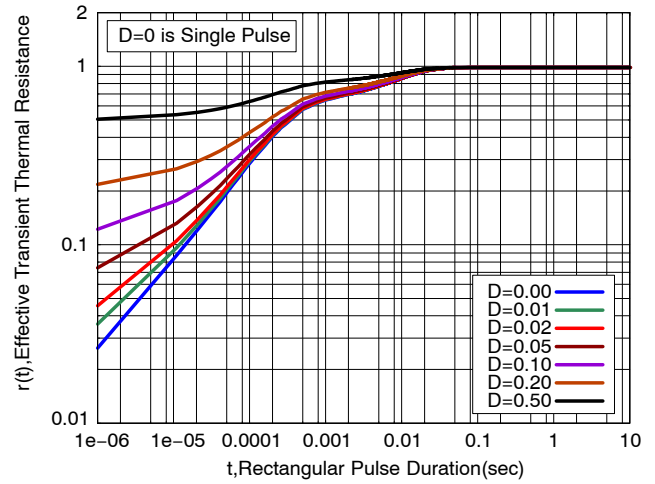



Figure 14. Thermal Response

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