NTMFSC006N12MC

Product Preview

Power MOSFET

120 V, 6.0 mΩ, TBD, Dualcool N−Channel, PQFN8

Features

- Advanced Dual−sided Cooled Packaging
- Ulra Low $R_{DS(on)}$
- MSL1 Robust Packaging Design

Typical Applications

- Primary DC−DC FET
- Synchronous Rectifier
- DC−DC Conversion

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	120	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	TBD	A
Power Dissipation $R_{\theta JC}$ (Note 2)			P_D	TBD	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	TBD	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			P_D	TBD	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	TBD	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	TBD	A
Single Pulse Drain−to−Source Avalanche Energy (I_{AV} = TBD, L = TBD)			E_{AS}	TBD	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	TBD	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	TBD	

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

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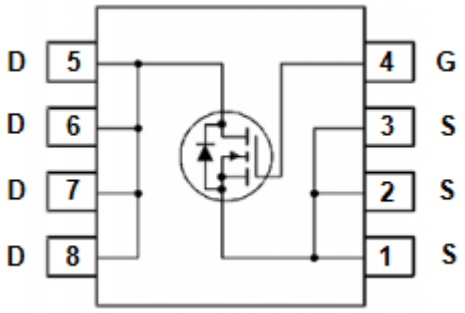
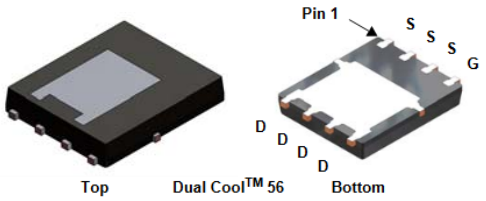
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
120 V	6.0 mΩ @ 10 V	TBD
	TBD @ 6 V	TBD



MARKING DIAGRAM



DUAL COOL 56
PQFN8
CASE 483BK

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFSC006N12MC	PQFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

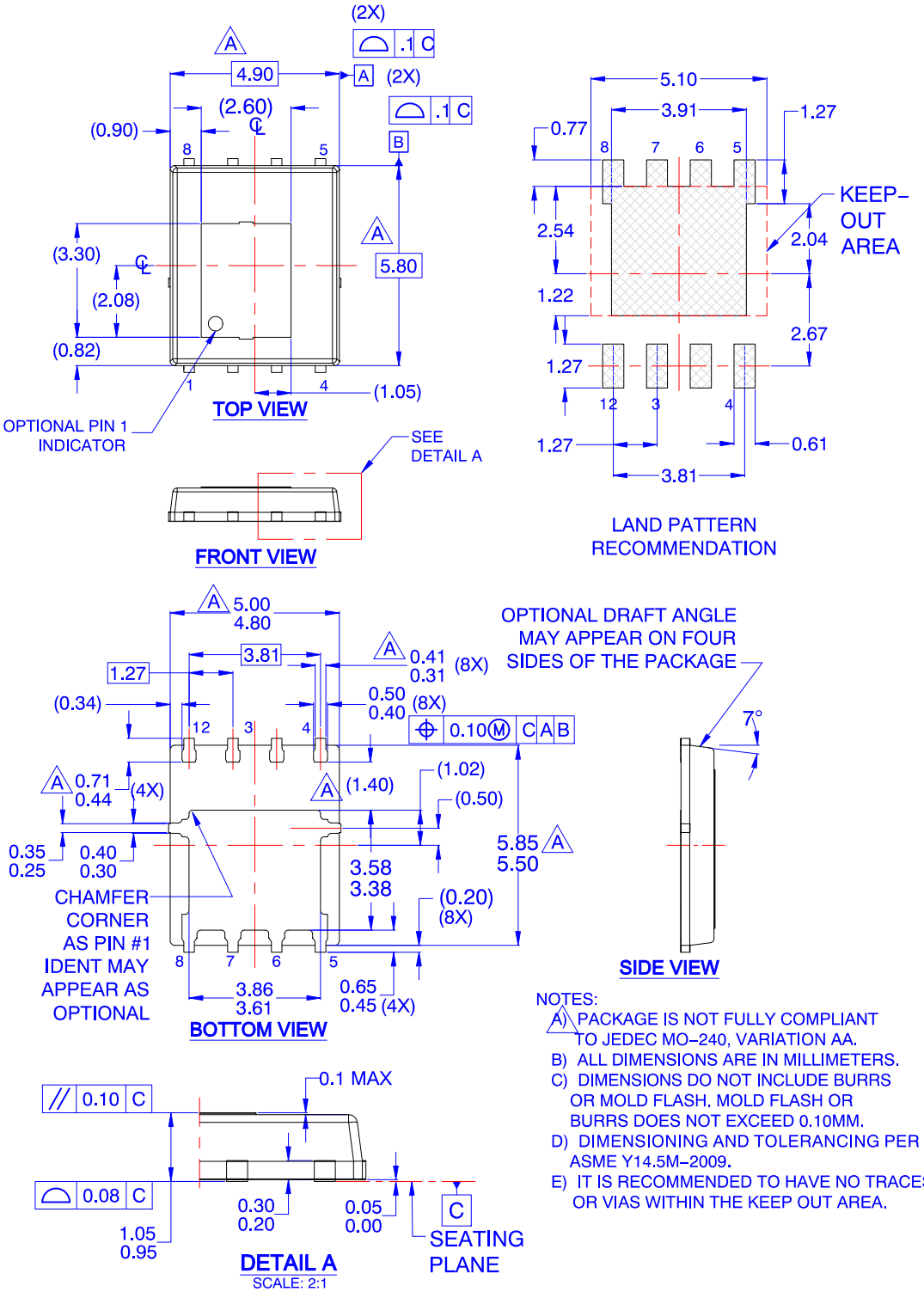
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		120			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			TBD		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V	T_J = 25°C			1	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 250 μA, ref to 25°C			TBD		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = TBD		TBD	6.0	mΩ
		V_{GS} = 6 V	I_D = TBD		TBD	TBD	
Forward Transconductance	g_{FS}	V_{DS} = TBD, I_D = TBD			TBD		S
Gate−Resistance	R_G	T_A = 25°C			TBD		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 60 V			TBD		pF
Output Capacitance	C_{OSS}				TBD		
Reverse Transfer Capacitance	C_{RSS}				TBD		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 6 V, V_{DS} = 60 V, I_D = TBD			TBD		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 60 V, I_D = TBD			42		
Gate−to−Source Charge	Q_{GS}				12		
Gate−to−Drain Charge	Q_{GD}				11		
Plateau Voltage	V_{GP}				TBD		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 60 V, I_D = TBD, R_G = TBD			TBD		ns
Rise Time	t_r				TBD		
Turn−Off Delay Time	$t_{d(OFF)}$				TBD		
Fall Time	t_f				TBD		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = TBD	T_J = 25°C		TBD		V
			T_J = 125°C		TBD		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = TBD			TBD		ns
Reverse Recovery Charge	Q_{RR}				TBD		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 1000 A/μs, I_S = TBD			TBD		ns
Reverse Recovery Charge	Q_{RR}				TBD		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P
CASE 483BK
ISSUE O



NOTES:
A) PACKAGE IS NOT FULLY COMPLIANT TO JEDEC MO–240, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

PUBLICATION ORDERING INFORMATION

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