NTMFSS1D5N06CL

Product Preview

Power MOSFET

60 V, 1.5 mΩ, 235 A, Single N−Channel, Source−Down WDFN9

ON Semiconductor®

www.onsemi.com

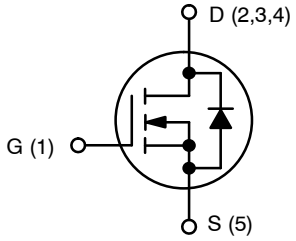
Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen−Free / BFR Free and are RoHS Compliant

Typical Applications

- DC−DC Converters
- Power Load Switch
- Notebook Battery Management

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	1.5 mΩ @ 10 V	235 A
	2.3 mΩ @ 4.5 V	



N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	235	A
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	P_D	167	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	36	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	3.8	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = TBD A, L = TBD mH)			E_{AS}	451	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

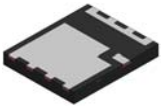
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.9	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 1 in^2 pad size, 2 oz. Cu pad.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



WDFN9 5x6
CASE 511DZ

MARKING DIAGRAM

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Wafer Lot

ORDERING INFORMATION

Device	Package	Shipping†
NTMFSS1D5N06CLT1G	WDFN9 (Pb−Free)	1500 / Tape & Reel
NTMFSS1D5N06CLT3G	WDFN9 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			12.7		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 250 μA, ref to 25°C			−5.76		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A			1.2	1.5	mΩ
		V_{GS} = 4.5 V, I_D = 50 A			1.65	2.3	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 50 A			151		S
Gate Resistance	R_G	T_A = 25°C			TBD		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			6660		pF
Output Capacitance	C_{OSS}				2953		
Reverse Capacitance	C_{RSS}				45		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 30 V, I_D = 50 A			91		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 30 V, I_D = 50 A			41		
Gate−to−Drain Charge	Q_{GD}				10.9		
Gate−to−Source Charge	Q_{GS}				17.1		
Plateau Voltage	V_{GP}				2.9		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 30 V, I_D = 50 A, R_G = 1.0 Ω			19		ns
Rise Time	t_r				51		
Turn−Off Delay Time	$t_{d(OFF)}$				47		
Fall Time	t_f				18		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.78	1.2	V
			T_J = 125°C		0.66		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 100 A/μs, I_S = 50 A			78		ns
Charge Time	t_a				36		
Discharge Time	t_b				42		
Reverse Recovery Charge	Q_{RR}				105		nC

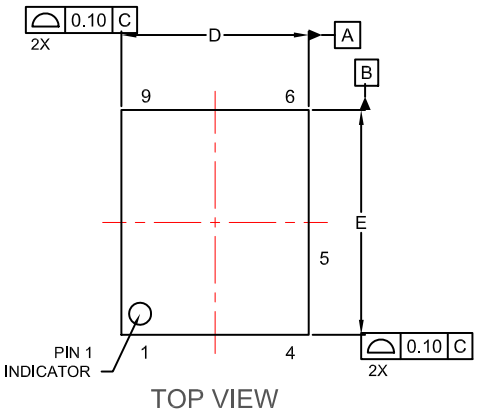
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

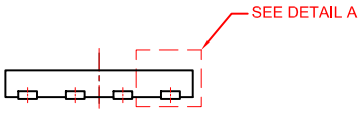
NTMFSS1D5N06CL

PACKAGE DIMENSIONS

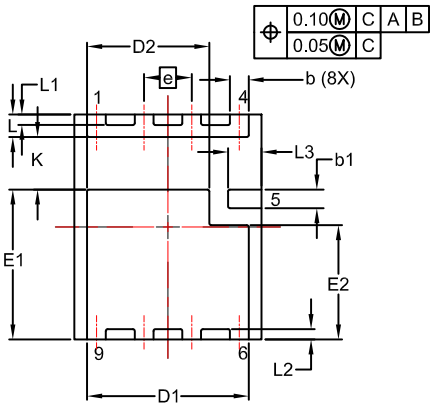
WDFN9 5x6, 1.27P
CASE 511DZ
ISSUE O



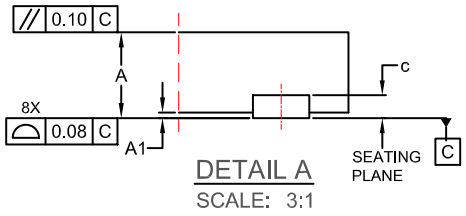
TOP VIEW



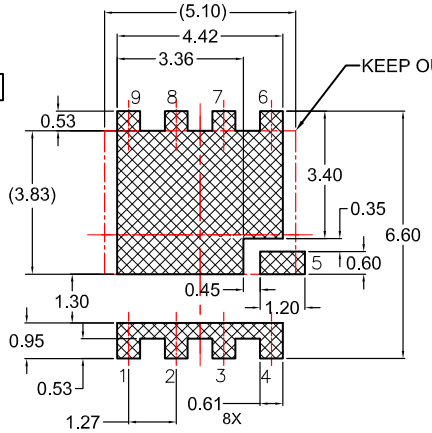
FRONT VIEW



BOTTOM VIEW



DETAIL A
SCALE: 3:1



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.45	0.50	0.55
b1	0.45	0.50	0.55
c	0.17	0.22	0.27
D	4.90	5.00	5.10
D1	4.10	4.30	4.50
D2	3.16	3.26	3.36
E	5.90	6.00	6.10
E1	3.90	4.00	4.10
E2	2.95	3.05	3.15
e	1.27 BSC		
K	1.30	1.40	1.50
L	0.50	0.60	0.70
L1	0.18	0.28	0.38
L2	0.18	0.28	0.38
L3	0.75	0.85	0.95

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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