

NTMKB4893N

Power MOSFET 25 V, 87 A, Single N-Channel, ICEPAK

Features

- Low Package Inductance
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Dual Sided Cooling Capability
- Compatible with SQ Footprint and Outline
- This is a Pb-Free Device

Applications

- CPU Power Delivery
- DC-DC Converters
- Optimized for both Synch FET and Control FET

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	25	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	15.8	A
		$T_A = 70^\circ\text{C}$	12.6	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	2.2	W	
Continuous Drain Current $R_{\theta J-PCB}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	87	A
		$T_A = 70^\circ\text{C}$	48	
Power Dissipation $R_{\theta J-PCB}$ (Note 2)	P_D	65	W	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	$T_C = 25^\circ\text{C}$	64	A
		$T_C = 70^\circ\text{C}$	51	
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	36	W	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	124	A
Current Limited by Package	$T_A = 25^\circ\text{C}$	I_{Dmax}	50	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode) (Note 1)	I_S	42	A	
Drain to Source DV/DT	dV/dt	6.0	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{DD} = 25 \text{ V}, V_{GS} = 10 \text{ V}, I_L = 23 \text{ A}_{pk}, L = 0.3 \text{ mH}, R_G = 25 \Omega$)	E_{AS}	79.4	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	270	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Measured with a T_J of approximately 90°C using 1 oz Cu board.
3. Surface mounted on FR4 board using 1 sq-in pad, 2 oz Cu.



ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
25 V	5.4 m Ω @ 10 V	87 A
	8.6 m Ω @ 4.5 V	

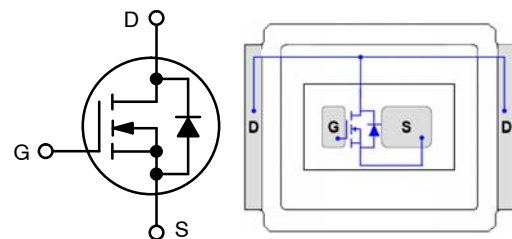


ICEPAK
B1 PAD
CASE 145AD

MARKING DIAGRAM



B4893 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)



N-CHANNEL MOSFET

ORDERING INFORMATION

Device	Package	Shipping†
NTMKB4893NT1G	ICEPAK (Pb-Free)	1500/Tape & Reel
NTMKB4893NT3G	ICEPAK (Pb-Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	3.5	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	58	
Junction-to-Ambient – Steady State (Notes 2 and 3)	$R_{\theta JA}$	20	
Junction-to-PCB (Note 2)	$R_{\theta J-PCB}$	1.0	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			23		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			1.0	μA
					10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.4		2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 17\text{ A}$		4.5	5.4	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 13\text{ A}$		7.2	8.6	
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 10\text{ A}$		40		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		1643		pF
Output Capacitance	C_{oss}			405		
Reverse Transfer Capacitance	C_{rss}			233		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 13\text{ A}$		13.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.8		
Gate-to-Source Charge	Q_{GS}			5.0		
Gate-to-Drain Charge	Q_{GD}			5.1		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 13\text{ A}$		24.9		nC

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 13\text{ A}, R_G = 1.8\ \Omega$		10.7		ns
Rise Time	t_r			23.6		
Turn-Off Delay Time	$t_{d(off)}$			16.6		
Fall Time	t_f			4.2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 13\text{ A}$	$T_J = 25^\circ\text{C}$	0.82	1.0	V
			$T_J = 125^\circ\text{C}$	0.67		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 13\text{ A}$		23.3		ns
Charge Time	t_a			7.6		
Discharge Time	t_b			15.7		
Reverse Recovery Charge	Q_{RR}			16.5		nC

PACKAGE PARASITIC VALUES

Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.6	2.5	Ω
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4. Pulse Test: pulse width = 300 μs , duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

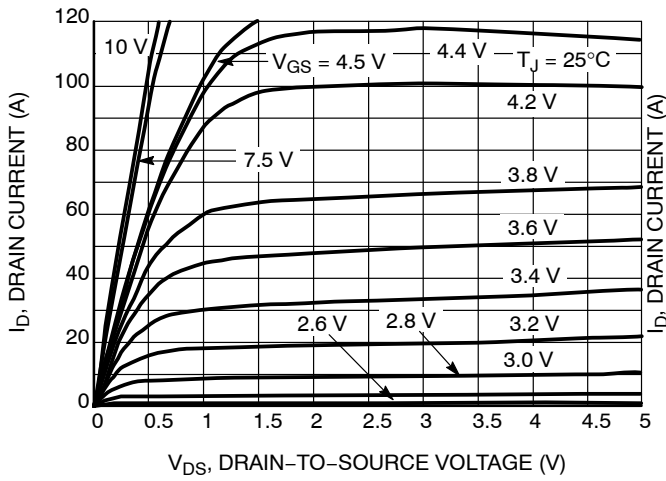


Figure 1. On-Region Characteristics

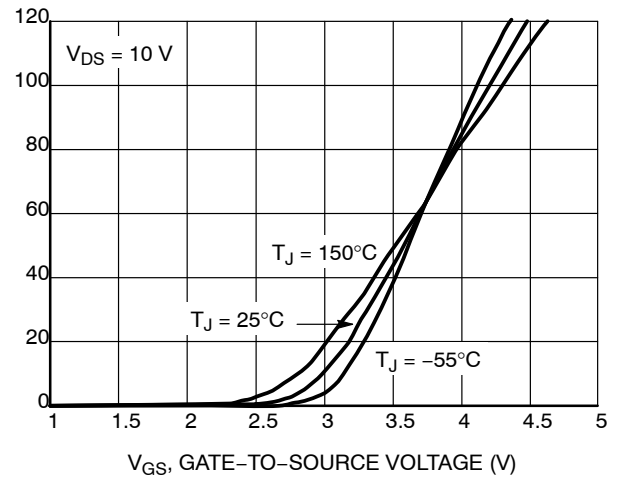


Figure 2. Transfer Characteristics

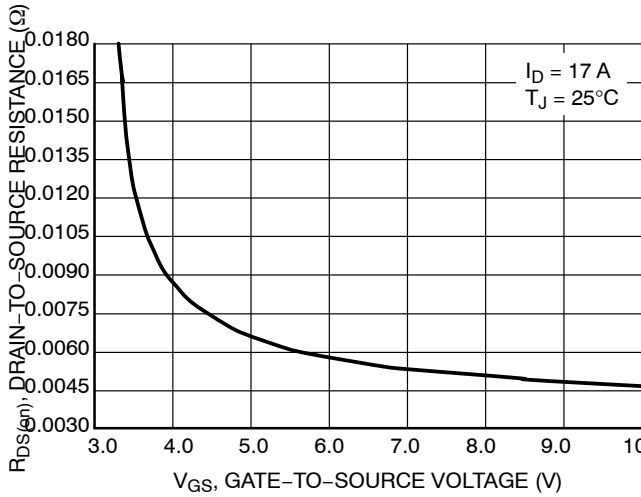


Figure 3. On-Resistance vs. Gate-to-Source Voltage

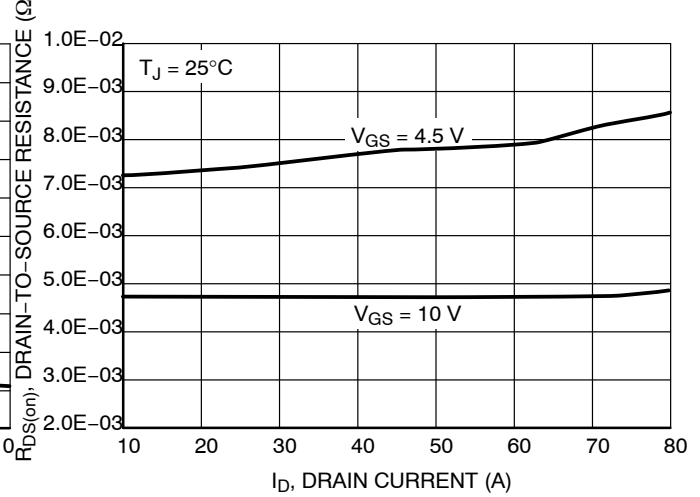


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

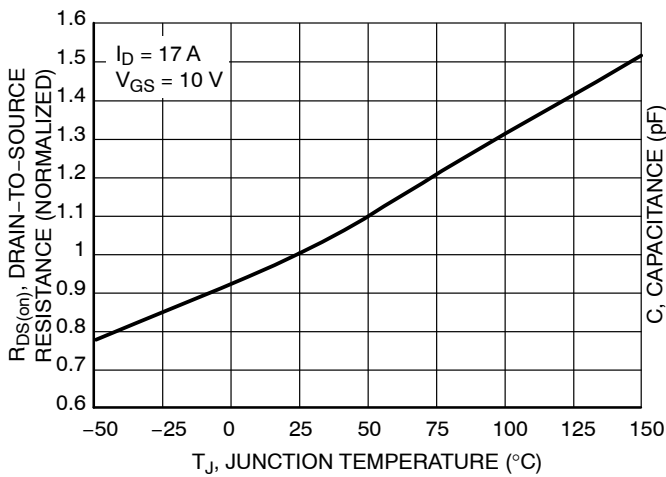


Figure 5. On-Resistance Variation with Temperature

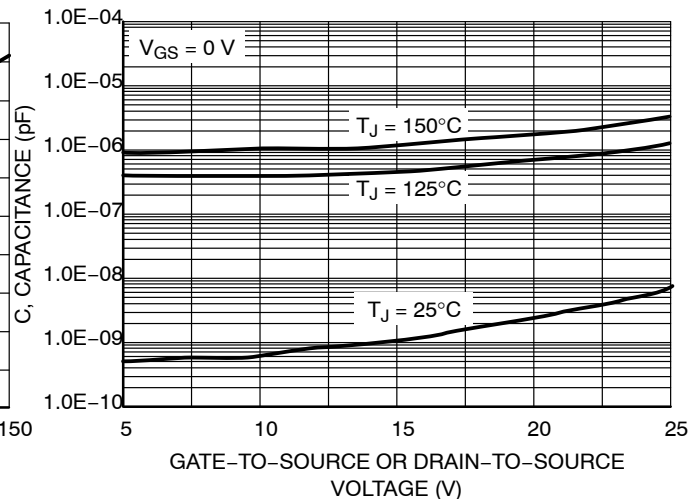


Figure 6. Capacitance Variation

TYPICAL CHARACTERISTICS

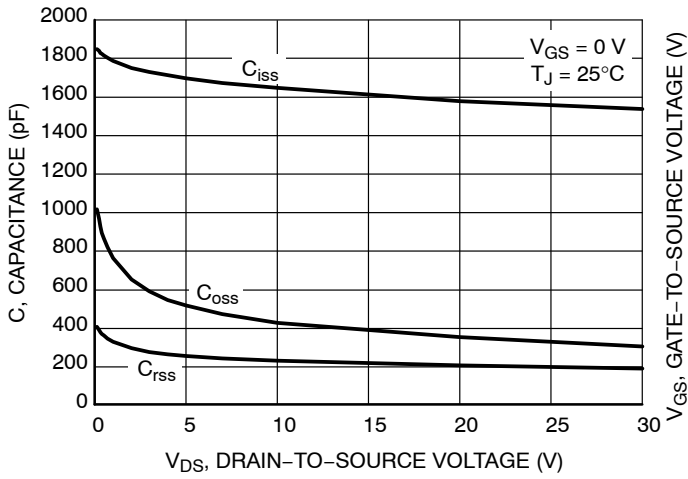


Figure 7. Capacitance Variation

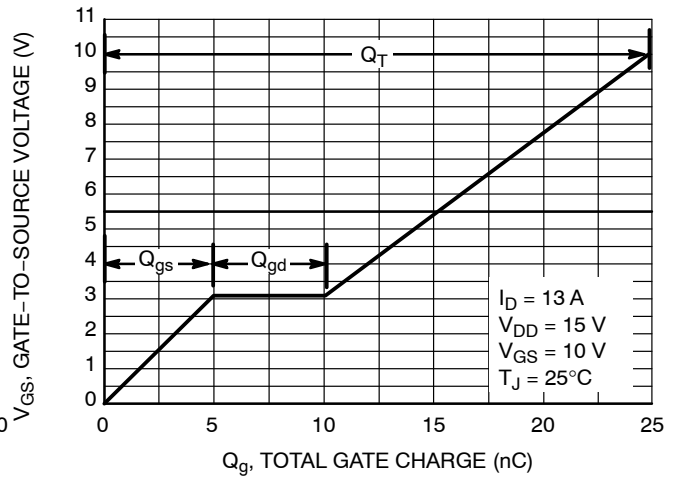


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

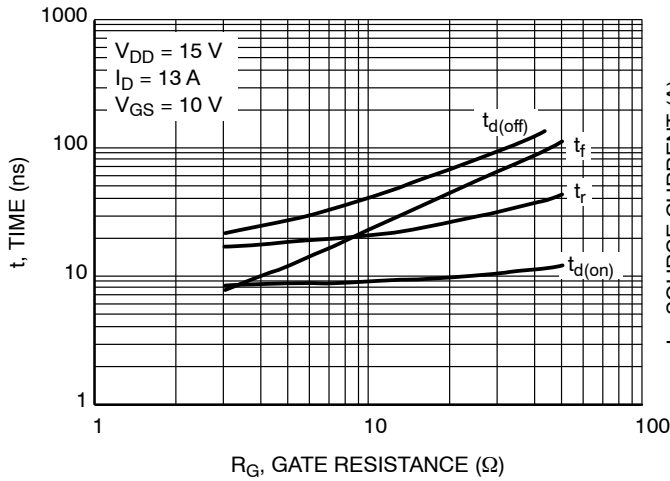


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

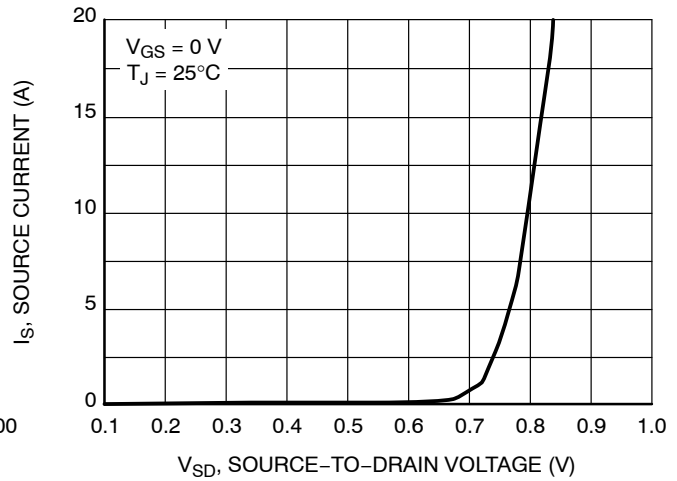


Figure 10. Diode Forward Voltage vs. Current

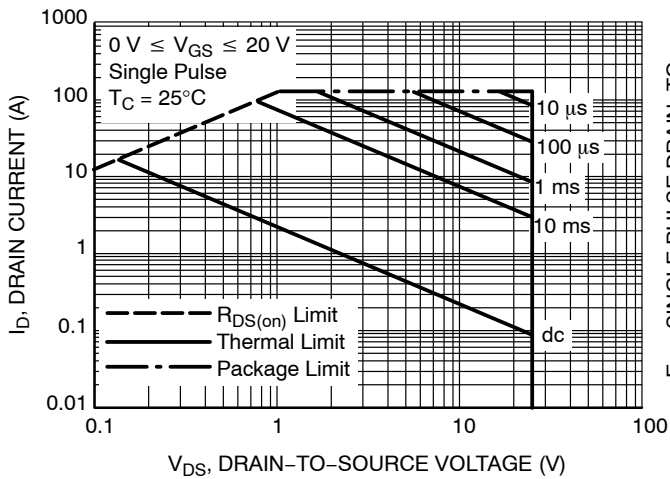


Figure 11. Maximum Rated Forward Biased Safe Operating Area

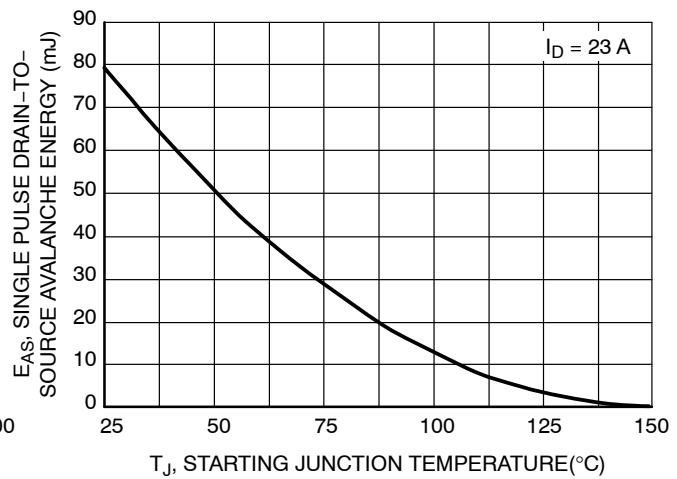
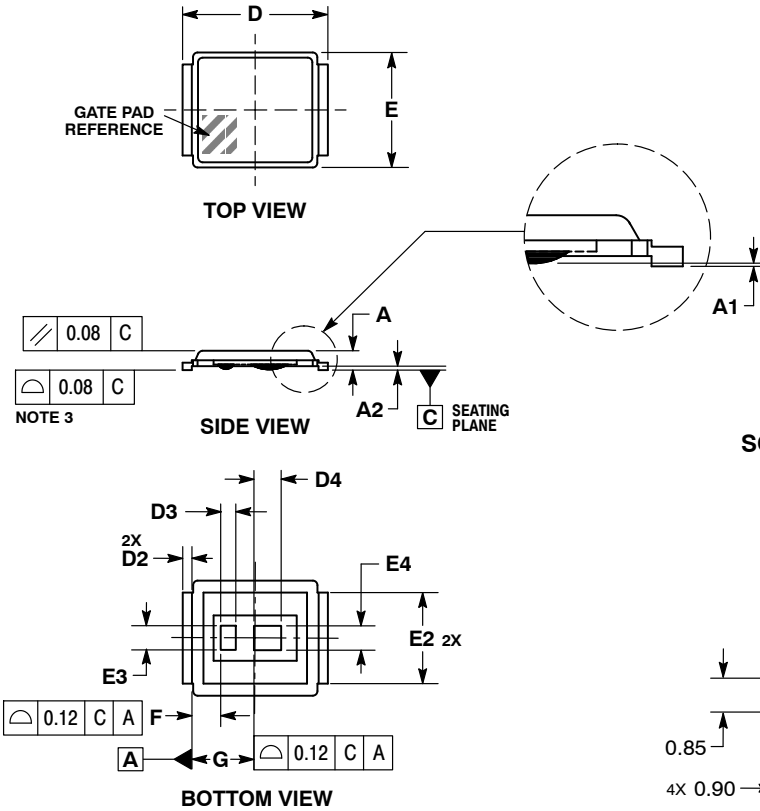


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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PACKAGE DIMENSIONS

ICEPAK 4.8x3.8 – B1 PAD CASE 145AD-01 ISSUE 0

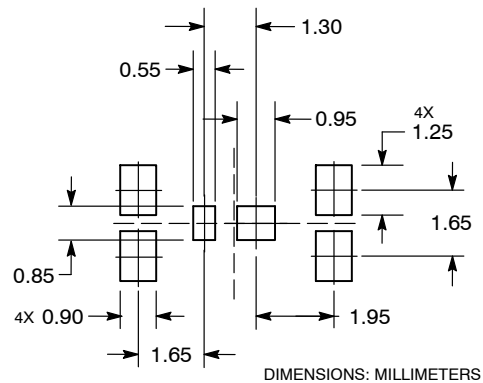


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE FLANGES OF LEADFRAME ONLY.

DIM	MILLIMETERS	
	MIN	MAX
A	0.61	0.68
A1	0.02	0.08
A2	0.08	0.17
D	4.75	4.85
D2	0.35	0.45
D3	0.44	0.48
D4	0.84	0.88
E	3.70	3.95
E2	2.75	2.85
E3	0.74	0.78
E4	0.74	0.78
F	0.97 BSC	
G	2.07 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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