NTMKE4890N

Power MOSFET
30 V, 155 A, Single N−Channel, ICEPAK

Features
- Low Package Inductance
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Dual Sided Cooling Capability
- Compatible with MX Footprint and Outline
- These are Pb−Free Devices

Applications
- CPU Power Delivery
- DC−DC Converters
- Optimized for both Synch FET

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

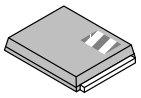
Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	32	A
		T_A = 70°C		25.5	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.8	W
Continuous Drain Current $R_{\theta J-PCB}$ (Note 2)		T_A = 25°C	I_D	155	A
		T_A = 70°C		86	
Power Dissipation $R_{\theta J-PCB}$ (Note 2)		T_A = 25°C	P_D	65	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	192	A
		T_C = 70°C		154	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	100	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	244	A
Current Limited by Package		T_A = 25°C	I_{Dmax}	50	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−40 to 150	°C
Source Current (Body Diode) (Note 1)			I_S	128	A
Drain to Source DV/DT			dV/dt	6.0	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 30 V, V_{GS} = 10 V, I_L = 58 A_{pk}, L = 0.3 mH, R_G = 25 Ω)			E_{AS}	505	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	270	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Surfacemounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Measured with a T_J of approximately 90°C using 1 oz Cu board.
3. Surfacemounted on FR4 board using 1 sq−in pad, 2 oz Cu.

ON Semiconductor®

http://onsemi.com

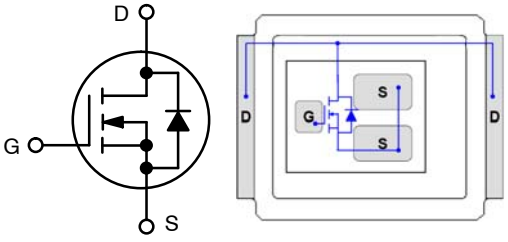
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	1.8 mΩ @ 10 V	155 A
	2.5 mΩ @ 4.5 V	



ICEPAK
E PAD
CASE 145AB

MARKING DIAGRAM

E4890 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)



N−CHANNEL MOSFET

ORDERING INFORMATION

Device	Package	Shipping†
NTMKE4890NT1G	ICEPAK (Pb−Free)	1500/Tape & Reel
NTMKE4890NT3G	ICEPAK (Pb−Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain) (Note 1)	$R_{\theta JC}$	1.25	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	45	
Junction−to−Ambient − Steady State (Notes 2 and 3)	$R_{\theta JA}$	25	
Junction−to−PCB (Note 2)	$R_{\theta J-PCB}$	1.0	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				20		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.4		2.4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.9		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A			1.5	1.8	mΩ
		V_{GS} = 4.5 V, I_D = 30 A			2.1	2.5	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 25 A			120		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 15 V			7100		pF
Output Capacitance	C_{oss}				1360		
Reverse Transfer Capacitance	C_{rss}				690		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 25 A			51.7		nC
Threshold Gate Charge	$Q_{G(TH)}$				6.0		
Gate−to−Source Charge	Q_{GS}				18.8		
Gate−to−Drain Charge	Q_{GD}				18.6		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 25 A			104		nC
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 25 A, R_G = 2.0 Ω			25		ns
Rise Time	t_r				23		
Turn−Off Delay Time	$t_{d(off)}$				42		
Fall Time	t_f				12		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.78	1.0	V
			T_J = 125°C		0.68		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 200 A/μs, I_S = 20 A			41.8		ns
Charge Time	t_a				19.4		
Discharge Time	t_b				22.4		
Reverse Recovery Charge	Q_{RR}				61		nC
PACKAGE PARASITIC VALUES							
Gate Resistance	R_G	T_A = 25°C			0.6	1.5	Ω

4. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

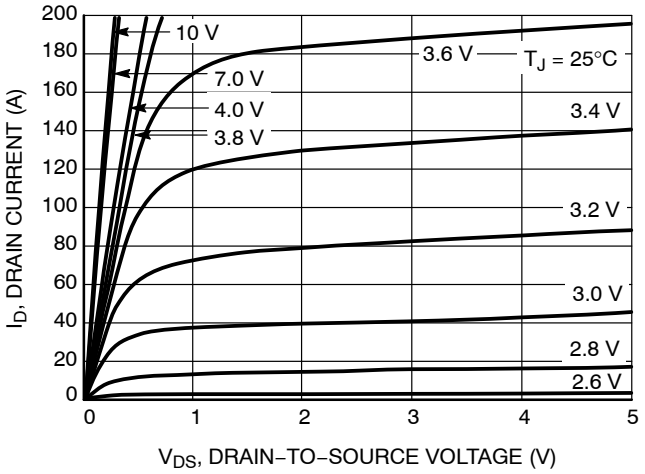


Figure 1. On−Region Characteristics

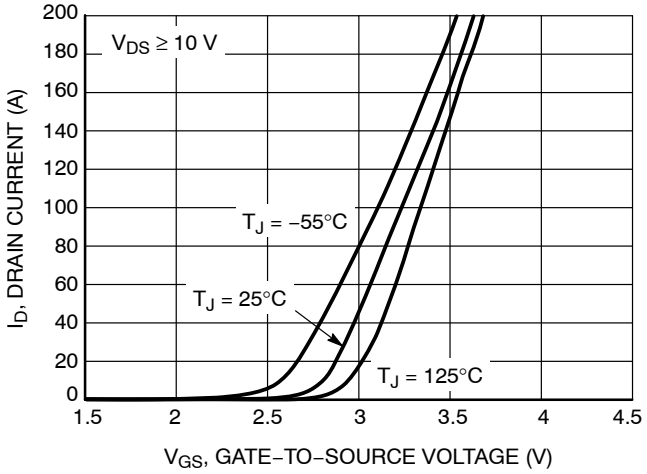


Figure 2. Transfer Characteristics

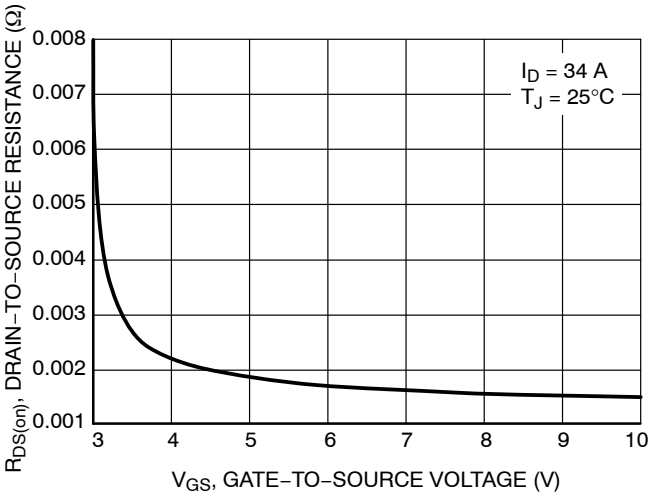


Figure 3. On−Resistance vs. Gate−to−Source Voltage

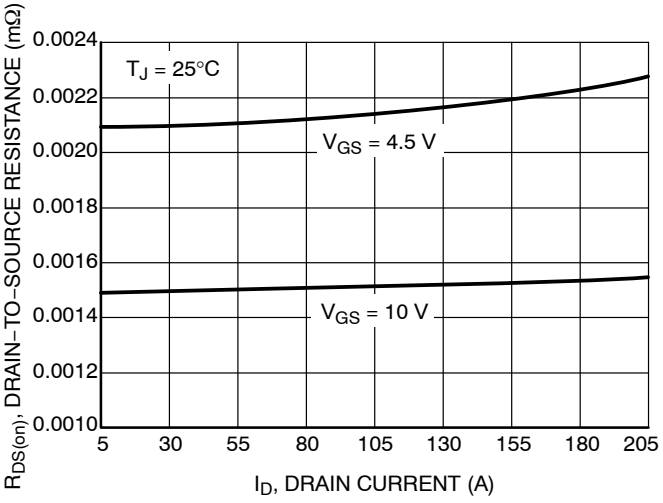


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

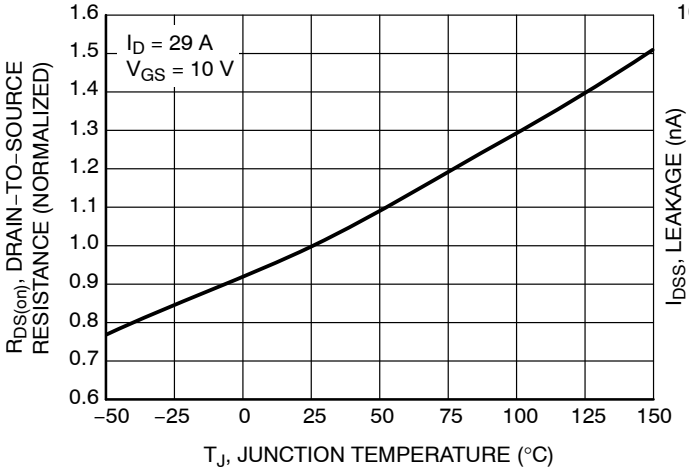


Figure 5. On−Resistance Variation with Temperature

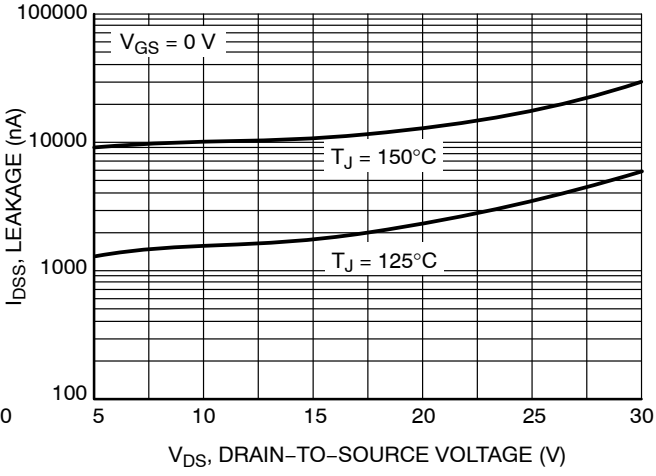


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

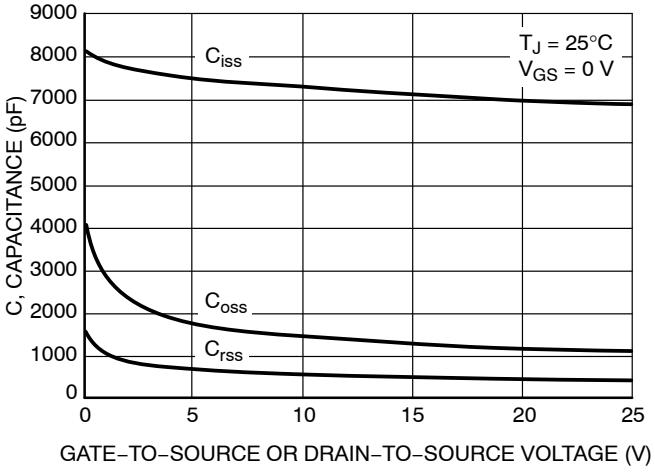


Figure 7. Capacitance Variation

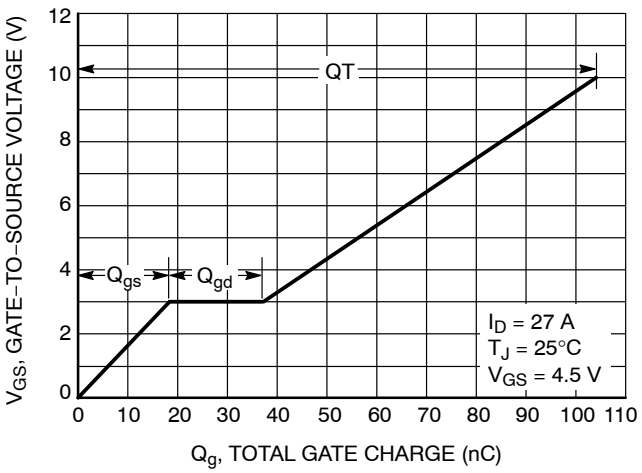


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

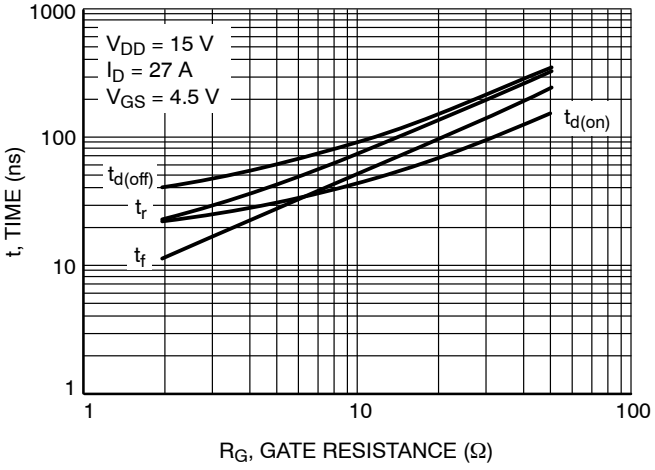


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

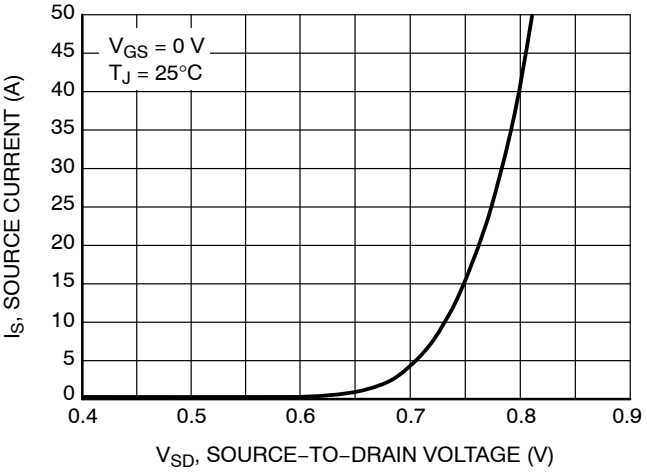


Figure 10. Diode Forward Voltage vs. Current

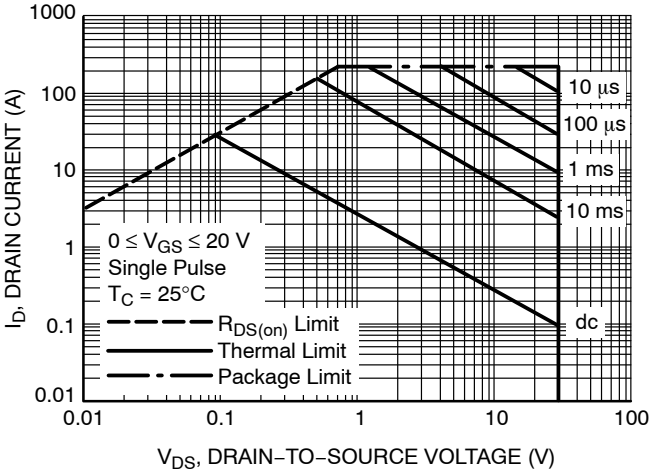


Figure 11. Maximum Rated Forward Biased Safe Operating Area

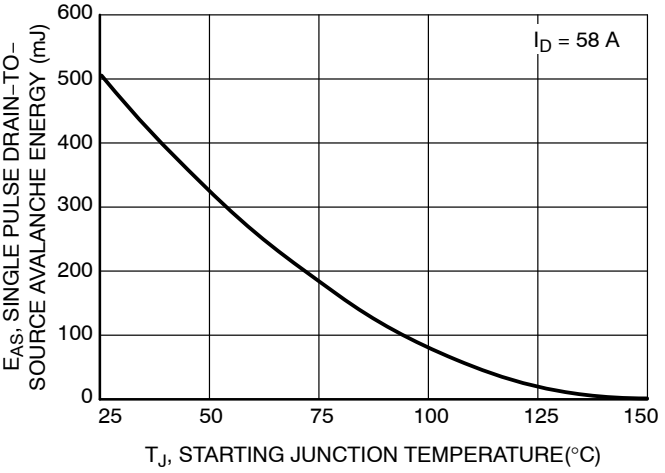


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

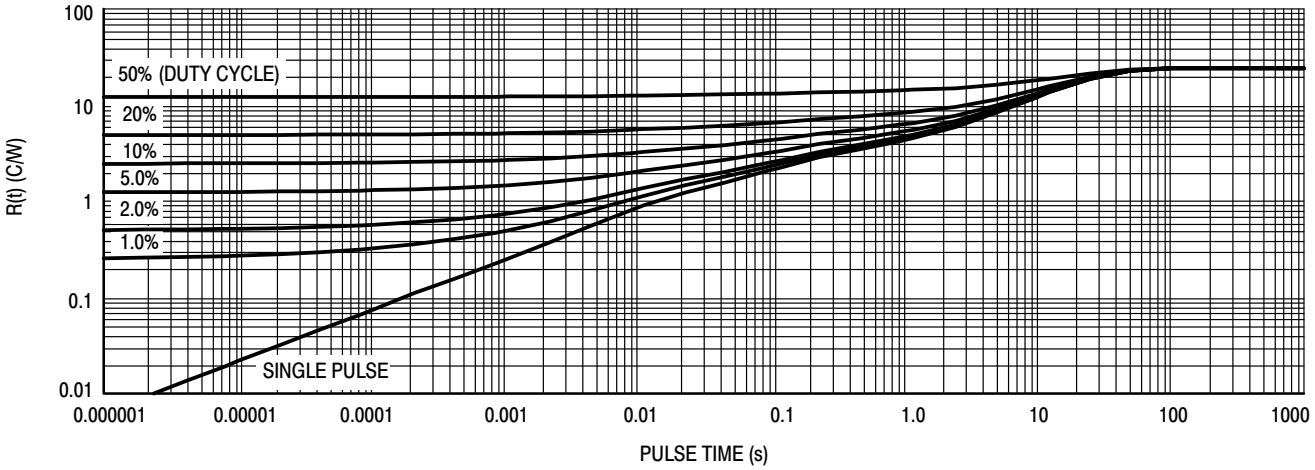
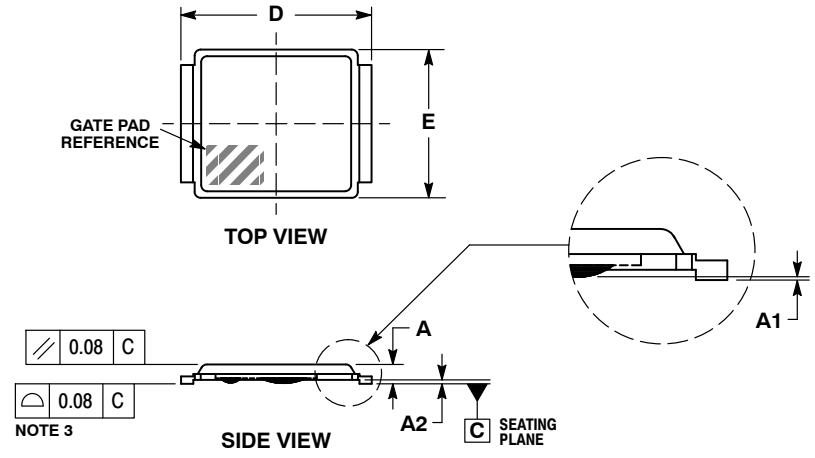


Figure 13. Thermal Impedance

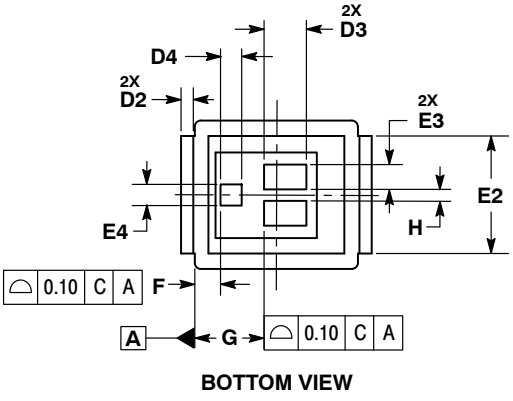
PACKAGE DIMENSIONS

ICEPAK 6.3x4.9 − E PAD
CASE 145AB−01
ISSUE O

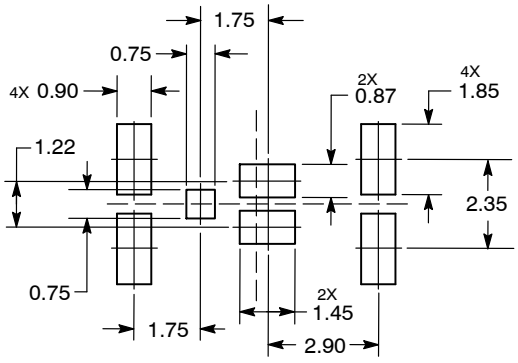


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE FLANGES OF LEADFRAME ONLY.

	MILLIMETERS	
DIM	MIN	MAX
A	0.61	0.68
A1	0.02	0.08
A2	0.08	0.17
D	6.25	6.35
D2	0.35	0.45
D3	1.38	1.42
D4	0.68	0.72
E	4.80	5.05
E2	3.85	3.95
E3	0.80	0.84
E4	0.68	0.72
F	0.94 BSC	
G	2.54 BSC	
H	0.38	0.42



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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