

NTMTS002N08MC

Product Preview

Power MOSFET

80 V, 2 mΩ, 229 A, Single N-Channel, PQFN88

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	80	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	229	A
Power Dissipation $R_{\theta JC}$ (Note 2)			
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	29	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			
Pulsed Drain Current	I_{DM}	3577	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 29\text{ A}, L = 3\text{ mH}$)	E_{AS}	1261.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{\theta JC}$	0.6	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	38	$^\circ\text{C}/\text{W}$

1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

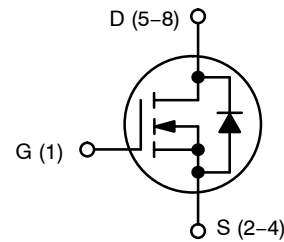
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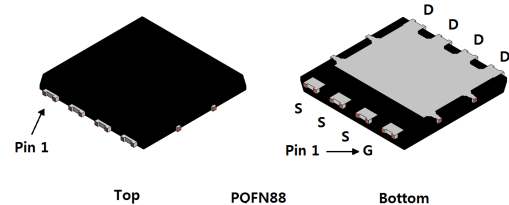
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	2 mΩ @ 10 V	229 A
	5.1 mΩ @ 6 V	

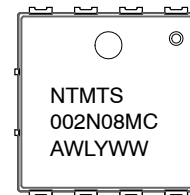


N-CHANNEL MOSFET



POWER 88
CASE 507AP

MARKING DIAGRAM



NTMTS002N08MC = Device Code
 A = Assembly Location
 WL = 2-digit Wafer Lot Code
 Y = Year Code
 WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMTS002N08MC

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		68		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 540\ \mu\text{A}$	2.0	2.7	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 540\ \mu\text{A}$, ref to 25°C		-7.9		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 90\text{ A}$		1.3	2.0	m Ω
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 6\text{ V}, I_D = 48\text{ A}$		1.8	5.1	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 90\text{ A}$		214		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		0.8		Ω

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 40\text{ V}$		6350	8900	pF
Output Capacitance	C_{OSS}			2100	3000	
Reverse Transfer Capacitance	C_{RSS}			93	130	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 90\text{ A}$		89	125	nC
Threshold Gate Charge	$Q_{G(TH)}$			16	22	
Gate-to-Source Charge	Q_{GS}			25		
Gate-to-Drain Charge	Q_{GD}			19		
Output Charge	Q_{OSS}			117		
Sync Charge	Q_{sync}			72		
Plateau Voltage	$V_{plateau}$			4		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 90\text{ A}, R_G = 6\ \Omega$		26		ns
Rise Time	t_r			20		
Turn-Off Delay Time	$t_{d(OFF)}$			65		
Fall Time	t_f			29		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 90\text{ A}$		0.8	1.3	
Reverse Recovery Time	t_{RR}	$I_F = 45\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		34	54	ns
Reverse Recovery Charge	Q_{RR}			71	114	
Reverse Recovery Time	t_{RR}	$I_F = 45\text{ A}, di/dt = 1000\text{ A}/\mu\text{s}$		27	43	nC
Reverse Recovery Charge	Q_{RR}			177	283	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

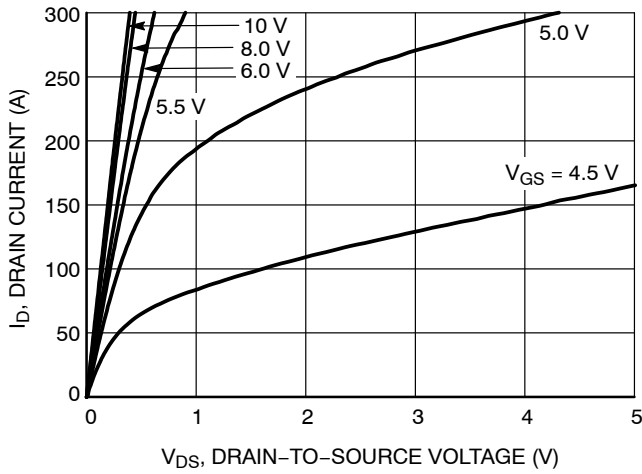


Figure 1. On-Region Characteristics

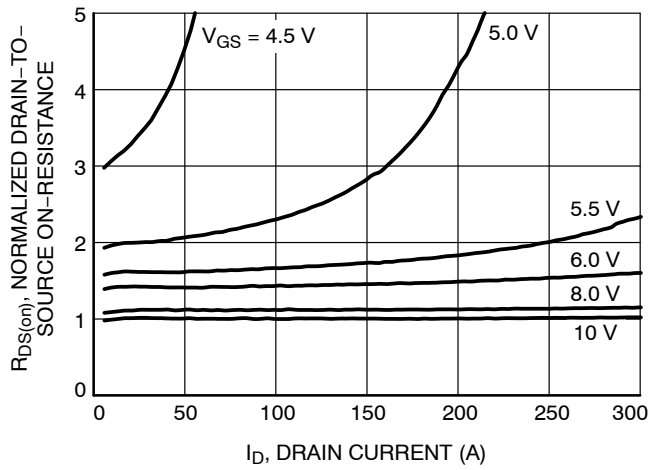


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

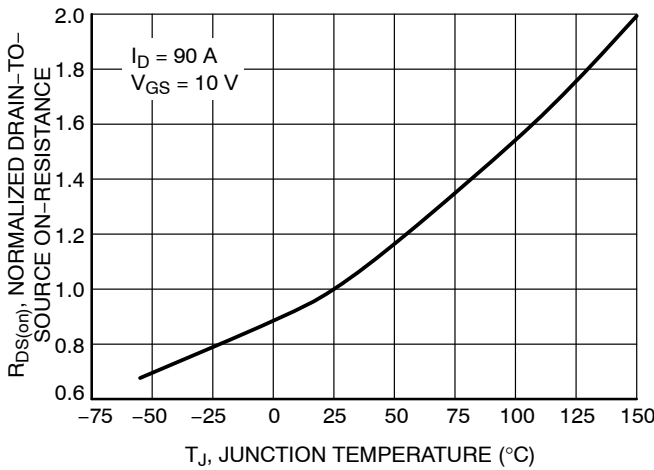


Figure 3. Normalized On Resistance vs. Junction Temperature

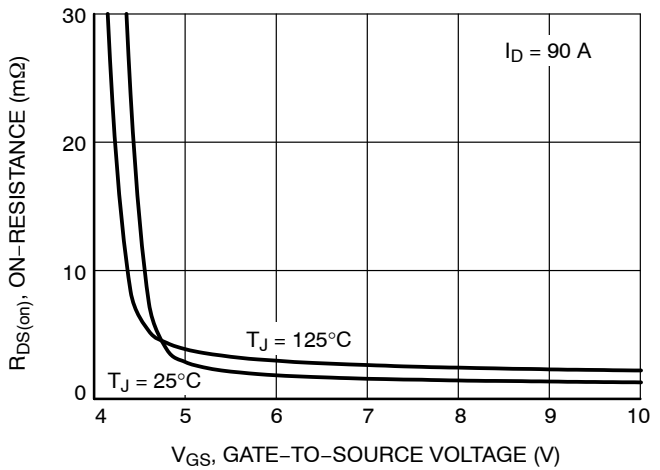


Figure 4. On-Resistance vs. Gate-to-Source Voltage

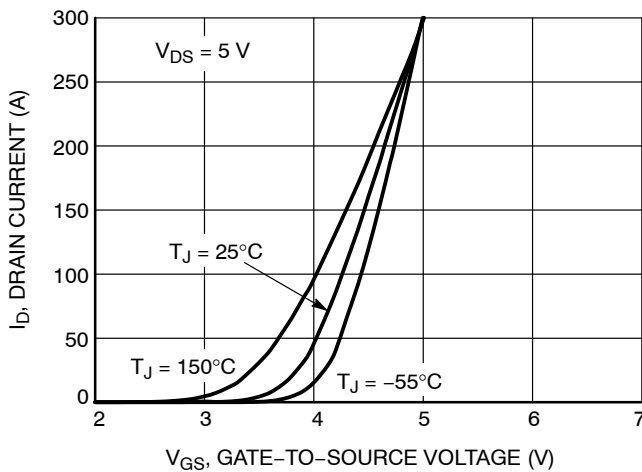


Figure 5. Transfer Characteristics

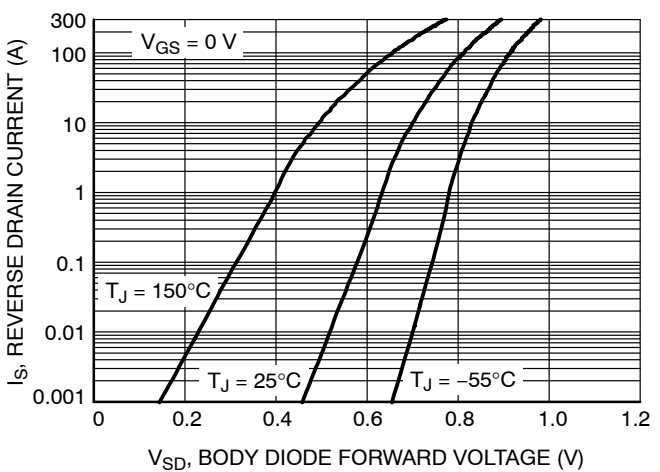


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

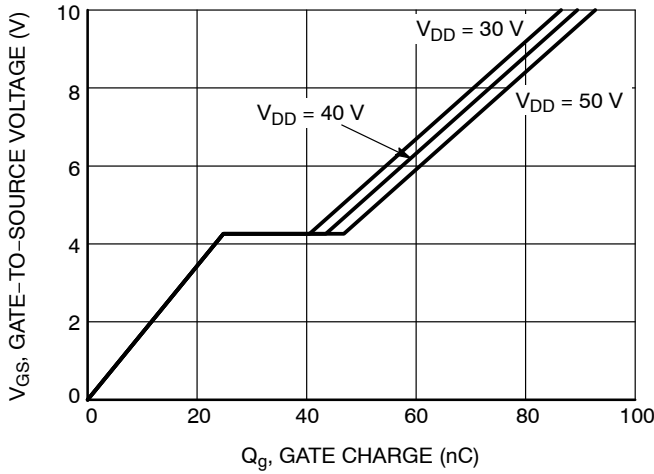


Figure 7. Gate Charge Characteristics

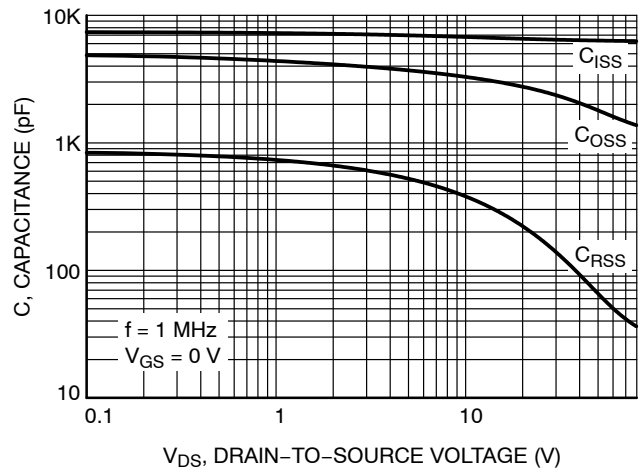


Figure 8. Capacitance vs. Drain-to-Source Voltage

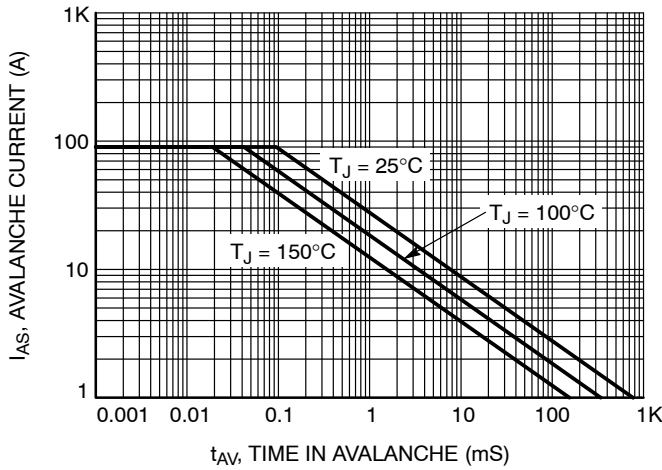


Figure 9. Unclamped Inductive Switching Capability

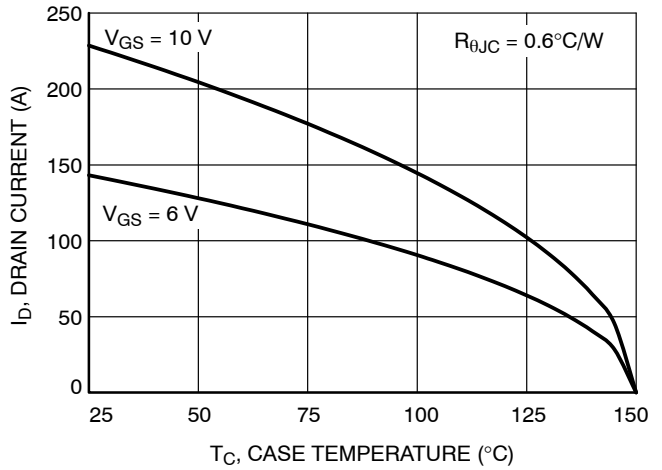


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

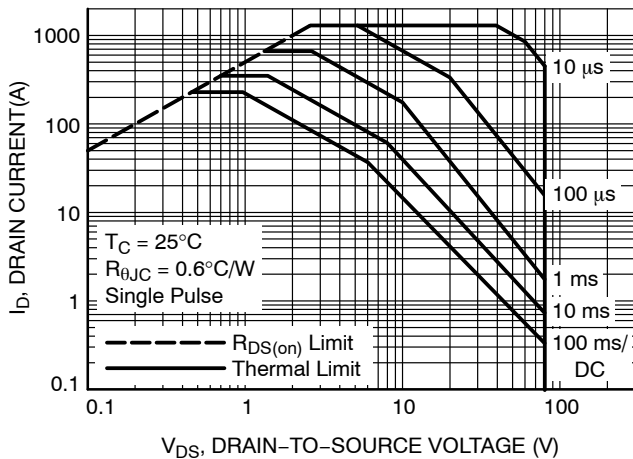


Figure 11. Forward Biased Safe Operating Area

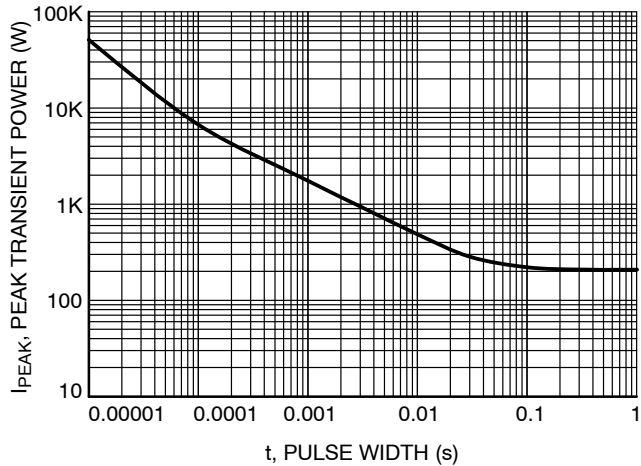


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

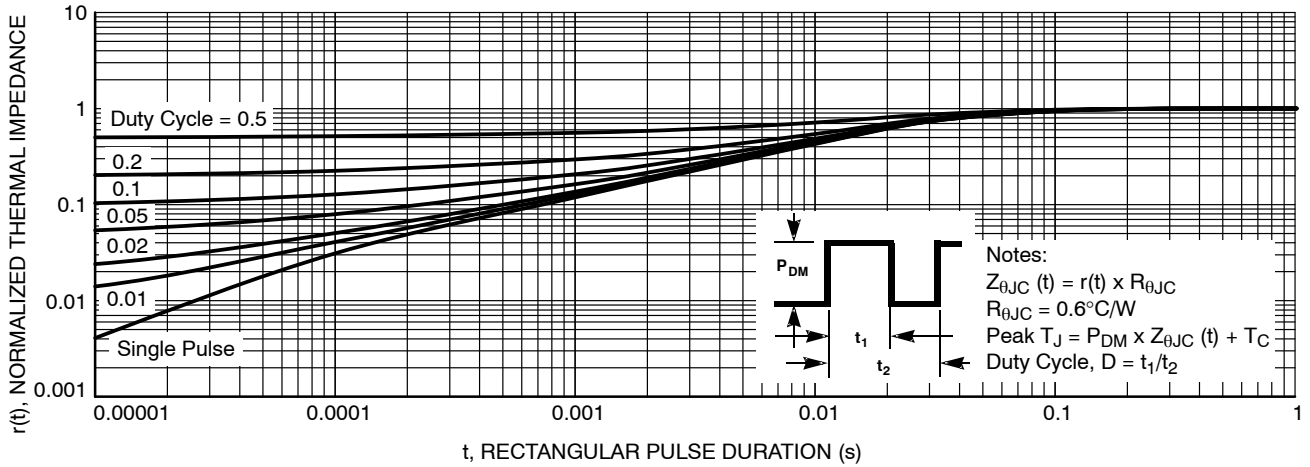


Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

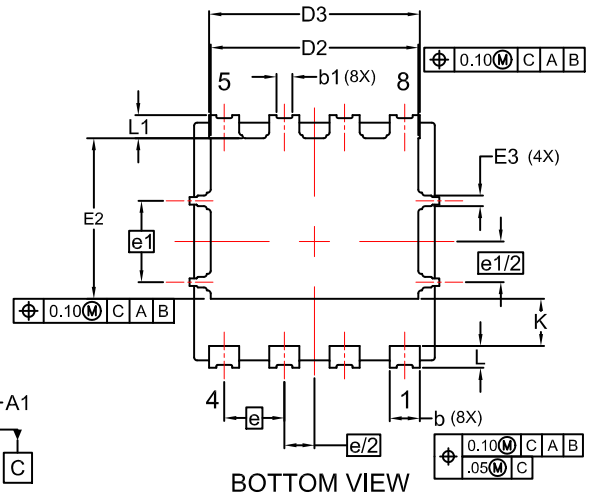
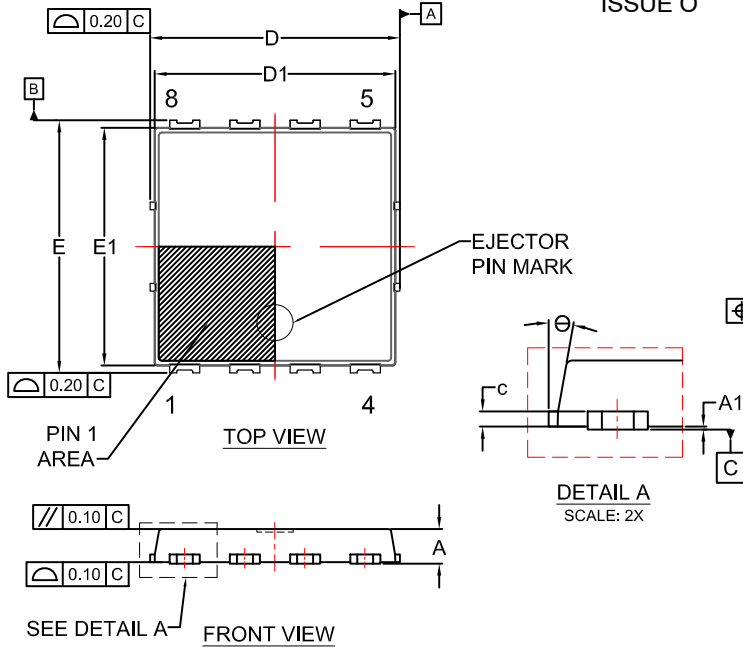
Device	Marking	Package	Shipping [†]
NTMTS002N08MC	NTMTS 002N08MC	POWER 88 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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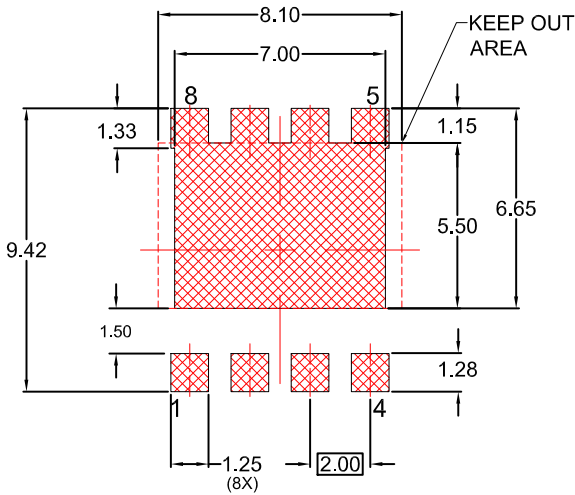
PACKAGE DIMENSIONS

DFNW8 8.3x8.4, 2P
CASE 507AP
ISSUE O




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS.
"A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	--	0.05
b	0.90	1.00	1.10
b1	0.43	0.53	0.63
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
θ	0°	--	12°

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