

MOSFET – Power, N-Channel, SUPERFET III, FRFET

650 V, 20 A, 190 mΩ



ON Semiconductor®

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NTPF190N65S3HF

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

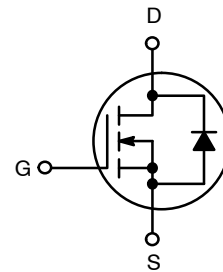
Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 152\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 34\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 316\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

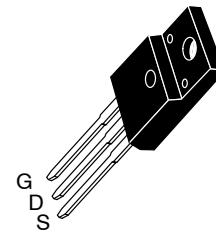
Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter

V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	190 mΩ @ 10 V	20 A

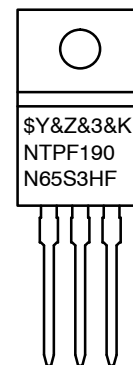


POWER MOSFET



TO-220 FULLPAK
CASE 221D

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
 &Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 NTPF190N65S3HF = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NTPF190N65S3HF

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	- DC	±30
		- AC (f > 1 Hz)	±30
I _D	Drain Current	- Continuous (T _C = 25°C)	20*
		- Continuous (T _C = 100°C)	12.7*
I _{DM}	Drain Current	- Pulsed (Note 1)	50*
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	220	mJ
I _{AS}	Avalanche Current (Note 2)	3.7	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	0.36	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P _D	Power Dissipation	(T _C = 25°C)	36
		- Derate Above 25°C	0.29
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. I_{AS} = 3.7 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 10 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	3.5	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTPF190N65S3HF	NTPF190N65S3HF	TO-220 FULLPACK	Tube	N/A	N/A	50 Units

NTPF190N65S3HF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C		0.65		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V			10	μA
		V _{DS} = 520 V, T _C = 125°C		65		
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.43 mA	3.0		5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 10 A		152	190	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 10 A		11		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz		1610		pF
C _{oss}	Output Capacitance			30		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		316		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		59		pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 10 A, V _{GS} = 10 V (Note 4)		34		nC
Q _{gs}	Gate to Source Gate Charge			11		nC
Q _{gd}	Gate to Drain "Miller" Charge			13		nC
ESR	Equivalent Series Resistance	f = 1 MHz		6.8		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 10 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 4)		19		ns
t _r	Turn-On Rise Time			19		ns
t _{d(off)}	Turn-Off Delay Time			58		ns
t _f	Turn-Off Fall Time			14		ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current			20		A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current			50		A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 10 A			1.3	V
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 10 A, dI _F /dt = 100 A/μs		80		ns
Q _{rr}	Reverse Recovery Charge			264		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

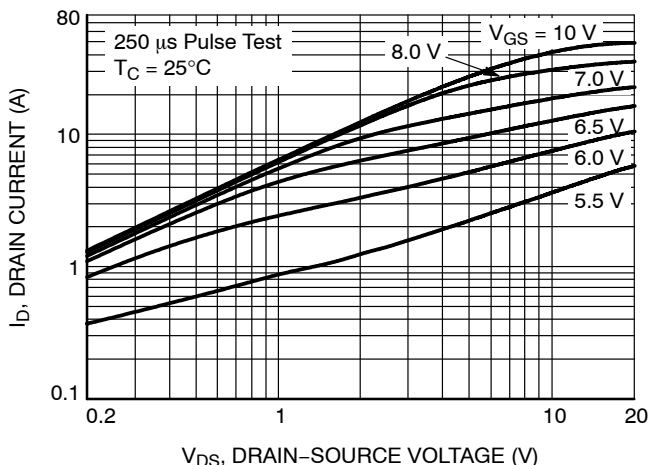


Figure 1. On-Region Characteristics

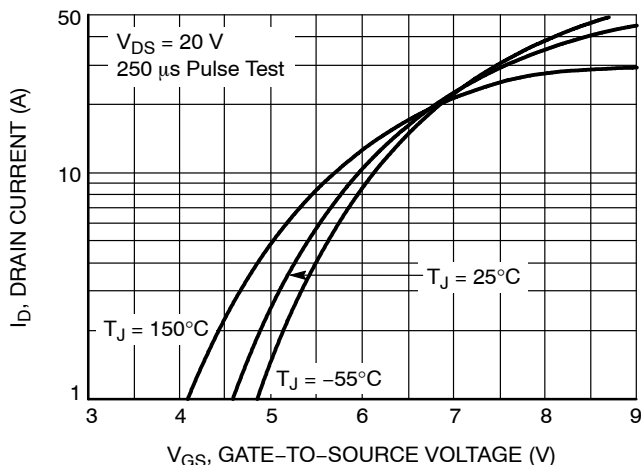


Figure 2. Transfer Characteristics

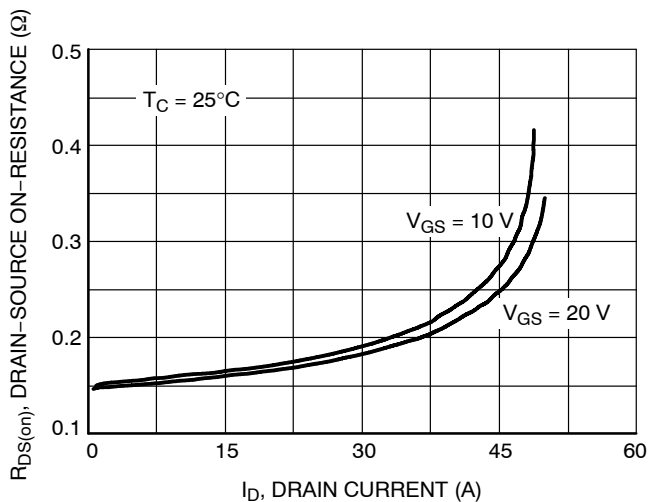


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

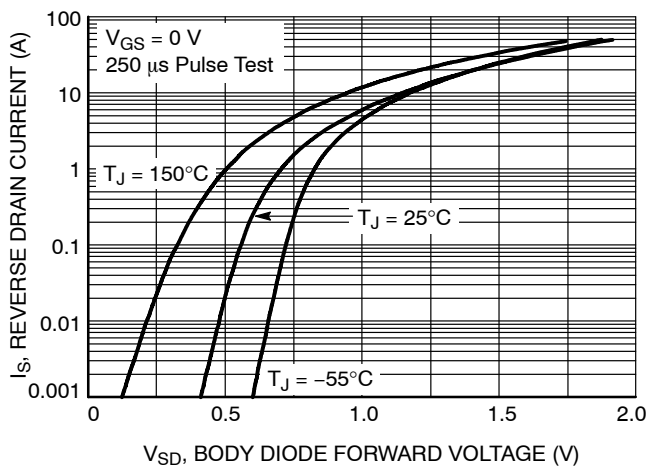


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

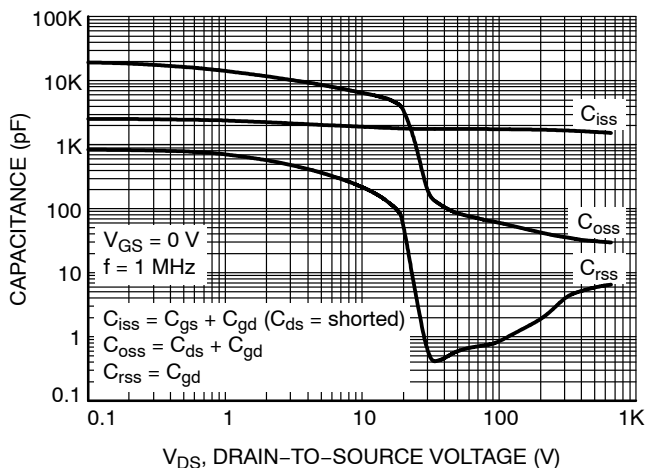


Figure 5. Capacitance Characteristics

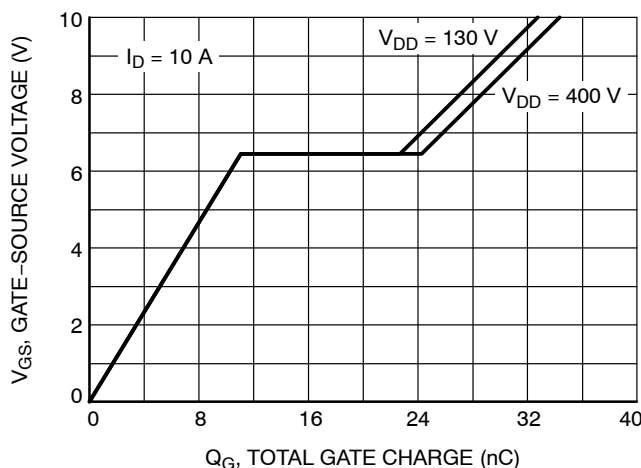


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

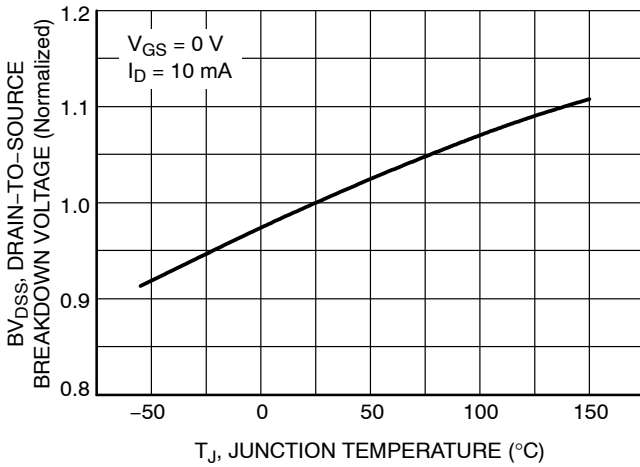


Figure 7. Breakdown Voltage Variation vs. Temperature

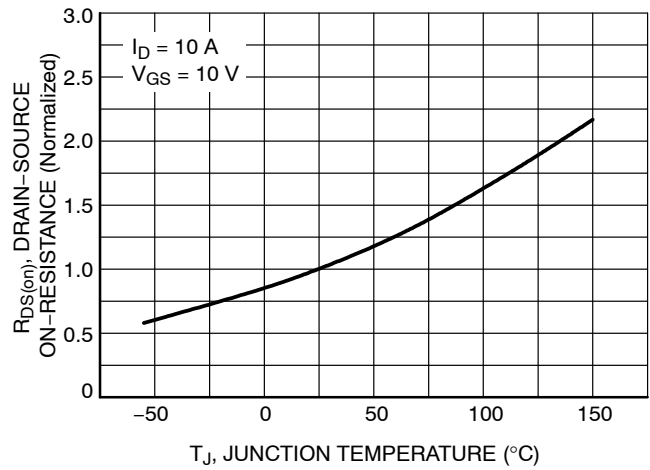


Figure 8. On-Resistance Variation vs. Temperature

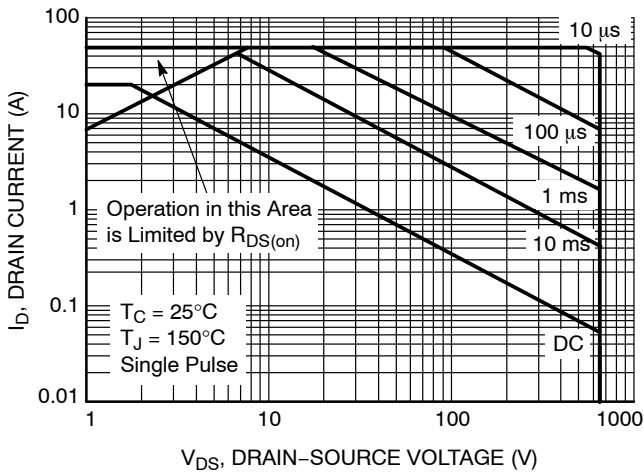


Figure 9. Maximum Safe Operating Area

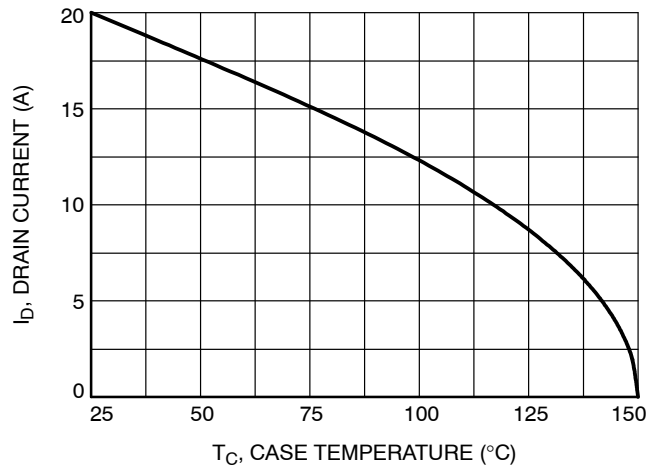


Figure 10. Maximum Drain Current vs. Case Temperature

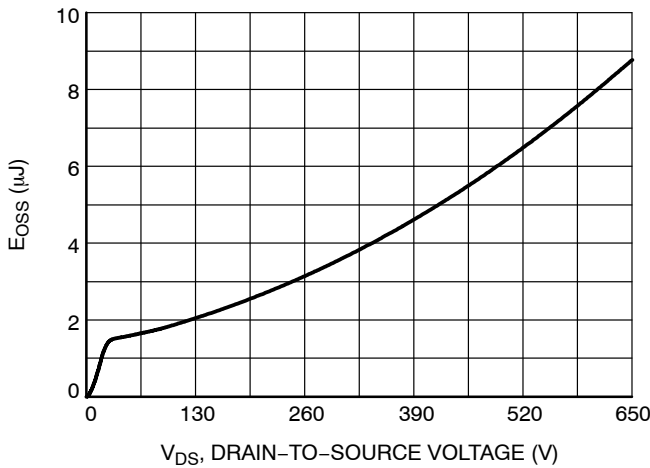


Figure 11. E_{OSS} vs. Drain-to-Source Voltage

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TYPICAL CHARACTERISTICS

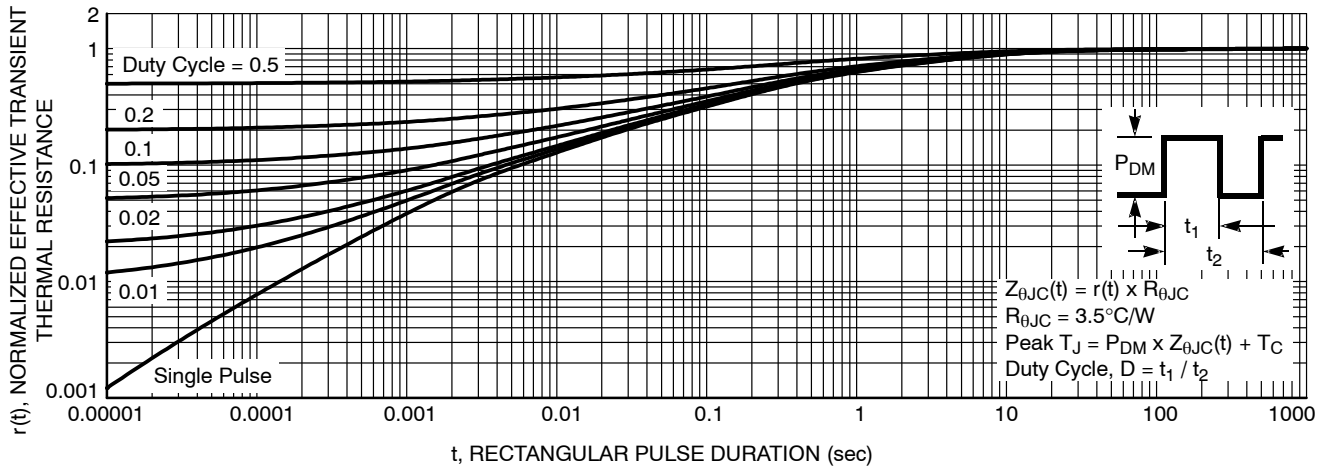


Figure 12. Transient Thermal Response Curve

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Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms



Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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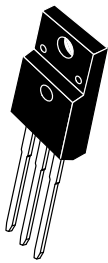


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

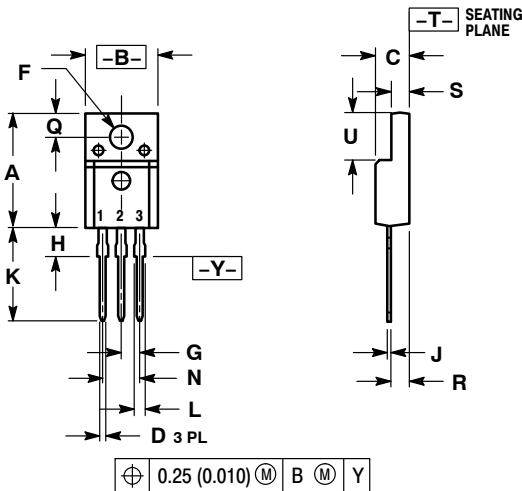
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SCALE 1:1

TO-220 FULLPAK CASE 221D-03 ISSUE K

DATE 27 FEB 2009



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH
 3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

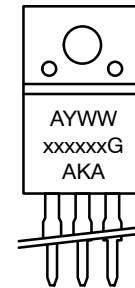
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

MARKING DIAGRAMS

- | | | |
|--|---|--|
| STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE |
| STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE | STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE |



Bipolar




Rectifier

- | | |
|-------------------------------|---------------------------|
| xxxxxx = Specific Device Code | A = Assembly Location |
| G = Pb-Free Package | Y = Year |
| A = Assembly Location | WW = Work Week |
| Y = Year | xxxxxx = Device Code |
| WW = Work Week | G = Pb-Free Package |
| | AKA = Polarity Designator |

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NEW STANDARD:		
DESCRIPTION:	TO-220 FULLPAK	PAGE 1 OF 2



ISSUE	REVISION	DATE
H	REMOVED KNOCKOUT PINS FROM DIAGRAM. REQ. BY S. MASLOWSKI.	19 JUN 2006
J	CHANGED MIN AND MAX VALUES FOR SEVERAL DIMENSIONS. ADDED RECTIFIER MARKING DIAGRAM ABD PREVIOUS MARKING DIAGRAM BIPOLAR. REQ. BY S. MASLOWSKI.	07 JUN 2007
K	RE-INTRODUCED KNOCKOUT PINS INTO DIAGRAM. REQ. BY L. TSAI.	27 FEB 2009

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