

# NTR4501NS

## Power MOSFET

20 V, 3.2 A, Single N-Channel, SOT-23

### Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- 2.5 V Rated for Low Voltage Gate Drive
- SOT-23 Surface Mount for Small Footprint
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Load/Power Switch for Portables
- Load/Power Switch for Computing
- DC-DC Conversion

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	20	V
Gate-to-Source Voltage			V <sub>GS</sub>	±12	V
Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	3.2	A
		T <sub>A</sub> = 85°C		2.4	A
Steady State Power Dissipation (Note 1)	Steady State		P <sub>D</sub>	1.25	W
Pulsed Drain Current	t <sub>p</sub> = 10 μs		I <sub>DM</sub>	10.0	A
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Continuous Source Current (Body Diode)			I <sub>S</sub>	1.6	A
Pulse Source Current (Body Diode) (Note 3)			I <sub>SM</sub>	4.8	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient (Note 1)	R <sub>θJA</sub>	100	°C/W
Junction-to-Ambient (Note 2)	R <sub>θJA</sub>	300	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size.
3. Guaranteed by design.

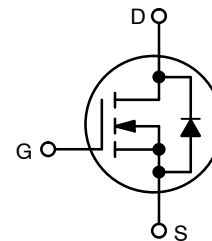


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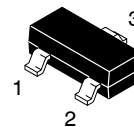
[www.onsemi.com](http://www.onsemi.com)

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> Typ	I <sub>D</sub> Max (Note 1)
20 V	70 mΩ @ 4.5 V	3.6 A
	88 mΩ @ 2.5 V	3.1 A

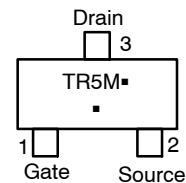
### N-Channel



### MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23  
CASE 318  
STYLE 21



TR5 = Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or overbar may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NTR4501NST1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Typ	Max	Unit
Junction-to-Ambient (Note 4)	$R_{\theta JA}$	94	100	°C/W
Junction-to-Ambient (Note 5)	$R_{\theta JA}$	282	300	

4. Surface-mounted on FR4 board using 1 sq-in pad, (Cu area = 1.127 in sq [1 oz] including traces).  
 5. Surface-mounted on FR4 board using the minimum recommended pad size.

## Electrical Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 6)	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20	24.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			22		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$			1.5	$\mu\text{A}$
		$V_{DS} = 16\text{ V}, T_J = 85^\circ\text{C}$			10	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS

Gate Threshold Voltage (Note 6)	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	0.65	0.85	1.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-2.3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 3.6\text{ A}$		70	84	m $\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 3.1\text{ A}$		88	106	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5.0\text{ V}, I_D = 3.6\text{ A}$		9.0		S

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 10\text{ V}$	140	200	260	pF
Output Capacitance	$C_{oss}$		56	80	104	
Reverse Transfer Capacitance	$C_{rss}$			50	65	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 3.6\text{ A}$	1.7	2.4	3.1	nC
Gate-to-Source Gate Charge	$Q_{GS}$		0.4	0.5	0.7	
Gate-to-Drain Charge	$Q_{GD}$		0.4	0.6	0.8	

### SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 3.6\text{ A}, R_G = 6.0\ \Omega$		6.5	8.5	ns
Rise Time	$t_r$			12	15.6	
Turn-Off Delay Time	$t_{d(off)}$			12	15.6	
Fall Time	$t_f$			3.0	3.9	

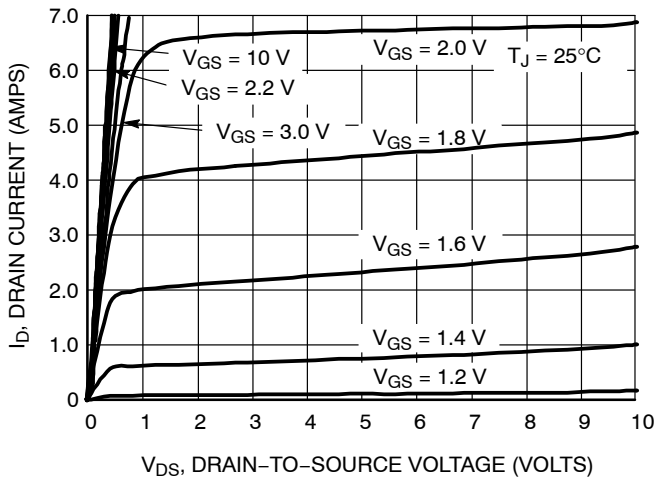
### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_{SD} = 1.6\text{ A}$		0.8	1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 1.6\text{ A}$		7.1	11.3	ns
Charge Time	$t_a$			5.0		
Discharge Time	$t_b$			1.9		
Reverse Recovery Charge	$Q_{RR}$			3.0		nC
Gate Resistance	$R_G$				12.5	16

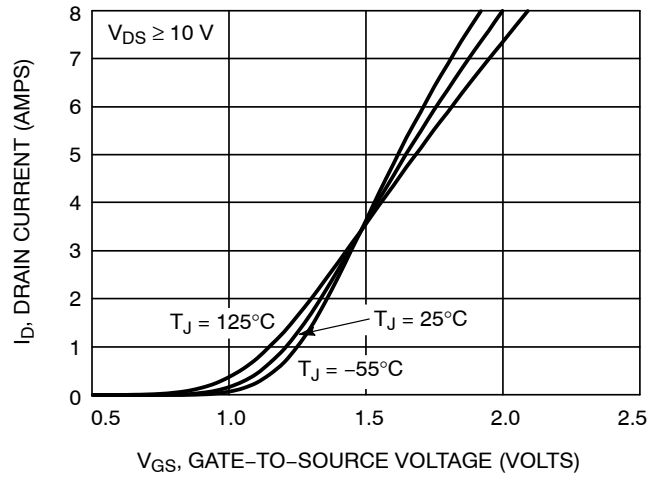
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: Pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 7. Switching characteristics are independent of operating junction temperatures.

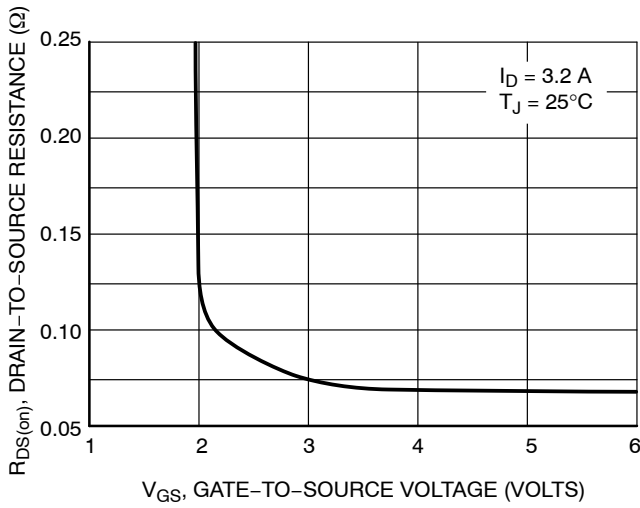
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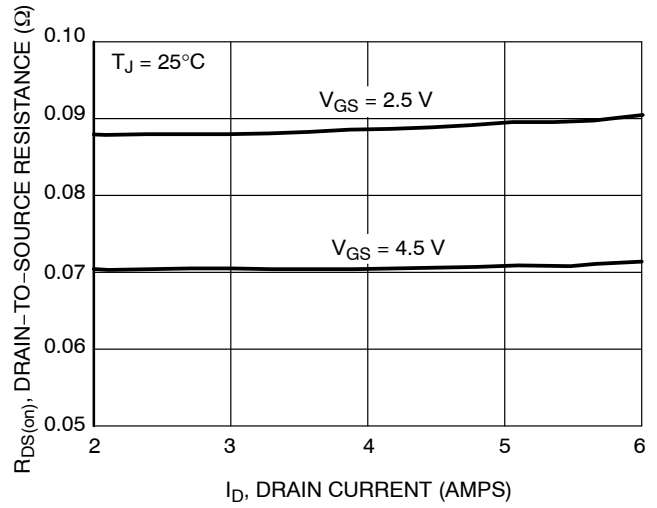
**Figure 1. On-Region Characteristics**



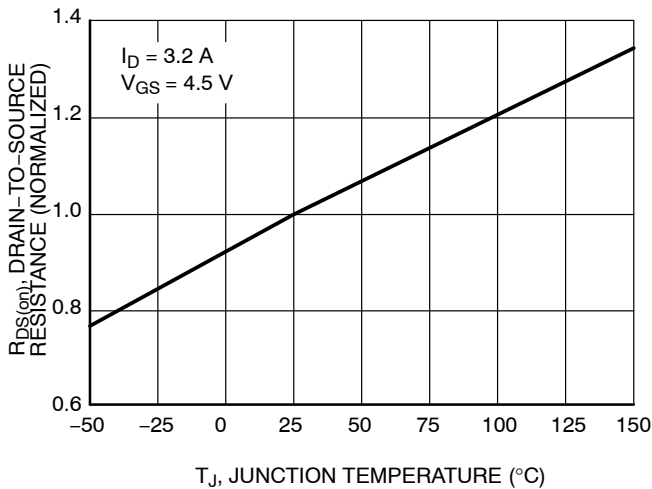
**Figure 2. Transfer Characteristics**



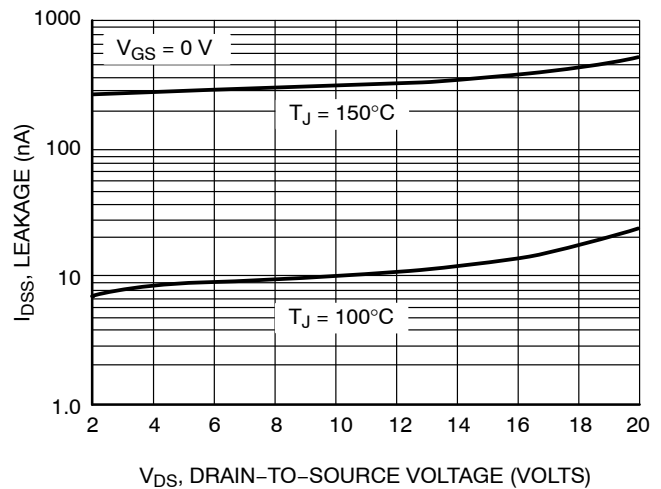
**Figure 3. On-Resistance versus Gate-to-Source Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current versus Voltage**

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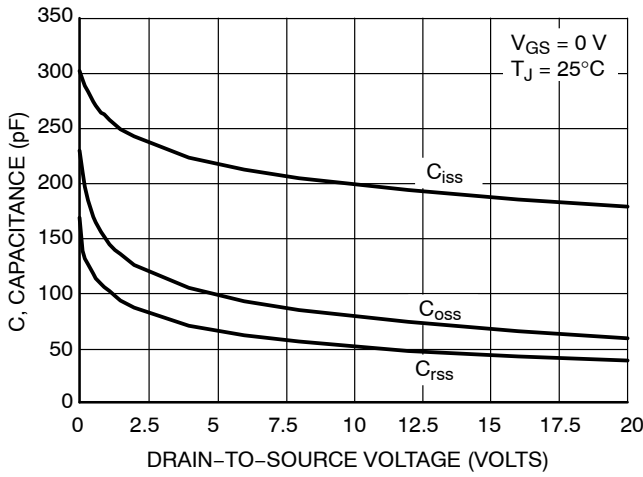


Figure 7. Capacitance Variation

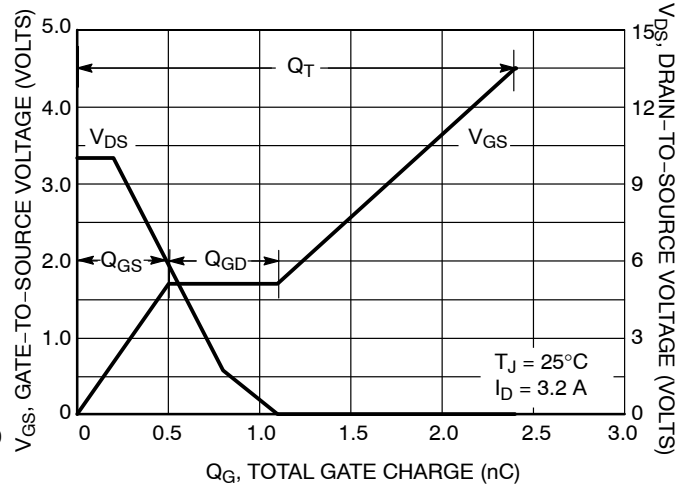


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

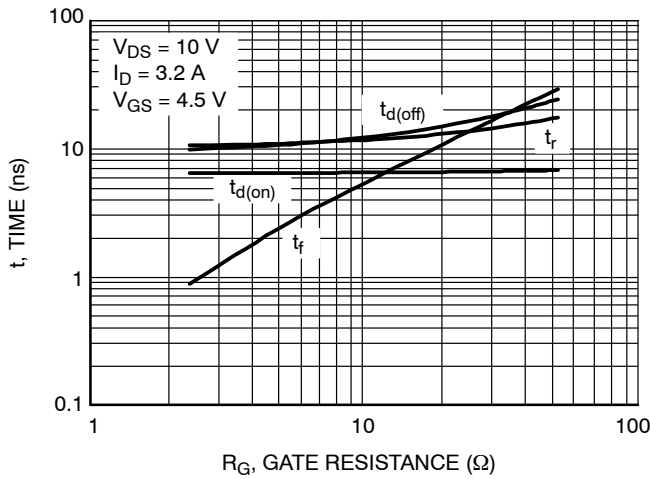


Figure 9. Resistive Switching Time Variation versus Gate Resistance

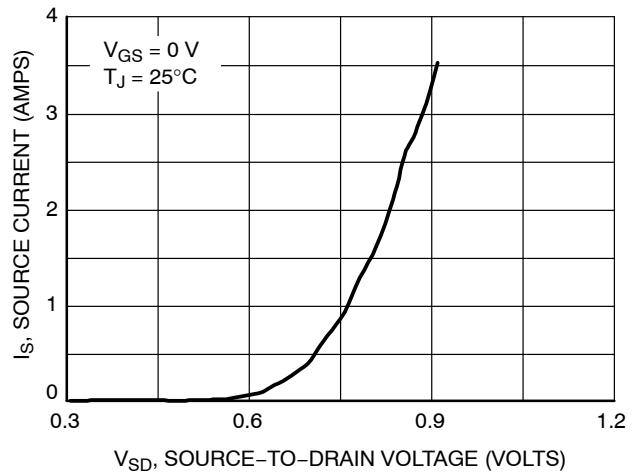


Figure 10. Diode Forward Voltage versus Current

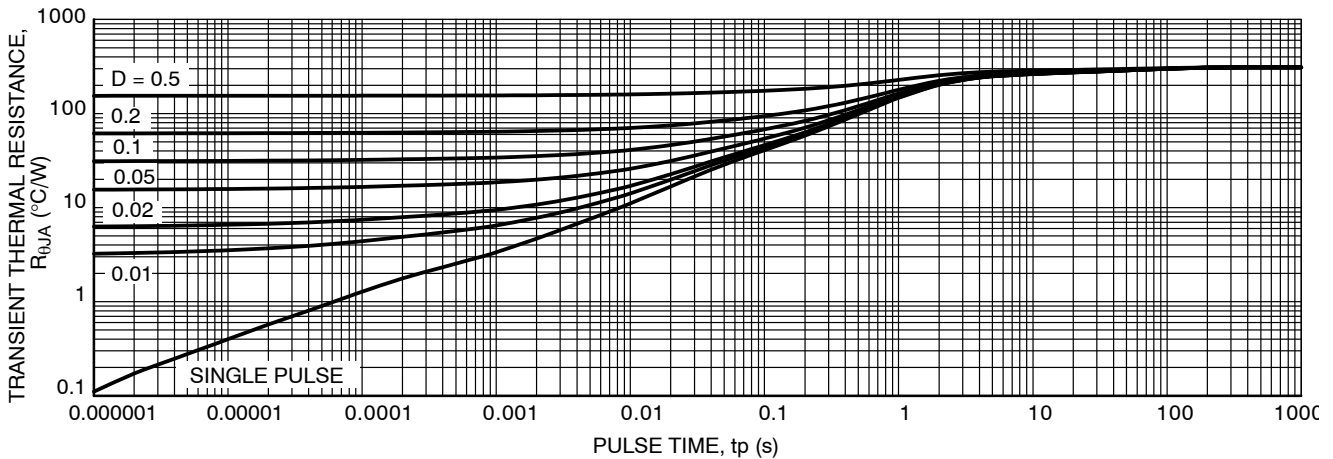
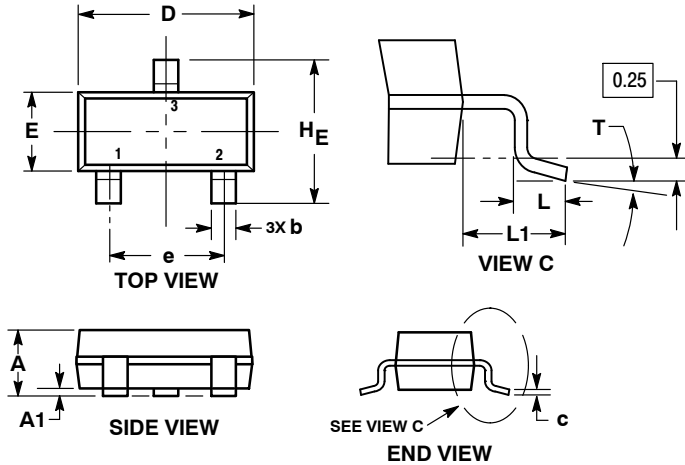


Figure 11. Thermal Response

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## PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AR



### NOTES:

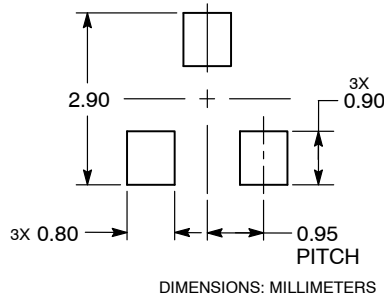
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

### STYLE 21:

- PIN 1. GATE
- SOURCE
- DRAIN

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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