# **Dual N-Channel PowerTrench® MOSFET**

Q1:30 V, 11.6 m $\Omega$ ; Q2: 30 V, 6.4 m $\Omega$ 

#### **General Description**

This device includes two specialized N-Channel MOSFETs in a dual power33 (3 mm X 3 mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

#### **Features**

O1: N-Channel

- Max  $r_{DS(on)} = 11.6 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 10 \text{ A}$
- Max  $r_{DS(on)} = 13.3 \text{ m}\Omega$  at  $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 9 \text{ A}$

Q2: N-Channel

- Max  $r_{DS(on)} = 6.4 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 16 \text{ A}$
- Max  $r_{DS(on)} = 7.0 \text{ m}\Omega$  at  $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 15 \text{ A}$
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

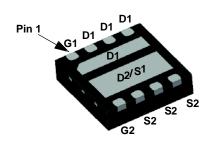
#### **Applications**

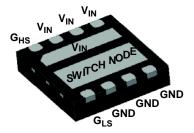
- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load



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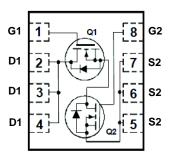
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(Bottom Views)

WDFN8 Power33 CASE 511DE



#### **ORDERING INFORMATION**

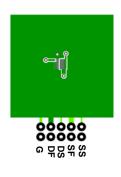
See detailed ordering and shipping information on page 3 of this data sheet.

**Table 1. MOSFET MAXIMUM RATINGS**  $T_C = 25^{\circ}C$  unless otherwise noted.

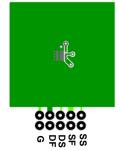
Symbol	Parameter	Q1	Q2	Units	
V <sub>DS</sub>	Drain to Source Voltage		30	30	V
$V_{GS}$	Gate to Source Voltage	(Note 4)	±12	±12	V
Ι <sub>D</sub>	Drain Current -Continuous	T <sub>C</sub> = 25°C (Note 9)	29	46	Α
	- Continuous	T <sub>C</sub> = 100°C (Note 9)	18	29	
	- Continuous	T <sub>A</sub> = 25°C	10 (Note 5)	16 (Note 6)	
	– Pulsed	T <sub>A</sub> = 25°C (Note 10)	113	302	
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 3)	24	54	mJ
$P_{D}$	Power Dissipation for Single Operation	T <sub>A</sub> = 25°C	1.9 (Note 5)	2.5 (Note 6)	W
	Power Dissipation for Single Operation	T <sub>A</sub> = 25°C	0.7 (Note 7)	1.0 (Note 8)	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		–55 to	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.
- Pulsed Id please refer to Figure 11 and Figure 24 SOA graphs for more details.
   Q1: E<sub>AS</sub> of 24 mJ is based on starting T<sub>J</sub> = 25°C; L = 3 mH, I<sub>AS</sub> = 4 A, V<sub>DD</sub> = 30 V, V<sub>GS</sub> = 10 V. 100% tested at L = 0.1 mH, I<sub>AS</sub> = 13 A. Q2: E<sub>AS</sub> of 54 mJ is based on starting T<sub>J</sub> = 25°C; L = 3 mH, I<sub>AS</sub> = 6 A, V<sub>DD</sub> = 30 V, V<sub>GS</sub> = 10 V. 100% tested at L = 0.1 mH, I<sub>AS</sub> = 22 A.
   As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.



5. 65°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



6. 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



7. 180°C/W when mounted on a minimum pad of 2 oz copper



8. 125°C/W when mounted on a minimum pad of 2 oz copper

### Table 2. PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
D13N03	NTTFD013N03P8	Power 33	13″	12 mm	3000 units

## **Table 3. THERMAL CHARACTERISTICS**

$R_{ heta JC}$	Thermal Resistance, Junction to Case	8.2	6.1	°C/W
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient	65 (Note 9)	50 (Note 9)	
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient	180 (Note 9)	125 (Note 9)	

R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material, R<sub>θCA</sub> is determined by the user's board design.

### **Table 4. ELECTRICAL CHARACTERISTICS** $T_J = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
OFF CHAR	ACTERISTICS	•	•	•	•		
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	Q1 Q2	30 30			V
$\Delta BV_{DSS}$ / $\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25°C	Q1 Q2		15 16		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	Q1 Q2			1 1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0 \text{ V}$	Q1 Q2			±100 ±100	nA nA
ON CHARA	CTERISTICS		•	•	•		•
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	Q1 Q2	1.0 1.0	1.3 1.8	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25°C	Q1 Q2		-4 -4		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A, T <sub>J</sub> = 125°C	Q1		7.7 8.9 10.8	11.5 13.3 16.3	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 16 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 16 A, T <sub>J</sub> = 125°C	Q2		4.4 5.4 6.2	6.3 7.0 9.0	
9FS	Forward Transconductance	V <sub>DD</sub> = 5 V, I <sub>D</sub> = 10 A V <sub>DD</sub> = 5 V, I <sub>D</sub> = 16 A	Q1 Q2		46 70		S
DYNAMIC (	CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHZ	Q1 Q2		792 1685	1100 2300	pF
C <sub>oss</sub>	Output Capacitance	]	Q1 Q2		230 467	320 650	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		Q1 Q2		20 36	30 50	pF
$R_g$	Gate Resistance		Q1 Q2	0.1 0.1	2.0 1.2	4.0 2.4	Ω
SWITCHING	CHARACTERISTICS				-		
t <sub>d(on)</sub>	Turn-On Delay Time	Q1: V <sub>DD</sub> = 15 V, I <sub>D</sub> = 10 A,	Q1 Q2		7 10	14 20	ns
t <sub>r</sub>	Rise Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		2 3	10 10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$Q_2$ : $V_{DD} = 15 \text{ V}, I_D = 16 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2		19 24	33 39	ns
t <sub>f</sub>	Fall Time		Q1 Q2		2 3	10 10	ns

Table 4. ELECTRICAL CHARACTERISTICS T<sub>.1</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions		Туре	Min	Тур	Max	Units
SWITCHING	CHARACTERISTICS							
Q <sub>g(tot)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	Q1 V <sub>DD</sub> = 15 V,	Q1 Q2		12 24	17 34	nC
Q <sub>g(tot)</sub>	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$	I <sub>D</sub> = 10 A	Q1 Q2		5.5 11	7.7 16	nC
$Q_{gs}$	Gate to Source Charge		V <sub>DD</sub> = 15 V, I <sub>D</sub> = 16 A	Q1 Q2		1.7 4.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			Q1 Q2		1.3 2.7		nC
DRAIN-SO	URCE DIODE CHARACTERISTICS							
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$ \begin{array}{c} V_{GS} = 0 \text{ V, } I_{S} = 10 \text{ A (Note 10)} \\ V_{GS} = 0 \text{ V, } I_{S} = 1.5 \text{ A (Note 10)} \\ V_{GS} = 0 \text{ V, } I_{S} = 16 \text{ A (Note 10)} \\ V_{GS} = 0 \text{ V, } I_{S} = 2 \text{ A (Note 10)} \\ \end{array} $		Q1 Q1 Q2 Q2		0.85 0.75 0.83 0.73	1.2 1.2 1.2 1.2	V
t <sub>rr</sub>	Reverse Recovery Time	Q1 $I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$ Q2 $I_F = 16 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		Q1 Q2		17 27	31 42	ns
Q <sub>rr</sub>	Reverse Recovery Charge			Q1 Q2		5 10	10 20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Pulse Test: Pulse Width < 300 µs, Duty Cycle < 2.0%.

## Typical Characteristics (Q1 N-Channel) T<sub>J</sub> = 25°C unless otherwise noted.

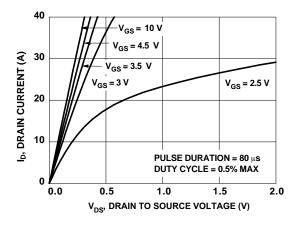


Figure 1. On Region Characteristics

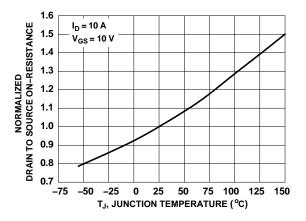


Figure 3. Normalized On–Resistance vs. Junction Temperature

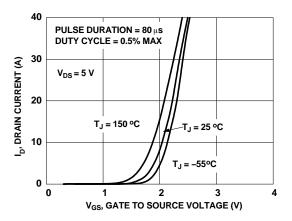


Figure 5. Transfer Characteristics

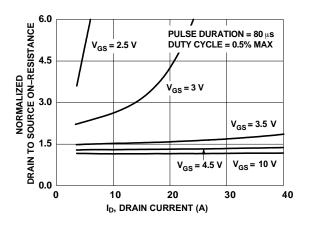


Figure 2. Normalized On–Resistance vs. Drain Current and Gate Voltage

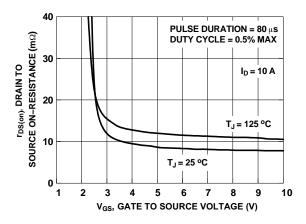


Figure 4. On–Resistance vs. Gate to Source Voltage

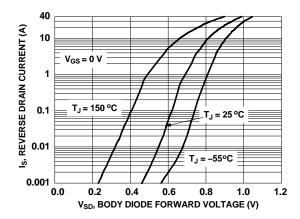


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

## Typical Characteristics (Q1 N-Channel) T<sub>J</sub> = 25°C unless otherwise noted.

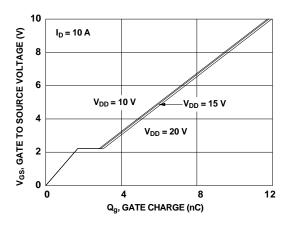


Figure 7. Gate Charge Characteristics

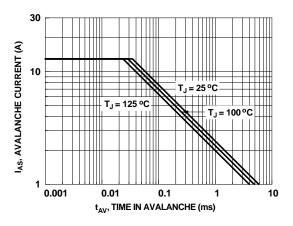


Figure 9. Unclamped Inductive Switching Capability

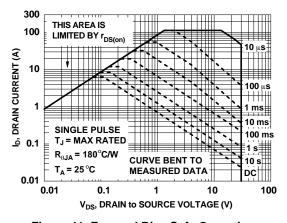


Figure 11. Forward Bias Safe Operating Area

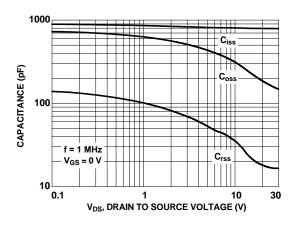


Figure 8. Capacitance vs. Drain to Source Voltage

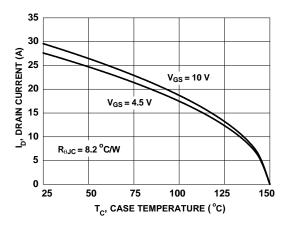


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

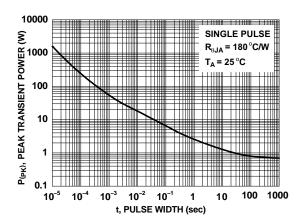


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N–Channel)  $T_J = 25$ °C unless otherwise noted.

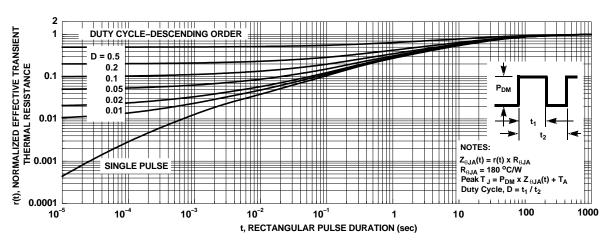


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

### Typical Characteristics (Q2 N-Channel) T<sub>.I</sub> = 25°C unless otherwise noted.

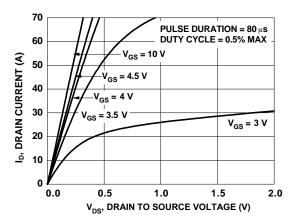


Figure 14. On Region Characteristics

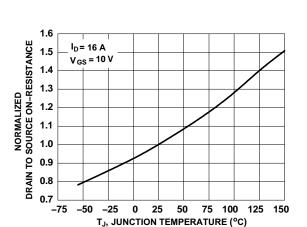


Figure 16. Normalized On–Resistance vs. Junction Temperature

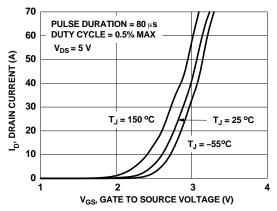


Figure 18. Transfer Characteristics

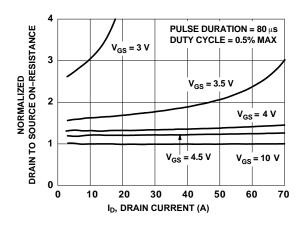


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

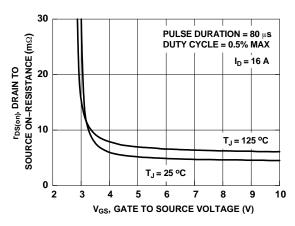


Figure 17. On–Resistance vs. Gate to Source Voltage

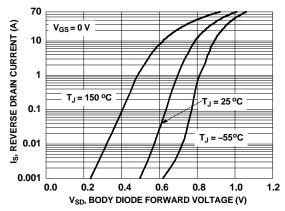


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

## Typical Characteristics (Q2 N-Channel) T<sub>J</sub> = 25°C unless otherwise noted.

10000

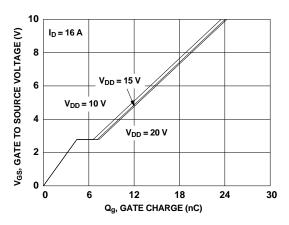


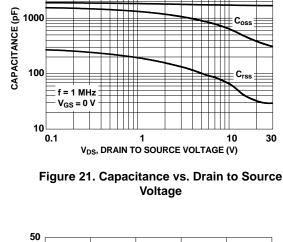
Figure 20. Gate Charge Characteristics

30

10

0.001

IAS, AVALANCHE CURRENT (A)



30

100

Figure 22. Unclamped Inductive Switching Capability

t<sub>AV</sub>, TIME IN AVALANCHE (ms)

1

10

T<sub>J</sub> = 125 °C

0.1

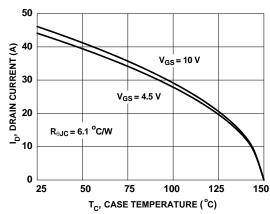


Figure 23. Maximum Continuous Drain **Current vs. Case Temperature** 

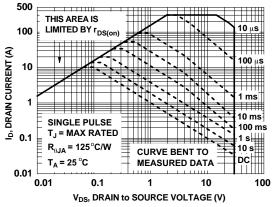


Figure 24. Forward Bias Safe Operating Area

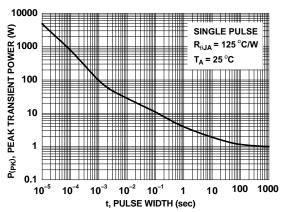


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N–Channel)  $T_J = 25$ °C unless otherwise noted.

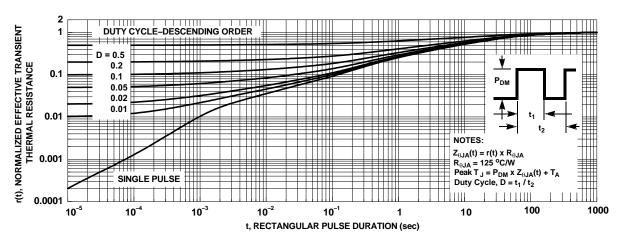
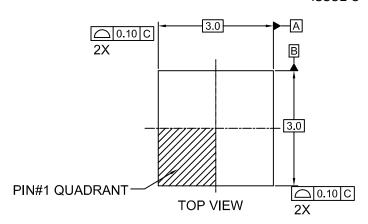
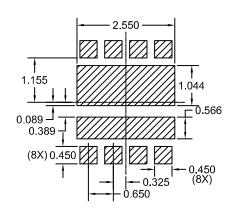


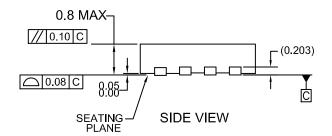
Figure 26. Junction-to-Ambient Transient Thermal Response Curve

#### **PACKAGE DIMENSIONS**

#### WDFN8 3x3, 0.65P CASE 511DE ISSUE O

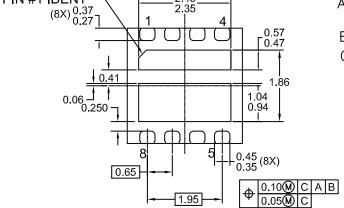






RECOMMENDED LAND PATTERN

## 



**BOTTOM VIEW** 

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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