Product Preview

Power MOSFET

120 V, 12.0 m Ω , TBD A, Single N-Channel

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Breakdown Voltage			$V_{(BR)DSS}$	120	V
Gate-to-Source Voltage)		V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady	T _C = 25°C	I _D	TBD	Α
Power Dissipation $R_{\theta JC}$ (Note 2)	State	T _C = 25°C	P _D	TBD	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady	T _A = 25°C	I _D	TBD	Α
Power Dissipation R _{θJA} (Notes 1, 2)	State	T _A = 25°C	P _D	TBD	W
Pulsed Drain Current	$T_A = 25$	°C, t _p = 10 μs	I _{DM}	TBD	Α
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Source Current (Body Diode)			I _S	TBD	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{AV} = TBD A, L = TBD)			E _{AS}	TBD	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			TL	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{\theta JC}$	TBD	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	TBD	

- 1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

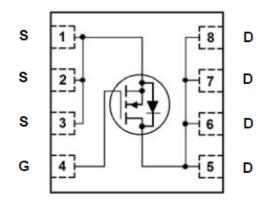
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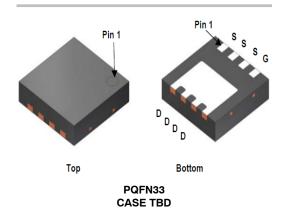


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V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX	
120 V	12.0 mΩ @ 10 V	TBD A	
	TBD mΩ @ 6 V	IDDA	





ORDERING INFORMATION

Device	Package	Shipping [†]
NTTFS012N12MC	PQFN33 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

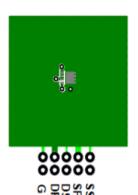
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
OFF CHARACTERISTICS								
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		120			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /	I _D = 250 μA, ref to 25°C			TBD		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$,	T _J = 25°C			10	μΑ	
		V _{DS} = 60 V	T _J = 125°C			100		
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 V, V_{GS}$	= ±20 V			±100	nA	
ON CHARACTERISTICS (Note 3)								
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D =$	TBD μA	2.0		4.0	V	
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 250 μA, ref	to 25°C		TBD		mV/°C	
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = TBD A		TBD	12.0	mΩ	
		V _{GS} = 6 V	I _D = TBD A		TBD	TBD	-	
Forward Transconductance	9 _{FS}	V _{DS} = TBD V, I _D	= TBD A		TBD		S	
Gate-Resistance	R_{G}	T _A = 25°	С		TBD		Ω	
CHARGES & CAPACITANCES								
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz	z, V _{DS} = 60 V		1338		pF	
Output Capacitance	Coss				633		1	
Reverse Transfer Capacitance	C _{RSS}				13		1	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 60 V, I _D = TBD A			20		nC	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 6 V, V _{DS}	; = 60 V,		TBD		1	
Gate-to-Source Charge	Q _{GS}	I _D = TBD A			5		1	
Gate-to-Drain Charge	Q_{GD}				7		1	
Plateau Voltage	V_{GP}				TBD		V	
SWITCHING CHARACTERISTICS (Note 3)	•							
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS}	s = 60 V,		TBD		ns	
Rise Time	t _r	$I_D = TBD A, R_G = TBD \Omega$			TBD		- - -	
Turn-Off Delay Time	t _{d(OFF)}				TBD			
Fall Time	t _f			TBD				
DRAIN-SOURCE DIODE CHARACTERISTIC	s							
Forward Diode Voltage	V _{SD}	$V_{GS} = 0 V$, $I_S = TBD A$	T _J = 25°C		TBD		V	
			T _J = 125°C		TBD		1	
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, dls/dt} = 300 \text{ A/}\mu\text{s,}$ $I_{S} = \text{TBD A}$ $V_{GS} = 0 \text{ V, dls/dt} = 1000 \text{ A/}\mu\text{s,}$ $I_{S} = \text{TBD A}$			TBD		ns	
Reverse Recovery Charge	Q _{RR}				TBD		nC	
Reverse Recovery Time	t _{RR}				TBD		ns	
Reverse Recovery Charge	Q _{RR}				TBD		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

NOTES:

4. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in² pad of 2 oz copper.



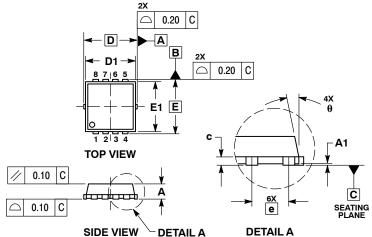
b. 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < TBD. Duty cycle < TBD.
 E_{AS} of TBD is based on started T_J = 25°C, L = TBD, I_{AS} = TBD, V_{DD} = TBD, V_{GS} = TBD. 100% test at L = TBD, I_{AS} = TBD.
 As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

PACKAGE DIMENSIONS

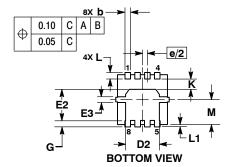
PQFN33 3.3x3.3, 0.65P

CASE TBD **ISSUE O**

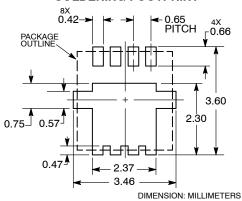


- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH
 PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00		0.05	0.000		0.002	
b	0.23	0.30	0.40	0.009	0.012	0.016	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D		3.30 BSC	C 0.130 BSC		0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
E		3.30 BSC		0.130 BSC			
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	0.23	0.30	0.40	0.009	0.012	0.016	
е		0.65 BSC 0.026 BSC			0		
G	0.30	0.41	0.51	0.012	0.016	0.020	
K	0.65	0.80	0.95	0.026	0.032	0.037	
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
M	1.40	1.50	1.60	0.055	0.059	0.063	
θ	0 °		12 °	0 °		12 °	



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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