NTTFS018N12MC

Product Preview

Power MOSFET

120 V, 18.0 mΩ, TBD A, Single N−Channel

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Breakdown Voltage			$V_{(BR)DSS}$	120	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	TBD	A
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	P_D	TBD	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	TBD	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	TBD	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	TBD	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	TBD	A
Single Pulse Drain−to−Source Avalanche Energy (I_{AV} = TBD A, L = TBD)			E_{AS}	TBD	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	TBD	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	TBD	

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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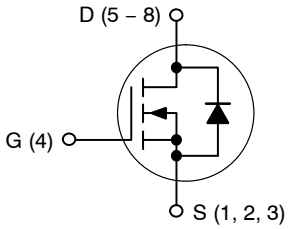
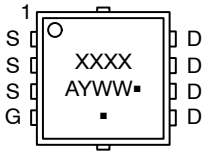
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
120 V	18.0 mΩ @ 10 V	TBD A
	TBD mΩ @ 6 V	

N−Channel



WDFN8
(μ8FL)
CASE 511AB

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS018N12MC	WDFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

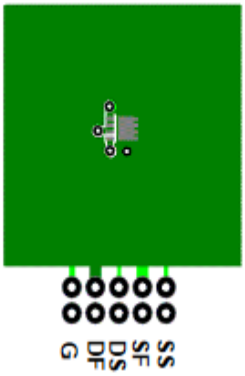
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		120			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			TBD		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			10	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = TBD μA		2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 250 μA, ref to 25°C			TBD		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = TBD A		TBD	18.0	mΩ
		V_{GS} = 6 V	I_D = TBD A		TBD	TBD	
Forward Transconductance	g_{FS}	V_{DS} =TBD V, I_D = TBD A			TBD		S
Gate−Resistance	R_G	T_A = 25°C			TBD		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 60 V			943		pF
Output Capacitance	C_{OSS}				439		
Reverse Transfer Capacitance	C_{RSS}				9		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 60 V, I_D = TBD A			14		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 6 V, V_{DS} = 60 V, I_D = TBD A			TBD		
Gate−to−Source Charge	Q_{GS}				4		
Gate−to−Drain Charge	Q_{GD}				5		
Plateau Voltage	V_{GP}				TBD		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 60 V, I_D = TBD A, R_G = TBD Ω			TBD		ns
Rise Time	t_r				TBD		
Turn−Off Delay Time	$t_{d(OFF)}$				TBD		
Fall Time	t_f				TBD		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = TBD A	T_J = 25°C		TBD		V
			T_J = 125°C		TBD		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 300 A/μs, I_S = TBD A			TBD		ns
Reverse Recovery Charge	Q_{RR}				TBD		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 1000 A/μs, I_S = TBD A			TBD		ns
Reverse Recovery Charge	Q_{RR}				TBD		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

NOTES:

4. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



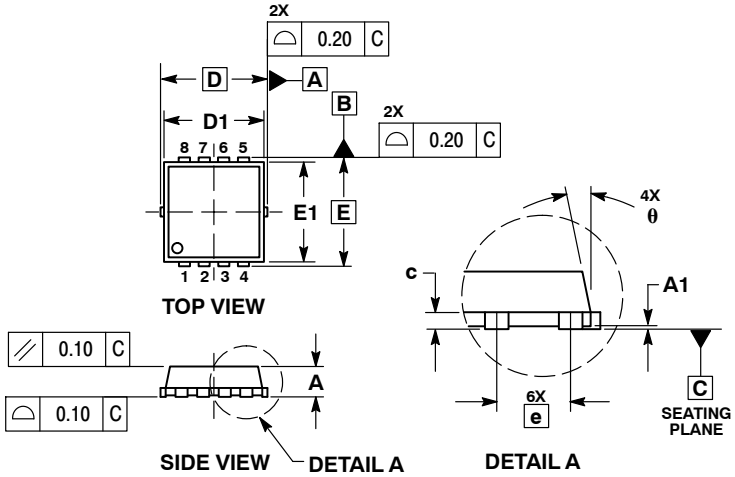
a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper.

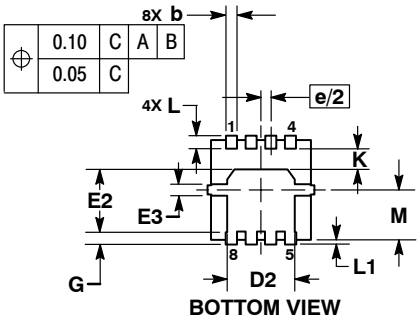
b. 125°C/W when mounted on a minimum pad of 2 oz copper.

5. Pulse Test: Pulse Width < TBD. Duty cycle < TBD.
6. E_{AS} of TBD is based on started T_J = 25°C, L = TBD, I_{AS} = TBD, V_{DD} = TBD, V_{GS} = TBD. 100% test at L = TBD, I_{AS} = TBD.
7. As an N−ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

PACKAGE DIMENSIONS

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

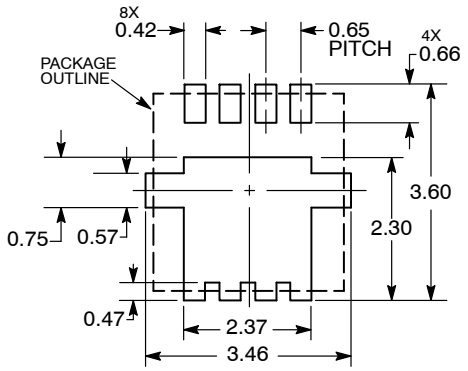




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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