MOSFET - Power, Single N-Channel, Power33 25 V, 1.0 mΩ, 180 A

Features

- Small Footprint for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DC-DC Converters
- Power Load Switch
- Notebook Battery Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	/ _{DSS} 25	
Gate-to-Source Voltage			V _{GS} +16/-1		٧
Continuous Drain		T _C = 25°C	I _D	180	Α
Current R _{θJC} (Note 3)	Steady	T _C = 85°C		130	
Power Dissipation $R_{\theta JC}$ (Note 3)	State	T _C = 25°C	P _D	52	W
Continuous Drain		T _A = 25°C	I _D	41	Α
Current R _{θJA} (Notes 1, 3)	Steady	T _A = 85°C	1	29	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	State	T _A = 25°C	P _D	2.7	W
Continuous Drain		T _A = 25°C	I _D	23	Α
Current R _{θJA} (Notes 2, 3)	Steady	T _A = 85°C		16	
Power Dissipation R _{θJA} (Notes 2, 3)	State T _A = 25°C		P _D	0.82	W
Pulsed Drain Current	$T_A = 25$	°C, t _p = 10 μs	I _{DM}	195	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 63.7 A) (Note 4)			E _{AS}	202	mJ
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Surface-mounted on FR4 board using a 1 in2 pad size, 2 oz Cu pad.
- Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
- 3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electromechanical application board design. $R_{\theta CA}$ is determined by the user's board design.
- 4. 100% UIS tested at L = 0.1 mH, I_{AV} = 40 A.

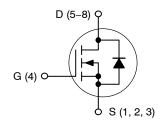


ON Semiconductor®

www.onsemi.com

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
25 V	1.0 m Ω @ 10 V	100 A
25 V	1.2 m Ω @ 4.5 V	180 A

NMOS





PQFN8 (Power33) CASE 483AW

MARKING DIAGRAM



2EJN = Specific Device Code A = Assembly Location

Y = Year WW = Work Week ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case - Steady State (Note 1)	$R_{ heta JC}$	2.4	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{ hetaJA}$	47	
Junction-to-Ambient - Steady State (Note 2)	$R_{ hetaJA}$	152	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_{D} = 1 \text{ mA}$		25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /	I _D = 1 mA, ref to 25°C			16		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			10	μΑ
		$V_{DS} = 20 \text{ V}$	T _J = 125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = +16/-12 V				±100	±nA
ON CHARACTERISTICS (Note 5)	•			•			
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 934 \mu A$		1.2		2.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = 934 μA, ref to 25°C			-4.4		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 38 A		0.86	1.0	mΩ
		V _{GS} = 4.5 V	I _D = 35 A		1.05	1.2	
Forward Transconductance	9 _{FS}	V _{DS} = 5 V, I _D = 38 A			224		S
Gate Resistance	R_{G}	T _A = 25°C			0.5		Ω
CHARGES & CAPACITANCES	•						
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 13 V			4040		pF
Output Capacitance	C _{OSS}				1100		
Reverse Capacitance	C _{RSS}				68		
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 13 \text{ V}; I_D = 38 \text{ A}$ $V_{GS} = 10 \text{ V}, V_{DS} = 13 \text{ V}; I_D = 38 \text{ A}$			24		nC
Threshold Gate Charge	Q _{G(TH)}				5.2		
Gate-to-Drain Charge	Q_{GD}				3.9		
Gate-to-Source Charge	Q_{GS}				9.8		
Total Gate Charge	Q _{G(TOT)}				54		
SWITCHING CHARACTERISTICS, V _{GS} =	4.5 V (Note 5)						
Turn-On Delay Time	t _{d(ON)}				24.6		T
Rise Time	t _r	V _{GS} = 4.5 V, V _E	nn = 13 V,		13		1
Turn-Off Delay Time	t _{d(OFF)}	$I_{\rm D} = 38 \text{ A}, R_{\rm G} = 6 \Omega$			38.5		ns -
Fall Time	t _f				9.8		
SWITCHING CHARACTERISTICS, V _{GS} =	10 V (Note 5)						
Turn-On Delay Time	t _{d(ON)}	V_{GS} = 10 V, V_{DD} = 13 V, I_{D} = 38 A, R_{G} = 6 Ω			14.8		
Rise Time	t _r				4.2		ns
Turn-Off Delay Time	t _{d(OFF)}				59		
Fall Time	t _f				7.9		
SOURCE-TO-DRAIN DIODE CHARACTE	ERISTICS						
Forward Diode Voltage	V_{SD}	$V_{GS} = 0 \text{ V}, \qquad T_{J} = 25^{\circ} \text{ C}$			0.78	1.2	١,,
		1 OO A			0.65		V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dl/dt = 100 A/μs,			38		ns
Reverse Recovery Charge	Q_{RR}	$V_{GS} = 0$ V, $di/dt = 100$ A/ μ s, $I_{S} = 38$ A			25		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

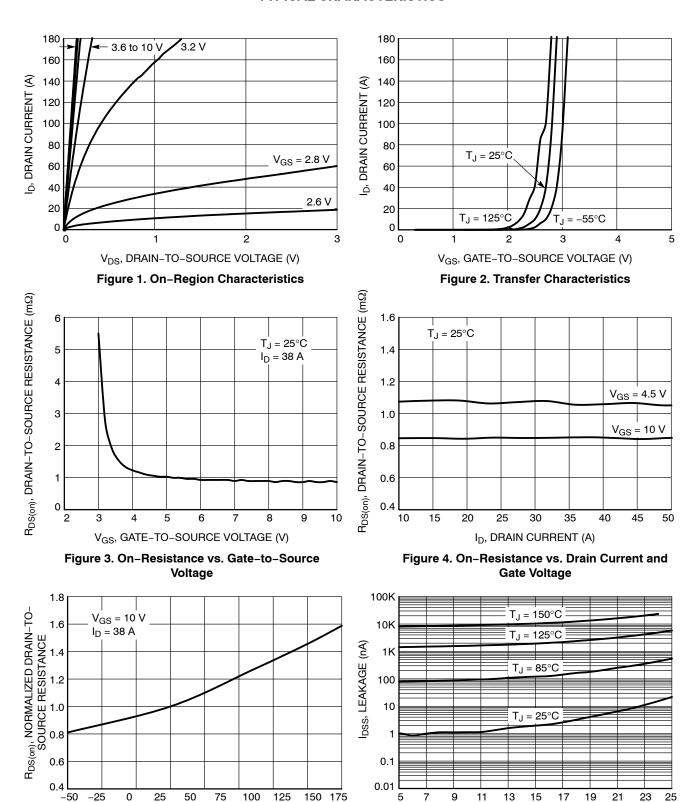


Figure 5. On–Resistance Variation with Temperature

T_J, JUNCTION TEMPERATURE (°C)

Figure 6. Drain-to-Source Leakage Current vs. Voltage

V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

TYPICAL CHARACTERISTICS

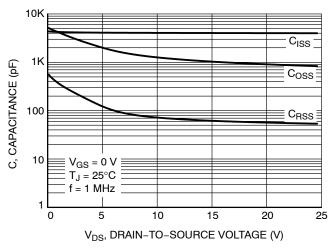


Figure 7. Capacitance Variation

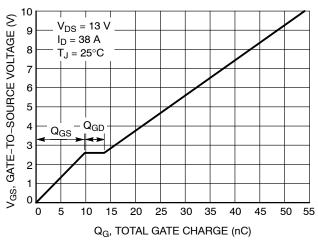


Figure 8. Gate-to-Source vs. Total Charge

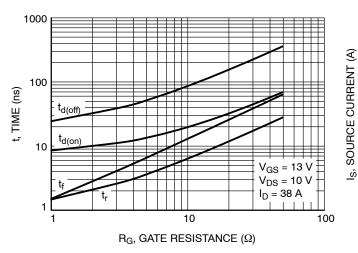


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

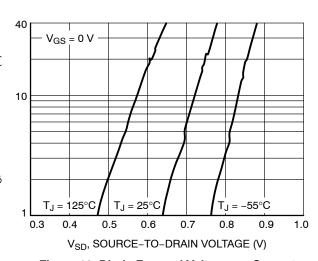


Figure 10. Diode Forward Voltage vs. Current

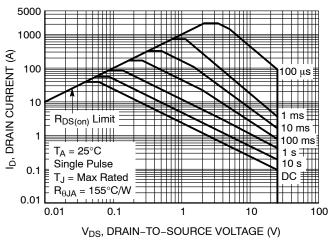


Figure 11. Maximum Rated Forward Biased Safe Operating Area

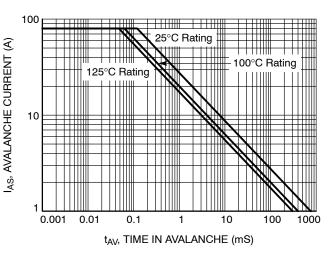


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

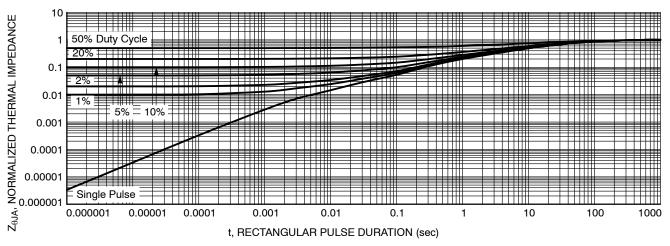


Figure 13. transient Thermal impedance

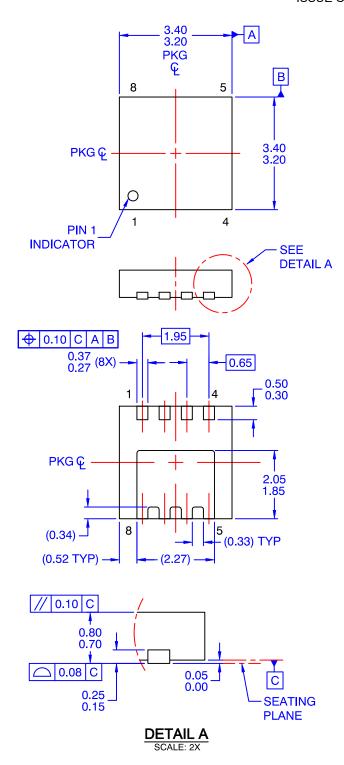
ORDERING INFORMATION

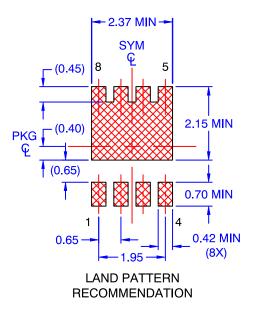
Device	Marking	Package	Shipping [†]
NTTFS1D2N02P1E	2EJN	Power33 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

PQFN8 3.3X3.3, 0.65P CASE 483AW ISSUE O





NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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