NV25010LV, NV25020LV, NV25040LV

EEPROM Serial 1/2/4-Kb SPI Low Voltage Automotive Grade 1

Description

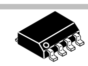
NV25010LV, NV25020LV and NV25040LV are EEPROM Serial 1/2/4−Kb SPI Low Voltage Automotive Grade 1 devices internally organized as 128x8, 256x8 and 512x8 bits. They feature a 16−byte page write buffer and support the Serial Peripheral Interface (SPI) protocol. The devices are enabled through a Chip Select ($\overline{CS}$) input. In addition, the required bus signals are clock input (SCK), data input (SI) and data output (SO) lines. The $\overline{HOLD}$ input may be used to pause any serial communication with the NV250x0 device. The device features software and hardware write protection, including partial as well as full array protection. Byte Level On−Chip ECC (Error Correction Code) makes the device suitable for high reliability applications. The device offers an additional Identification Page which can be permanently write protected.

Features

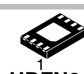
- Automotive AEC−Q100 Grade 1 (−40°C to +125°C) Qualified
- 1.7 V to 5.5 V Supply Voltage Range
- 20 / 10 MHz SPI Compatible
- SPI Modes (0,0) & (1,1)
- 16−byte Page Write Buffer
- Self−timed Write Cycle
- Hardware and Software Protection
- Additional Identification Page with Permanent Write Protection
- NV Prefix for Automotive and Other Applications Requiring Site and Change Control
- Block Write Protection
  - Protect $^1/_4$, $^1/_2$ or Entire EEPROM Array
- Low Power CMOS Technology
- Program/Erase Cycles:
  - 4,000,000 at 25°C
  - 1,200,000 at +85°C
  - 600,000 at +125°C
- 200 Year Data Retention
- SOIC, TSSOP, US 8−lead & Wettable Flank UDFN 8−pad Packages
- This Device is Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

ON Semiconductor®

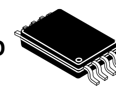
www.onsemi.com



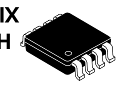
SOIC−8
DW SUFFIX
CASE 751BD



UDFN8
MUW3 SUFFIX
CASE 517DH

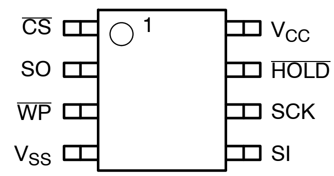


TSSOP−8
DT SUFFIX
CASE 948AL



US8
UV SUFFIX
CASE 493

PIN CONFIGURATION



SOIC (DW), TSSOP (DT), UDFN (MUW3)

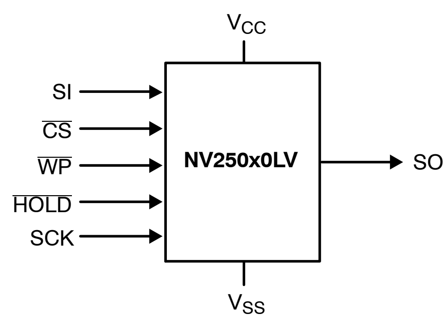


Figure 1. Functional Symbol

PIN FUNCTION

Pin Name	Function
$\overline{CS}$	Chip Select
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock
$\overline{HOLD}$	Hold Transmission Input
V_{CC}	Power Supply

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Unit
Operating Temperature	−45 to +150	°C
Storage Temperature	−65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Test Condition	Max	Unit
NEND	Endurance	$T_A \le 25$°C, 1.7 V < V_{CC} < 5.5 V	4,000,000	Write Cycles (Note 3)
		T_A = 85°C, 1.7 V < V_{CC} < 5.5 V	1,200,000	
		T_A = 125°C, 1.7 V < V_{CC} < 5.5 V	600,000	
TDR	Data Retention	T_A = 25°C	200	Year

2. Determined through qualification/characterization.
3. A Write Cycle refers to writing a Byte, a Page, the Status Register or the Identification Page.

Table 3. DC OPERATING CHARACTERISTICS
(V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Unit
I_{CCR}	Supply Current (Read Mode)	Read, SO open	V_{CC} = 1.7 V, f_{SCK} = 5 MHz		1.5	mA
			V_{CC} = 2.5 V, f_{SCK} = 10 MHz		2	mA
			V_{CC} = 5.5 V, f_{SCK} = 20 MHz		3	mA
I_{CCW}	Supply Current (Write Mode)	Write, CS = V_{CC}	1.7 V < V_{CC} < 5.5 V		2	mA
I_{SB1}	Standby Current	V_{IN} = GND or V_{CC}, CS = V_{CC}, WP = V_{CC}, HOLD = V_{CC}, V_{CC} = 5.5 V			3	μA
I_{SB2}	Standby Current	V_{IN} = GND or V_{CC}, CS = V_{CC}, WP = GND, HOLD = GND, V_{CC} = 5.5 V			5	μA
I_L	Input Leakage Current	V_{IN} = GND or V_{CC}		−2	2	μA
I_{LO}	Output Leakage Current	CS = V_{CC}, V_{OUT} = GND or V_{CC}		−2	2	μA
V_{IL1}	Input Low Voltage	$V_{CC} \ge 2.5$ V		−0.5	0.3 V_{CC}	V
V_{IH1}	Input High Voltage	$V_{CC} \ge 2.5$ V		0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL2}	Input Low Voltage	V_{CC} < 2.5 V		−0.5	0.2 V_{CC}	V
V_{IH2}	Input High Voltage	V_{CC} < 2.5 V		0.8 V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	$V_{CC} \ge 2.5$ V, I_{OL} = 3.0 mA			0.4	V
V_{OH1}	Output High Voltage	$V_{CC} \ge 2.5$ V, I_{OH} = −1.6 mA		V_{CC} −0.8 V		V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL}= 150 μA			0.2	V
V_{OH2}	Output High Voltage	V_{CC} < 2.5 V, I_{OH} = −100 μA		V_{CC} −0.2 V		V
V_{PORth}	Internal Power−On Reset Threshold			0.6	1.5	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. PIN CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V) (Note 4)

Symbol	Test	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output Capacitance (SO)	V_{OUT} = 0 V			8	pF
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	V_{IN} = 0 V			8	pF

4. Determined through qualification/characterization.

Table 5. AC CHARACTERISTICS (Note 5)

Symbol	Parameter	V_{CC} ≤ 2.5 V		V_{CC} = 2.5 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCK}	Clock Frequency	DC	5	DC	10	DC	20	MHz
t_{SU}	Data Setup Time	20		10		5		ns
t_H	Data Hold Time	20		10		5		ns
t_{WH}	SCK High Time	75		40		20		ns
t_{WL}	SCK Low Time	75		40		20		ns
t_{LZ}	HOLD to Output Low Z		50		25		25	ns
t_{RI} (Note 6)	Input Rise Time		2		2		2	µs
t_{FI} (Note 6)	Input Fall Time		2		2		2	µs
t_{HD}	HOLD Setup Time	0		0		0		ns
t_{CD}	HOLD Hold Time	10		10		5		ns
t_V	Output Valid from Clock Low		75		40		20	ns
t_{HO}	Output Hold Time	0		0		0		ns
t_{DIS}	Output Disable Time		50		20		20	ns
t_{HZ}	HOLD to Output High Z		100		25		25	ns
t_{CS}	CS High Time	80		40		20		ns
t_{CSS}	CS Setup Time	60		30		15		ns
t_{CSH}	CS Hold Time	60		30		15		ns
t_{CNS}	CS Inactive Setup Time	60		30		15		
t_{CNH}	CS Inactive Hold Time	60		30		15		
t_{WC} (Note 7)	Write Cycle Time		4		4		4	ms

5. AC Test Conditions:
   Input Pulse Voltages: 0.3 V_{CC} to 0.7 V_{CC} at V_{CC} > 2.5 V, 0.2 V_{CC} to 0.8 V_{CC} at V_{CC} < 2.5 V
   Input rise and fall times: ≤ 10 ns
   Input and output reference voltages: 0.5 V_{CC}
   Output load: current source $I_{OL\ max}/I_{OH\ max}$; C_L = 30 pF
6. This parameter is tested initially and after a design or process change that affects the parameter.
7. t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.

Table 6. POWER−UP TIMING (Notes 6, 8)

Symbol	Parameter	Max	Unit
t_{PUR}	Power−up to Read Operation	0.35	ms
t_{PUW}	Power−up to Write Operation	0.35	ms

8. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Pin Description

SI: The serial data input pin accepts op−codes, addresses and data. In SPI modes (0,0) and (1,1) input data is latched on the rising edge of the SCK clock input.

SO: The serial data output pin is used to transfer data out of the device. In SPI modes (0,0) and (1,1) data is shifted out on the falling edge of the SCK clock.

SCK: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and NV250x0.

$\overline{\text{CS}}$: The chip select input pin is used to enable/disable the NV250x0. When $\overline{\text{CS}}$ is high, the SO output is tri−stated (high impedance) and the device is in Standby Mode (unless an internal write operation is in progress). *Every communication session between host and NV250x0 must be preceded by a high to low transition and concluded with a low to high transition of the $\overline{\text{CS}}$ input.*

$\overline{\text{WP}}$: The write protect input pin will allow all write operations to the device when held high. When $\overline{\text{WP}}$ pin is tied low all write operations are inhibited.

$\overline{\text{HOLD}}$: The $\overline{\text{HOLD}}$ input pin is used to pause transmission between host and NV250x0, without having to retransmit the entire sequence at a later time. To pause, $\overline{\text{HOLD}}$ must be taken low and to resume it must be taken back high, with the SCK input low during both transitions. When not used for pausing, the $\overline{\text{HOLD}}$ input should be tied to V_{CC}, either directly or through a resistor.

Functional Description

The NV250x0 device supports the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8−bit instruction register. The instruction set and associated op−codes are listed in Table 7.

Reading data stored in the NV250x0 is accomplished by simply providing the READ command and an address. Writing to the NV250x0, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the $\overline{\text{CS}}$ input pin, the NV250x0 will accept any one of the six instruction op−codes listed in Table 7 and will ignore all other possible 8−bit combinations. The communication protocol follows the timing from Figure 2.

The NV250x0 features an additional Identification Page (16 bytes) which can be accessed for Read and Write operations when the IPL bit from the Status Register is set to “0”. The user can also choose to make the Identification Page permanent write protected.

Table 7. INSTRUCTION SET

Instruction	Op−code	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

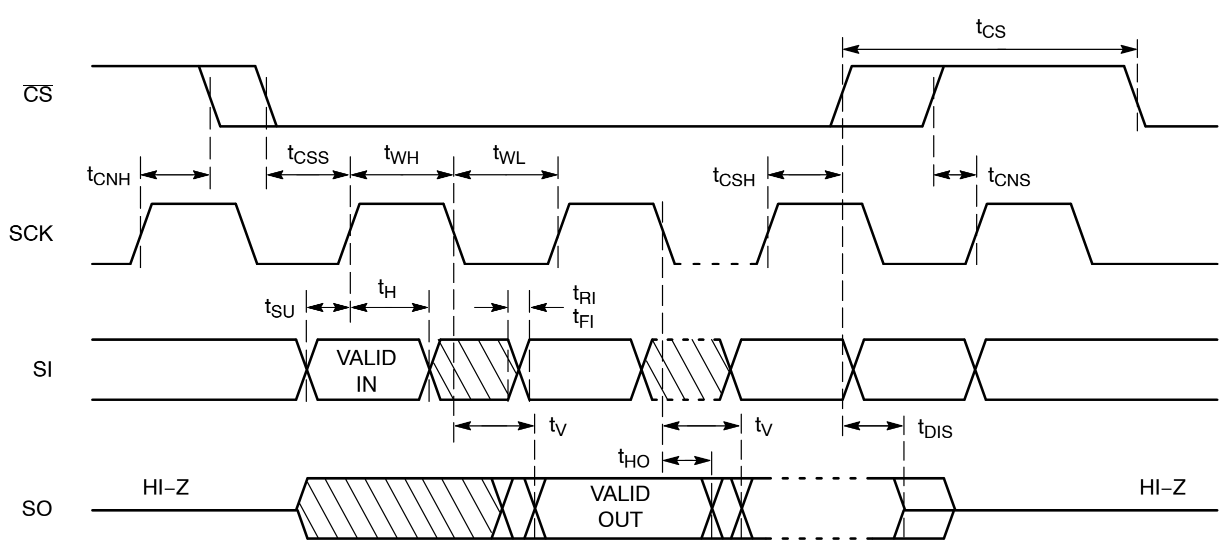


Figure 2. Synchronous Data Timing

Status Register

The Status Register, as shown in Table 8, contains a number of status and control bits.

The $\overline{RDY}$ (Ready) bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

The WEL (Write Enable Latch) bit is set/reset by the WREN/WRDI commands. When set to 1, the device is in a Write Enable state and when set to 0, the device is in a Write Disable state.

The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non−volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 9. The protected blocks then become read−only.

The IPL (Identification Page Latch) bit determines whether the additional Identification Page (IPL = 0) or main memory array (IPL = 1) can be accessed both for Read and Write operations. The IPL bit is set by the user with the WRSR command and is volatile. The IPL bit is automatically set to 1 after read/write operations. The LIP (Lock Identification Page) bit is set by the user with the WRSR command and is non−volatile. When set to 0, the Identification Page is permanently write protected (locked in Read−only mode).

Note: *The IPL and LIP bits cannot be set to 0 using the same WRSR instruction. If the user attempts to set (“0”) both the IPL and LIP bit in the same time, these bits cannot be written and therefore they will remain unchanged.*

Table 8. STATUS REGISTER

7	6	5	4	3	2	1	0
1	IPL	1	LIP	BP1	BP0	WEL	$\overline{RDY}$

Table 9. BLOCK PROTECTION BITS

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	NV25010LV: 060−07F, NV25020LV: 0C0−0FF, NV25040LV: 180−1FF	Quarter Array Protection
1	0	NV25010LV: 040−07F, NV25020LV: 080−0FF, NV25040LV: 100−1FF	Half Array Protection
1	1	NV25010LV: 000−07F, NV25020LV: 000−0FF, NV25040LV: 000−1FF	Full Array Protection

Table 10. WRITE PROTECT CONDITIONS

$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
Low	X	Protected	Protected	Protected
High	0	Protected	Protected	Protected
High	1	Protected	Writable	Writable

WRITE OPERATIONS

The NV250x0 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

Write Enable and Write Disable

The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN instruction to the NV250x0. Care must be taken to take the $\overline{CS}$ input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 3. The WREN instruction must be sent prior to any WRITE or WRSR instruction.

The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 4. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

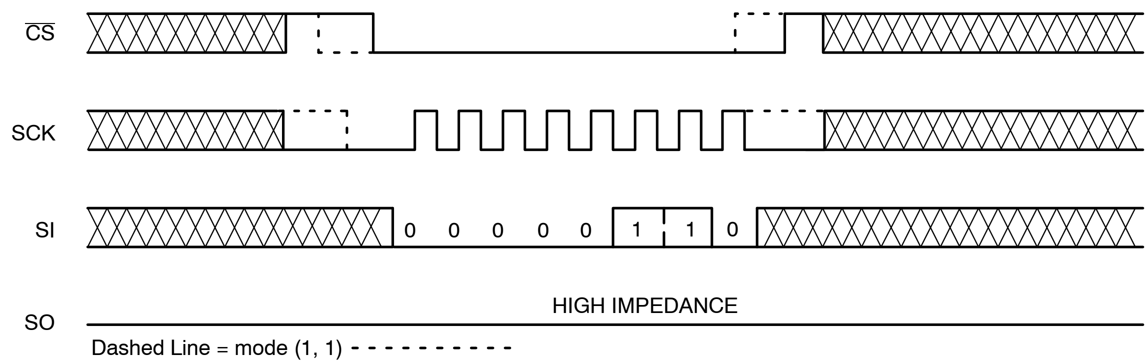


Figure 3. WREN Timing

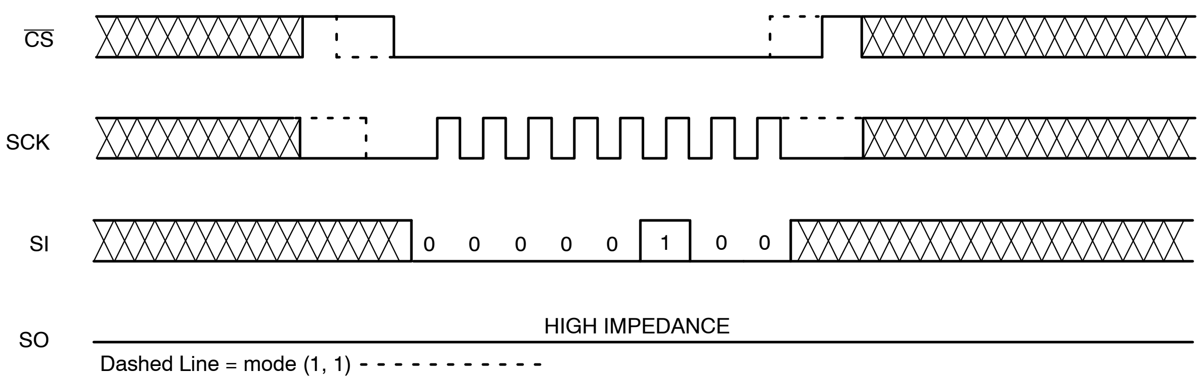


Figure 4. WRDI Timing

Byte Write

Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, an 8−bit address and data as shown in Figure 5. For the NV25040LV, bit 3 of the write instruction opcode contains A8 address bit. Internal programming will start after the low to high $\overline{CS}$ transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The $\overline{RDY}$ bit will indicate if the internal write cycle is in progress ($\overline{RDY}$ high), or the device is ready to accept commands ($\overline{RDY}$ low).

Page Write

After sending the first data byte to the NV250x0, the host may continue sending data, up to a total of 16 bytes, according to timing shown in Figure 6. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will "roll over" to the first byte in the page, thus possibly overwriting previously loaded data. Following completion of the write cycle, the NV250x0 is automatically returned to the write disable state.

Write Identification Page

The additional 16−byte Identification Page (IP) can be written with user data using the same Write commands sequence as used for Page Write to the main memory array (Figure 6). **The IPL bit from the Status Register must be set to 0 using the WRSR instruction, before attempting to write to the IP.** The address bits [A8:A4] are Don't Care and the [A3:A0] bits define the byte address within the Identification Page. In addition, the Byte Address must point to a location outside the protected area defined by the BP1, BP0 bits from the Status Register. When the full memory array is write protected (BP1, BP0 = 1,1), the write instruction to the IP is not accepted and not executed. Also, the write to the IP is not accepted if the LIP bit from the Status Register is set to 0 (the page is locked in Read−only mode).

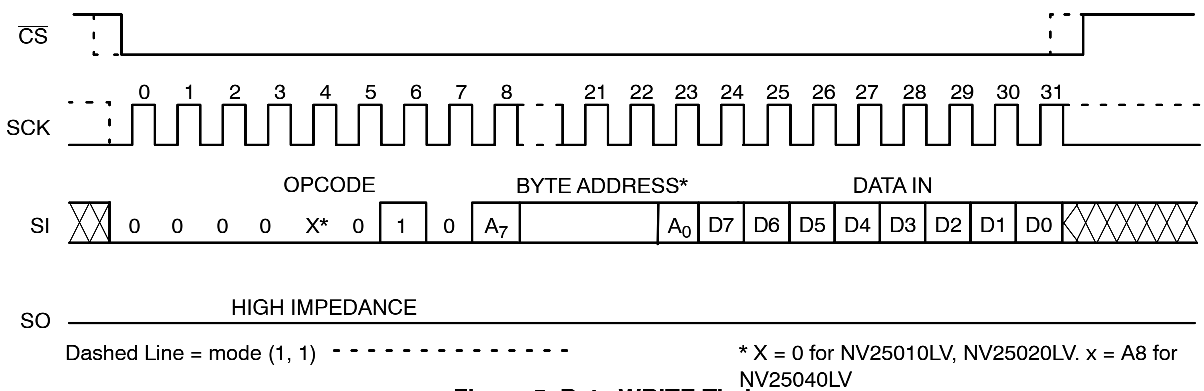


Figure 5. Byte WRITE Timing

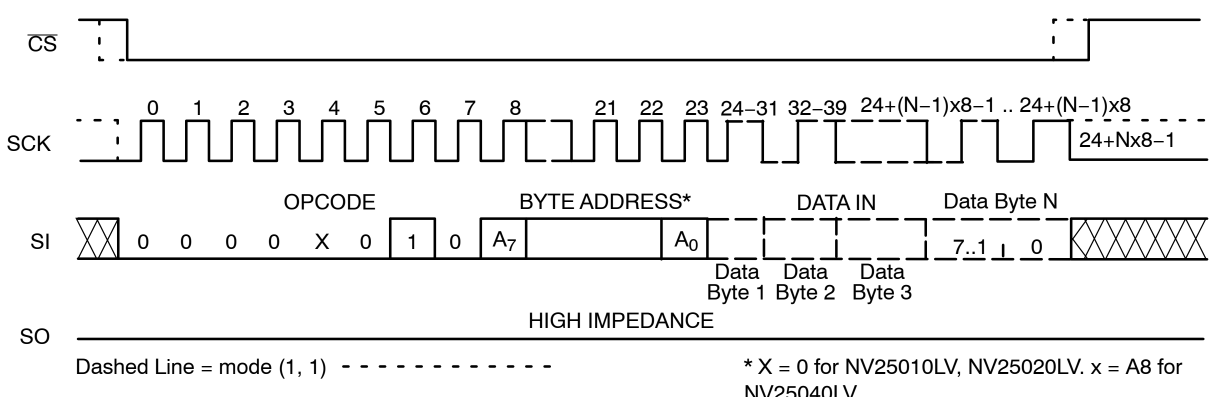


Figure 6. Page WRITE Timing

Write Status Register

The Status Register is written by sending a WRSR instruction according to timing shown in Figure 7. Only bits 2, 3, 4 and 6 can be written using the WRSR command.

Write Protection

When $\overline{WP}$ input is low all write operations to the memory array and Status Register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write operation. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the Status Register or memory array.

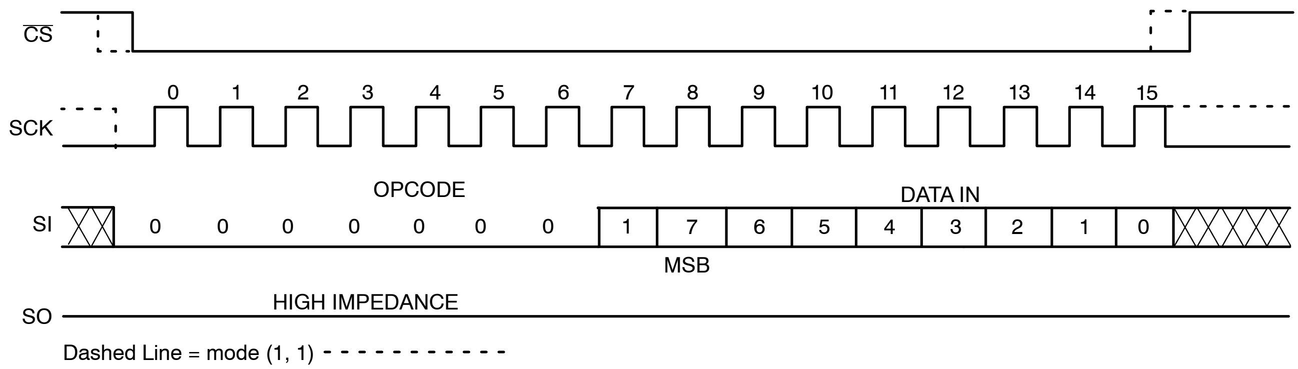


Figure 7. WRSR Timing

READ OPERATIONS

Read from Memory Array

To read from memory, the host sends a READ instruction followed by a 8−bit address (for the NV25040LV, bit 3 of the read instruction opcode contains A8 address bit).

After receiving the last address bit, the NV250x0 will respond by shifting out data on the SO pin (as shown in Figure 8). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter "rolls over" to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Read Status Register

To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the NV250x0 will shift out the contents of the status register on the SO pin (Figure 9). The status register may be read at any time, including during an internal write cycle. While the internal write cycle is in progress, the RDSR command will output the full content of the status register. For easy detection of the internal write cycle completion, we recommend sampling the RDY bit only through the polling routine. After detecting the RDY bit "0", the next RDSR instruction will always output the expected content of the status register.

Read Identification Page

Reading the additional 16−byte Identification Page (IP) is achieved using the same Read command sequence as used for Read from main memory array (Figure 8). **The IPL bit from the Status Register must be set to 0 before attempting to read from the IP.** The [A3:A0] are the address significant bits that point to the data byte shifted out on the SO pin. If the CS continues to be held low, the internal address register defined by [A3:A0] bits is automatically incremented and the next data byte from the IP is shifted out. The byte address must not exceed the 16−byte page boundary.

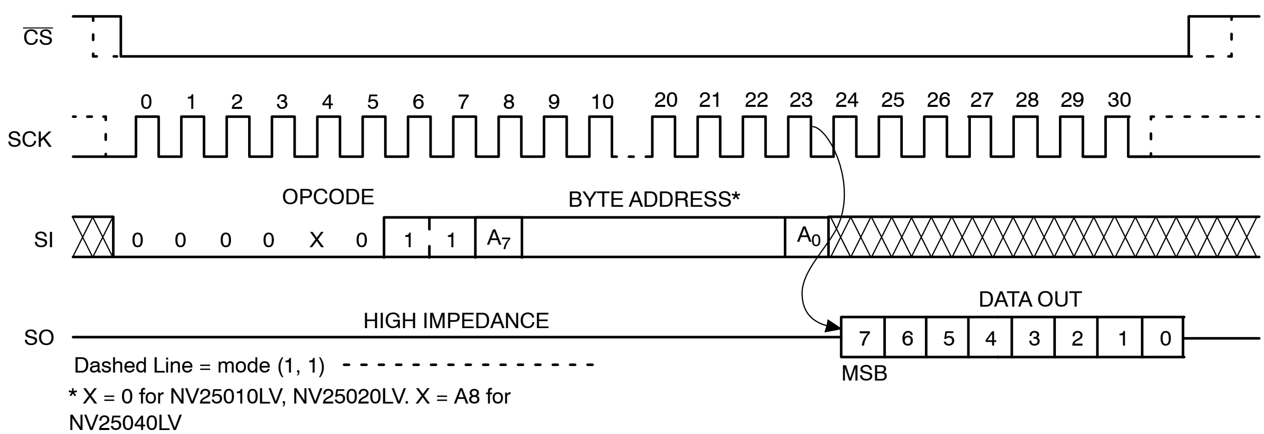


Figure 8. READ Timing

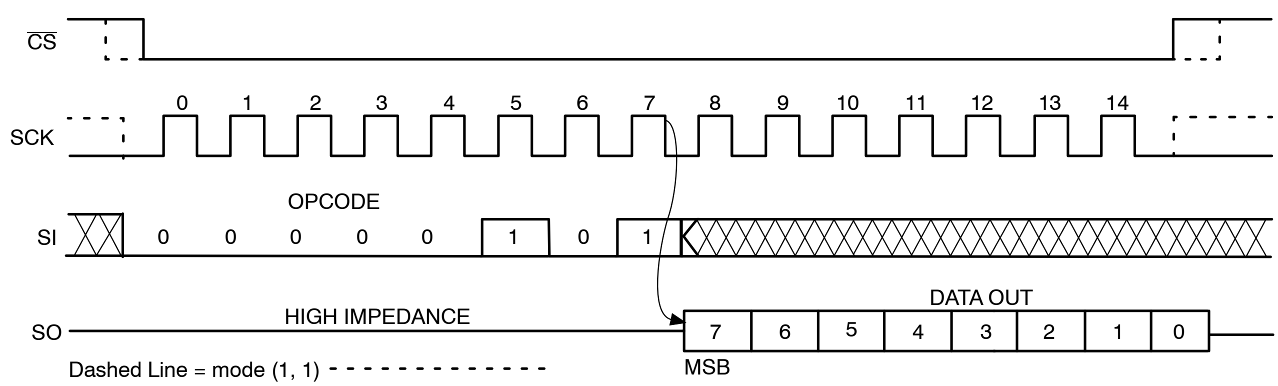


Figure 9. RDSR Timing

Hold Operation

The $\overline{HOLD}$ input can be used to pause communication between host and NV250x0. To pause, $\overline{HOLD}$ must be taken low while SCK is low (Figure 10). During the hold condition the device must remain selected ($\overline{CS}$ low). During the pause, the data output pin (SO) is tri−stated (high impedance) and SI transitions are ignored. To resume communication, $\overline{HOLD}$ must be taken high while SCK is low.

Design Considerations

The NV250x0 device incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR behavior protects the device against ‘brown−out’ failure following a temporary loss of power.

The NV250x0 device powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior to any writes to the device.

After power up, the $\overline{CS}$ pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The $\overline{CS}$ input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid op−code will be ignored and the serial output pin (SO) will remain in the high impedance state.

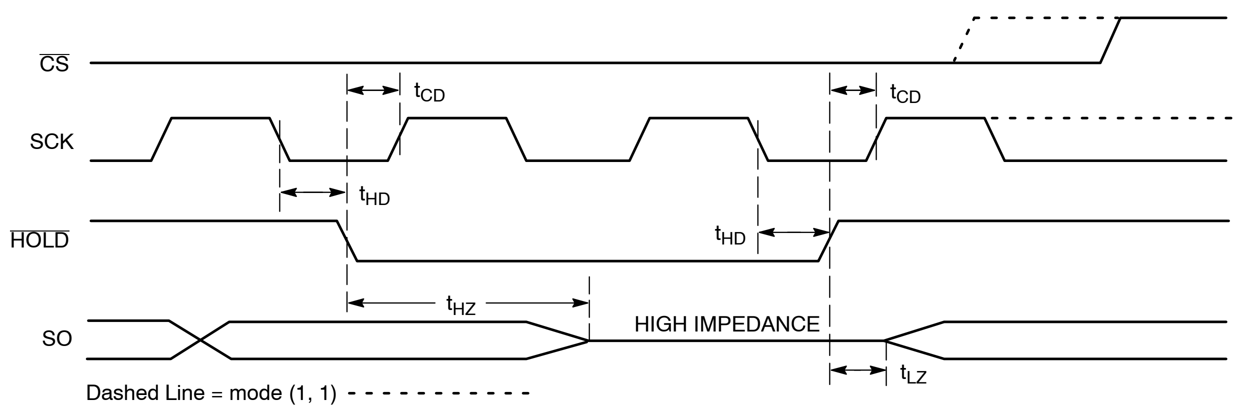


Figure 10. $\overline{HOLD}$ Timing

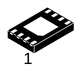
Error Correction Code

The NV250x0 incorporates on−board Error Correction Code (ECC) circuitry, which makes it possible to detect and correct one faulty bit in a byte. ECC improves data reliability by correcting random single bit failures that might occur over the life of the device.

ORDERING INFORMATION (Notes 9, 10)

OPN	Density	Automotive Grade	Package Type	Shipping†
NV25010DTVLT3G	1 kb	Grade 1 (−40°C to +125°C)	TSSOP−8 (Pb−Free)	3000 / Tape & Reel
NV25010DWVLT3G	1 kb	Grade 1 (−40°C to +125°C)	SOIC−8 (Pb−Free)	3000 / Tape & Reel
NV25010MUW3VLT3G*	1 kb	Grade 1 (−40°C to +125°C)	UDFN−8 (Pb−Free) Wettable Flank	3000 / Tape & Reel
NV25010UVLT2G*	1 kb	Grade 1 (−40°C to +125°C)	US8 (Pb−Free)	3000 / Tape & Reel
NV25020DTVLT3G	2 kb	Grade 1 (−40°C to +125°C)	TSSOP−8 (Pb−Free)	3000 / Tape & Reel
NV25020DWVLT3G	2 kb	Grade 1 (−40°C to +125°C)	SOIC−8 (Pb−Free)	3000 / Tape & Reel
NV25020MUW3VLT3G*	2 kb	Grade 1 (−40°C to +125°C)	UDFN−8 (Pb−Free) Wettable Flank	3000 / Tape & Reel
NV25020UVLT2G*	2 kb	Grade 1 (−40°C to +125°C)	US8 (Pb−Free)	3000 / Tape & Reel
NV25040DTVLT3G	4 kb	Grade 1 (−40°C to +125°C)	TSSOP−8 (Pb−Free)	3000 / Tape & Reel
NV25040DWVLT3G	4 kb	Grade 1 (−40°C to +125°C)	SOIC−8 (Pb−Free)	3000 / Tape & Reel
NV25040MUW3VLT3G*	4 kb	Grade 1 (−40°C to +125°C)	UDFN−8 (Pb−Free) Wettable Flank	3000 / Tape & Reel
NV25040UVLT2G*	4 kb	Grade 1 (−40°C to +125°C)	US8 (Pb−Free)	3000 / Tape & Reel

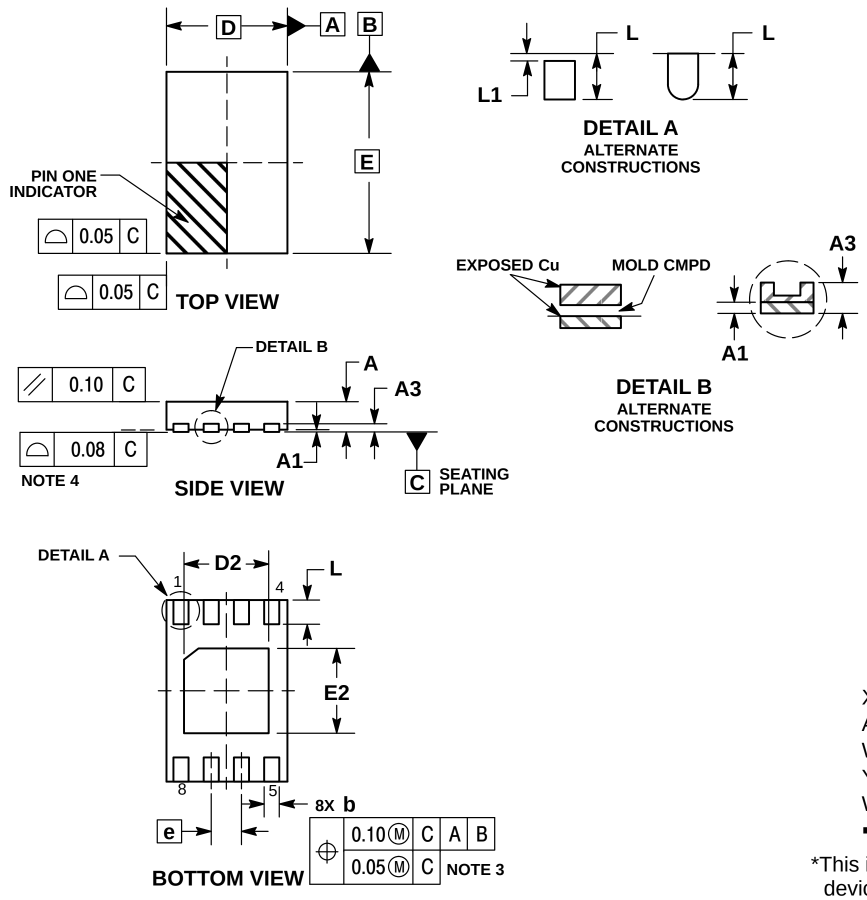
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Product in development.
9. All packages are RoHS−compliant (Pb−Free, Halogen−free).
10. The standard lead finish is NiPdAu.



SCALE 2:1

UDFN8 2x3, 0.5P
CASE 517DH
ISSUE O

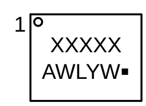
DATE 06 NOV 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.30	1.50
e	0.50 BSC	
L	0.30	0.50
L1	---	0.15

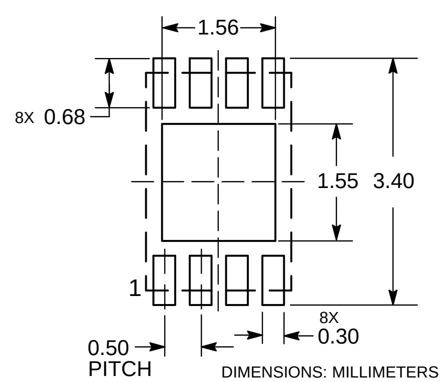
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON06579G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
REFERENCE:		
DESCRIPTION:	UDFN8 2X3, 0.5P	PAGE 1 OF 2

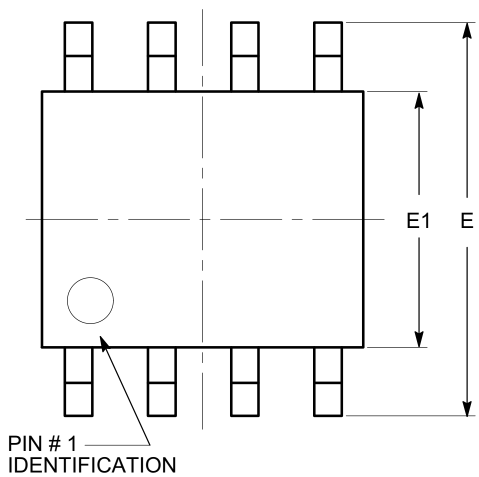
ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY I. HYLAND.	06 NOV 2015

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

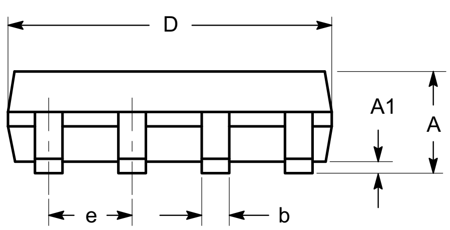
SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

DATE 19 DEC 2008

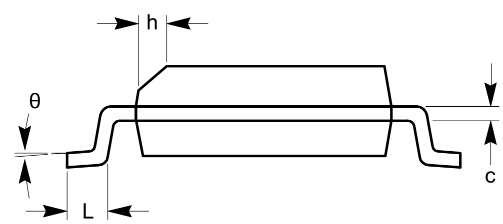


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



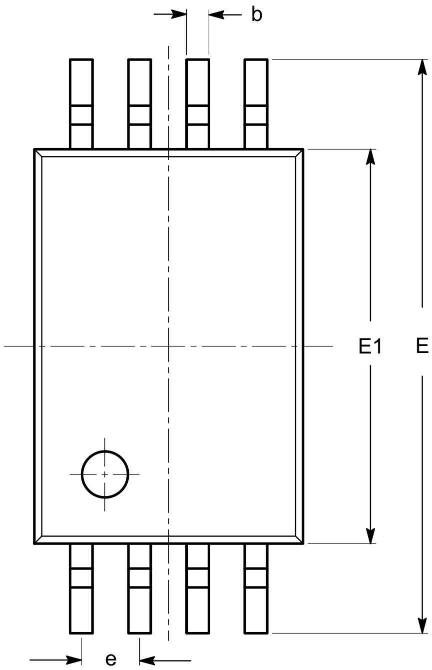
END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM POD #SOIC8−002−01 TO ON SEMICONDUCTOR. REQ. BY B. BERGMAN.	19 DEC 2008

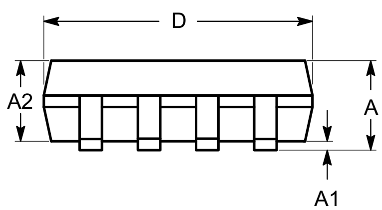
TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

DATE 19 DEC 2008

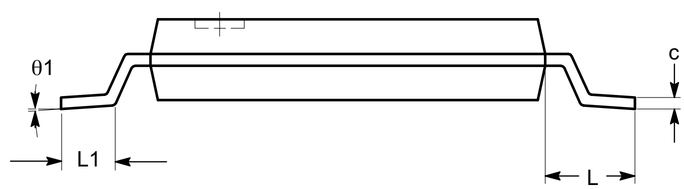


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW

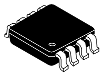


END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

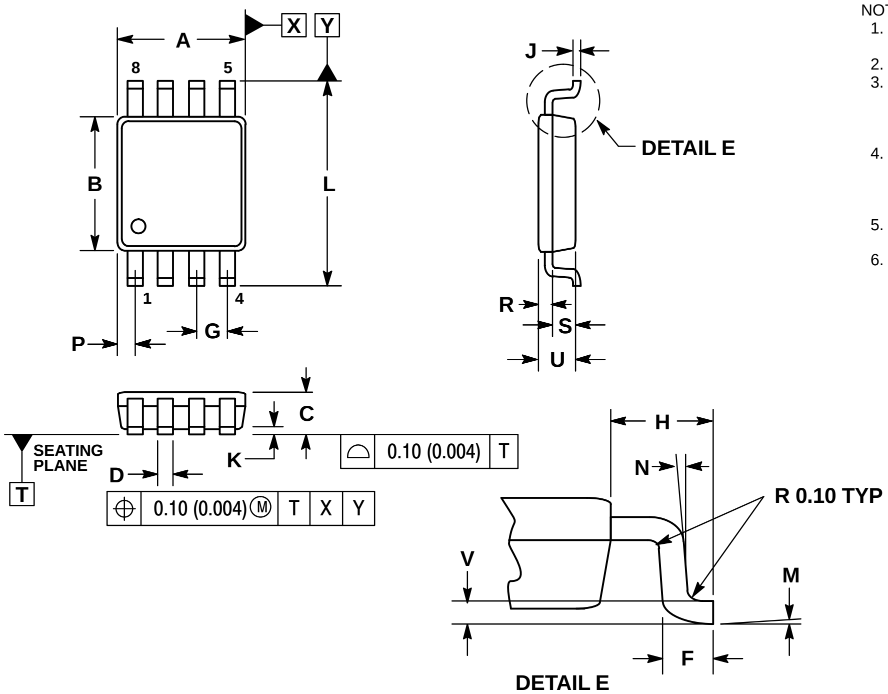
ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM POD #TSSOP8−004−01 TO ON SEMICONDUCTOR. REQ. BY B. BERGMAN.	19 DEC 2008



SCALE 4 :1

US8
CASE 493
ISSUE D

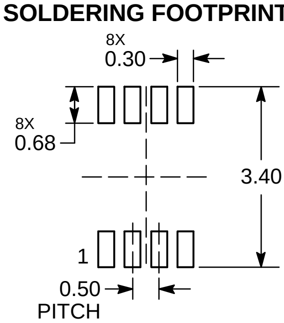
DATE 15 JUL 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.14MM (0.0055”) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14MM (0.0055”) PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076−0.0203MM (0.003−0.008”).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508MM (0.0002”).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.128
M	0 °	6 °	0 °	6 °
N	0 °	10 °	0 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

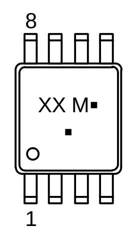
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

DOCUMENT NUMBER:	98AON04475D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	US8		PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ BY R. FORNESS	19 MAR 2001
A	CHANGED DIM “P” TO 0.23 MM MIN, 0.34 MM MAX AND 0.010 IN MIN, 0.013 IN MAX. REQ BY J. MILLER	25 JUN 2003
B	ADDED SOLDERING FOOTPRINT. REQ. BY D. TRUHITTE.	13 APR 2006
C	MODIFIED SOLDERING FOOTPRINT. REQ. BY B. BECKER.	23 MAR 2015
D	MODIFIED DIMENSION A MIN VALUE AND DIMENSION C MAX VALUE FOR MM. REQ. BY R. AVILA.	15 JUL 2015

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

◊