NVC5C426NK8

Single N-Channel Power MOSFET

40 V, 1.3 mΩ

Description

This Known Good Die N−Channel Power MOSFET is manufactured using the innovative Trench process. This advance technology has been tailored to minimize conduction loss. Low Qg and Capacitance minimizes driver losses.

Features

- Typical $R_{DS(on)}$ = 0.92 mΩ at V_{GS} = 10 V; I_D = 20 A
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

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Gate and Source: AlCu
Drain: Ti/Ni/Ag (back side of die)
Passivation: Polyimide
Wafer Diameter: 8 inch

DIMENSION (μm)

Die Size (Typical, L x W)	3671 x 2163
Die Size (Length) Die Size (Width)	Min: 3661, Max: 3680 Min: 2155, Max: 2171
Source Attach Area	2945 x 1477
Gate Attach Area	200 x 200
Die Thickness	76.2 ± 12

ORDERING INFORMATION

Device	Package	Shipping†
NVC5C426NK8	KGD on Tape	Max of 3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40% to 66%

The Chip is 100% tested as Known Good Die (KGD) to Meet the Conditions and Limits Specified below at Tc = 25°C.

Symbol	Parameter		Min	Typ	Max	Units
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy	L = 0.1 mH, I_{D} = 56 A	157	_	_	mJ
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA	40	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V	–	–	10	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 20 A, V_{GS} = 0 V	–	–	1.2	V
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	–	3.5	V
* $R_{DS(on)}$	Bare Die Drain to Source On Resistance	I_D = 20 A, V_{GS} = 10 V	–	0.92	1.3	mΩ

*Accurate $R_{DS(on)}$ test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max $R_{DS(on)}$ specification is defined from the historical performance of the die in package but is not guaranteed by test in production.

ABSOLUTE MAXIMUM RATINGS in Reference to the NVMFS5C426N electrical data in SO−8FL (T_J = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		40	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	T_C = 25°C	235	A
		T_C = 100°C	166	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	T_C = 25°C	128	W
		T_C = 100°C	64	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	T_C = 25°C	41	A
		T_C = 100°C	29	A
P_D	Power Dissipation $R_{\theta JA}$ (Note 1 & 2)	T_C = 25°C	3.8	W
		T_C = 100°C	1.9	W
I_{DM}	Pulsed Drain Current T_A = 25°C, tp = 10 us		900	A
T_J, T_{STG}	Operating and Storage Temperature (NVMFS5C426N)		−55 to +175	°C
IS	Source Current (Body Diode)		122	A
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy (IL(pk) = 19 A)		739	mJ
$R_{\theta JC}$	Thermal Resistance (Junction to Case Steady State)		1.2	°C/W
$R_{\theta JA}$	Thermal Resistance (Junction to Ambient) Steady State (Note 2)		39	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle

ELECTRICAL CHARACTERISTICS in Reference to the NVMFS5C426N electrical data in SO−8FL (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		40	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 40 V, V_{GS} = 0 V	T_J = 25°C	–	–	10	μA
			T_J = 125°C	–	–	100	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20V		–	–	100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.5	–	3.5	V
$r_{DS(on)}$	Drain to Source On−Resistance	I_D = 50 A, V_{GS} = 10 V		–	1.1	1.3	mΩ
gFS	Forward Transconductance	V_{DS} =15 V, I_D = 50 A		–	145	–	S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		–	4300	–	pF
C_{oss}	Output Capacitance			–	2100	–	pF
C_{rss}	Reverse Transfer Capacitance			–	59	–	pF
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 50 A		–	65	–	nC
$Q_{g(th)}$	Threshold Gate Charge			–	13	–	
Q_{gs}	Gate to Source Gate Charge			–	20	–	
Q_{gd}	Reverse Transfer Capacitance			–	12	–	
VGP	Plateau Voltage			–	4.7	–	V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(on)}$	Turn−On Delay Time	V_{DS} = 20 V, I_D = 50 A, V_{GS} = 10 V, R_G = 2.5 Ω		–	15	–	ns
t_r	Turn−On Rise Time			–	47	–	ns
$t_{d(off)}$	Turn−Off Delay Time			–	36	–	ns
t_f	Turn−Off Fall Time			–	9	–	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 50 A, V_{GS} = 0 V		–	–	1.2	V
T_{rr}	Reverse Recovery Time	I_{SD} = 50 A, dI_{SD}/dt = 100 A/μs		–	63	-	ns
Q_{rr}	Reverse Recovery Charge			–	92	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

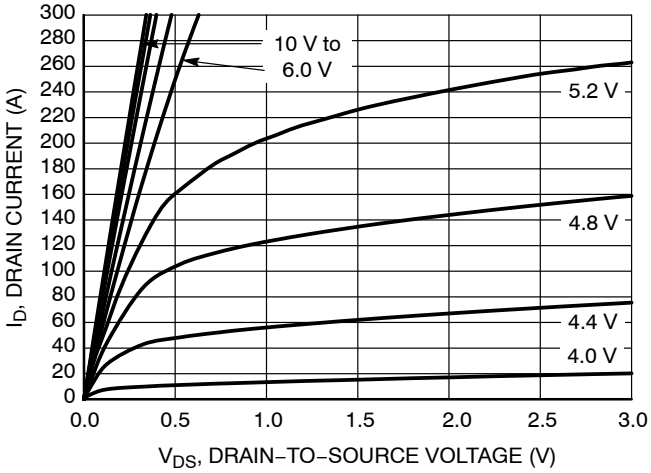


Figure 1. On−Region Characteristics

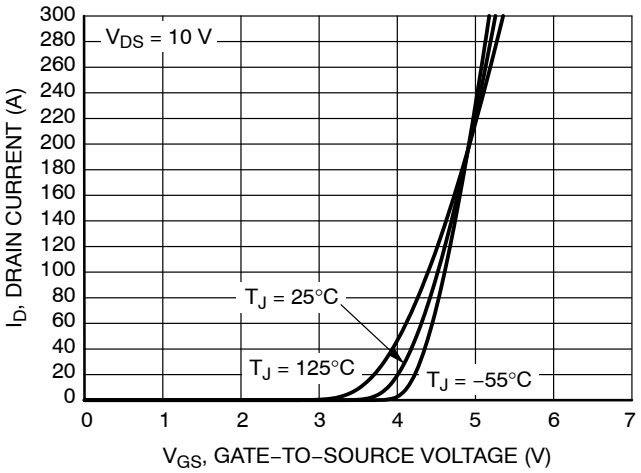


Figure 2. Transfer Characteristics

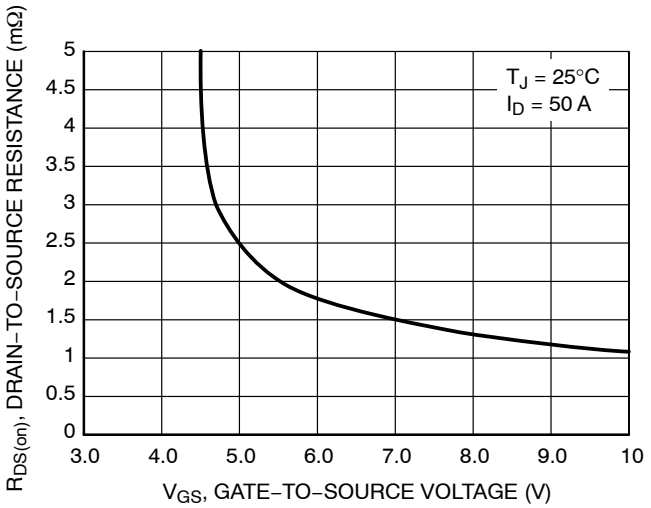


Figure 3. On−Resistance vs. Gate−to−Source Voltage

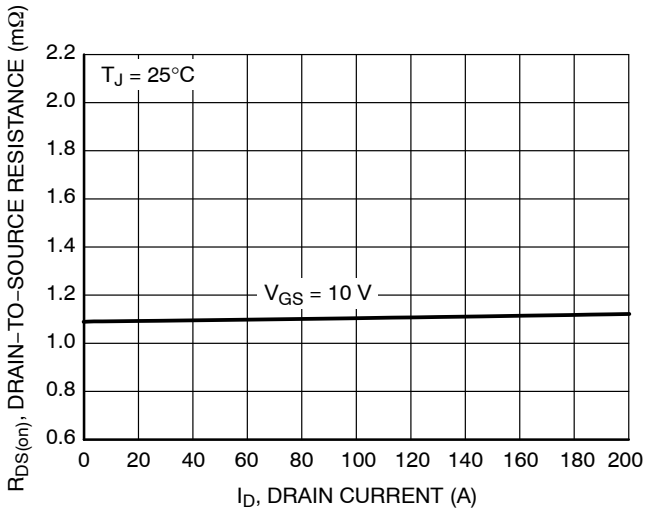


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

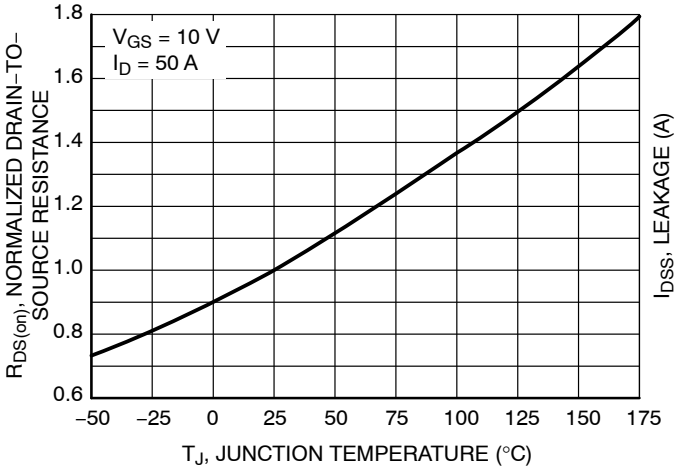


Figure 5. On−Resistance Variation with Temperature

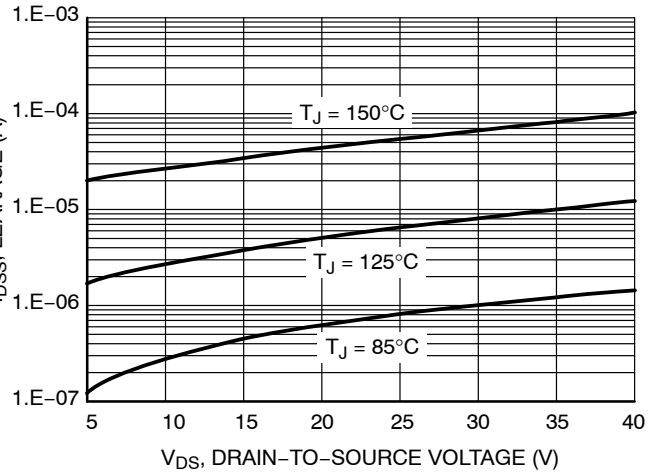


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

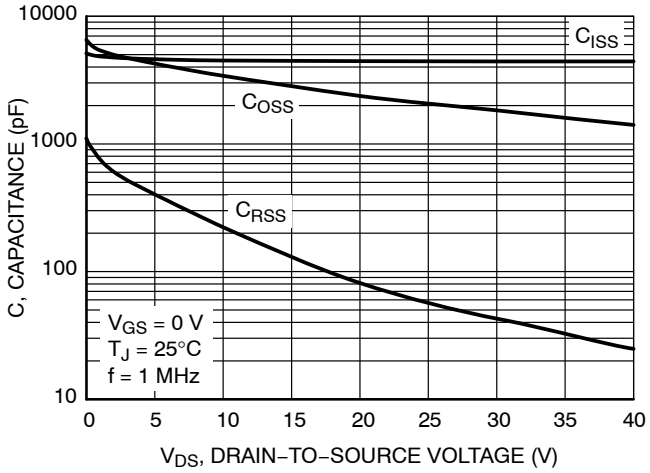


Figure 7. Capacitance Variation

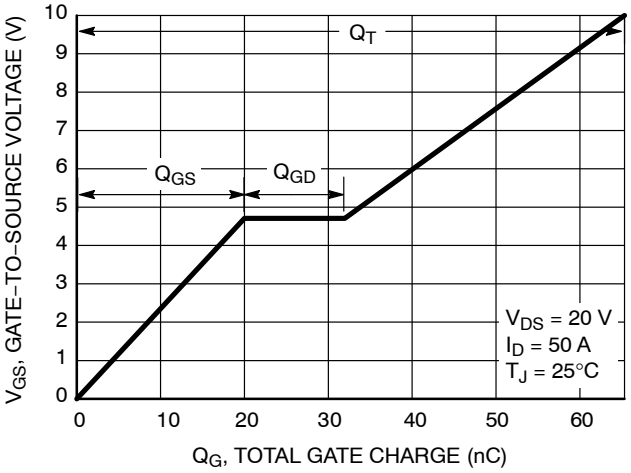


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

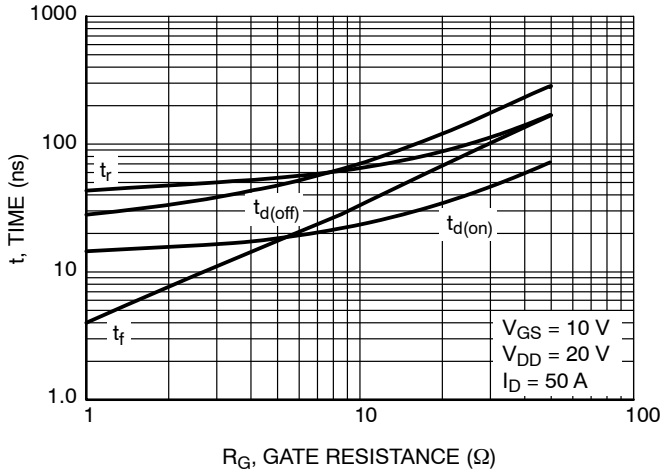


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

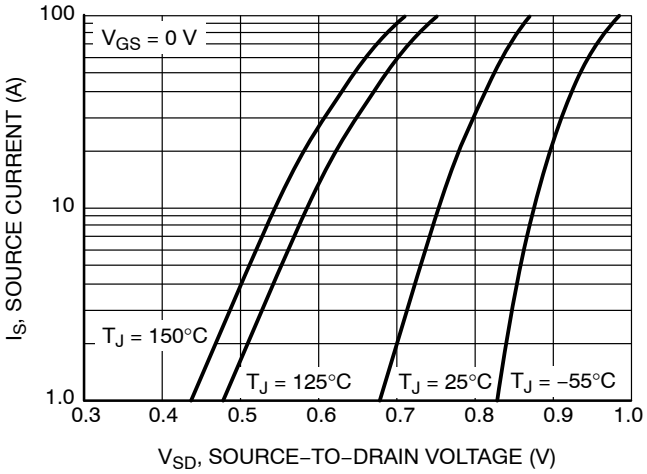


Figure 10. Diode Forward Voltage vs. Current

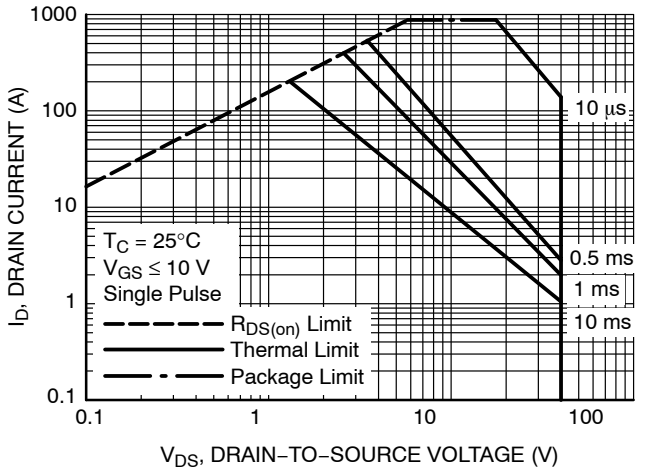


Figure 11. Safe Operating Area

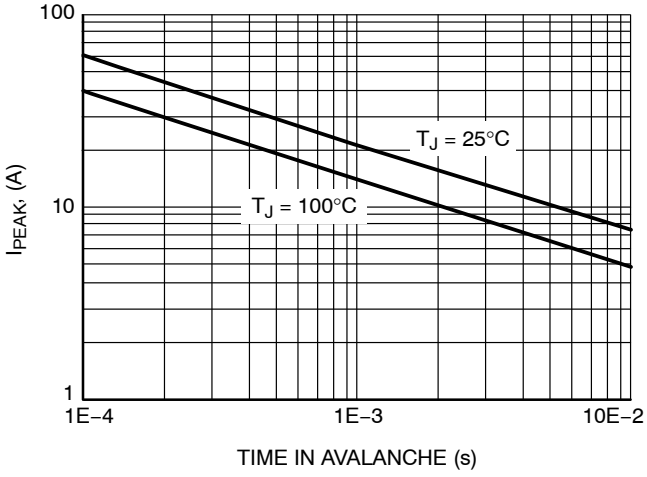


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

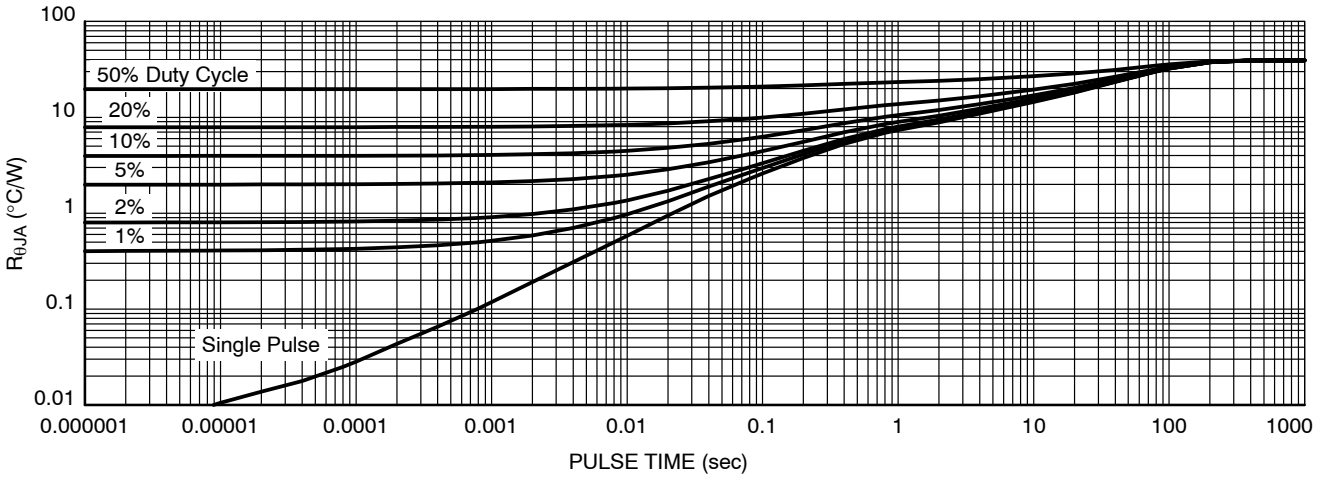
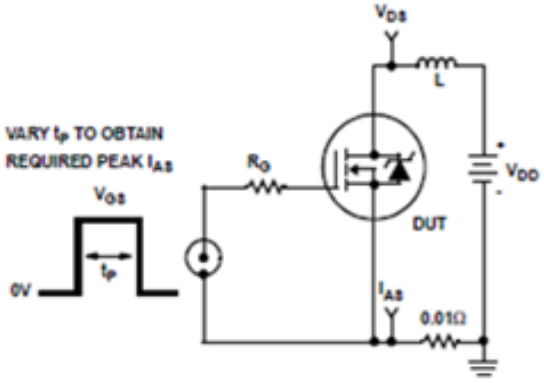
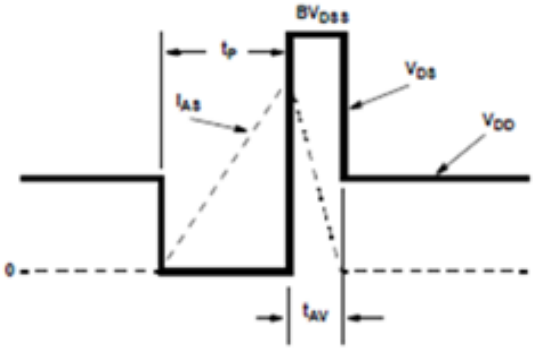


Figure 13. Thermal Characteristics

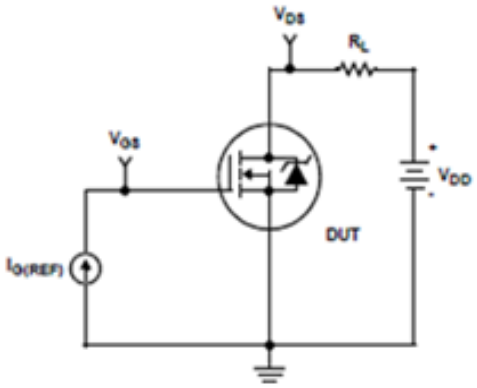
Test Circuits and Waveforms



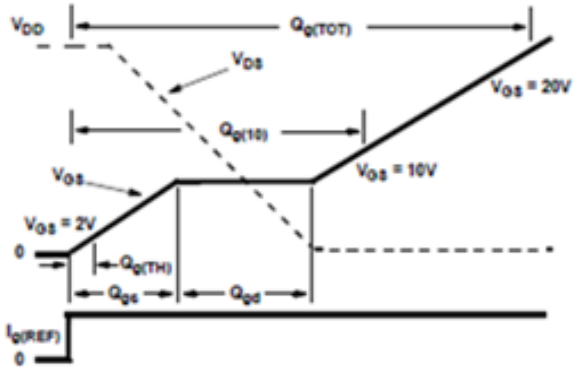
UNCLAMPED ENERGY TEST CIRCUIT



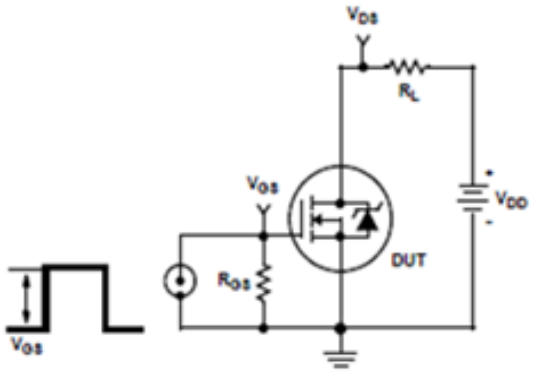
UNCLAMPED ENERGY WAVEFORMS



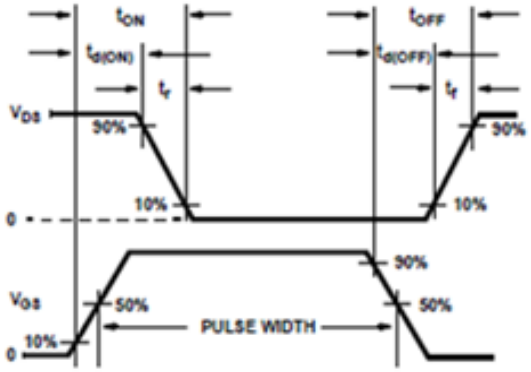
GATE CHARGE TEST CIRCUIT



GATE CHARGE WAVEFORM



SWITCHING TIME TEST CIRCUIT



RESISTIVE SWITCHING WAVEFORMS

PUBLICATION ORDERING INFORMATION

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