

NVC5C426NK8

Single N-Channel Power MOSFET

40 V, 1.3 m Ω

Description

This Known Good Die N-Channel Power MOSFET is manufactured using the innovative Trench process. This advance technology has been tailored to minimize conduction loss. Low Qg and Capacitance minimizes driver losses.

Features

- Typical $R_{DS(on)} = 0.92 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$; $I_D = 20 \text{ A}$
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant



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Gate and Source: AlCu
Drain: Ti/Ni/Ag (back side of die)
Passivation: Polyimide
Wafer Diameter: 8 inch

DIMENSION (μm)

Die Size (Typical, L x W)	3671 x 2163
Die Size (Length)	Min: 3661, Max: 3680
Die Size (Width)	Min: 2155, Max: 2171
Source Attach Area	2945 x 1477
Gate Attach Area	200 x 200
Die Thickness	76.2 \pm 12

ORDERING INFORMATION

Device	Package	Shipping [†]
NVC5C426NK8	KGD on Tape	Max of 3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40% to 66%

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The Chip is 100% tested as Known Good Die (KGD) to Meet the Conditions and Limits Specified below at $T_c = 25^\circ\text{C}$.

Symbol	Parameter	Min	Typ	Max	Units	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy	$L = 0.1 \text{ mH}, I_D = 56 \text{ A}$	157	-	-	mJ
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	10	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	100	nA
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 20 \text{ A}, V_{GS} = 0 \text{ V}$	-	-	1.2	V
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.5	-	3.5	V
* $R_{DS(on)}$	Bare Die Drain to Source On Resistance	$I_D = 20 \text{ A}, V_{GS} = 10 \text{ V}$	-	0.92	1.3	$\text{m}\Omega$

*Accurate $R_{DS(on)}$ test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max $R_{DS(on)}$ specification is defined from the historical performance of the die in package but is not guaranteed by test in production.

ABSOLUTE MAXIMUM RATINGS in Reference to the NVMFS5C426N electrical data in SO-8FL ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Units	
V_{DSS}	Drain to Source Voltage	40	V	
V_{GS}	Gate to Source Voltage	± 20	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	$T_C = 25^\circ\text{C}$	235	A
		$T_C = 100^\circ\text{C}$	166	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 25^\circ\text{C}$	128	W
		$T_C = 100^\circ\text{C}$	64	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	$T_C = 25^\circ\text{C}$	41	A
		$T_C = 100^\circ\text{C}$	29	A
P_D	Power Dissipation $R_{\theta JA}$ (Note 1 & 2)	$T_C = 25^\circ\text{C}$	3.8	W
		$T_C = 100^\circ\text{C}$	1.9	W
I_{DM}	Pulsed Drain Current $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	900	A	
T_J, T_{STG}	Operating and Storage Temperature (NVMFS5C426N)	-55 to +175	$^\circ\text{C}$	
IS	Source Current (Body Diode)	122	A	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_L(pk) = 19 \text{ A}$)	739	mJ	
$R_{\theta JC}$	Thermal Resistance (Junction to Case Steady State)	1.2	$^\circ\text{C}/\text{W}$	
$R_{\theta JA}$	Thermal Resistance (Junction to Ambient) Steady State (Note 2)	39	$^\circ\text{C}/\text{W}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle

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ELECTRICAL CHARACTERISTICS in Reference to the NVMFS5C426N electrical data in SO-8FL ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
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OFF CHARACTERISTICS

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}$	40	-	-	V	
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 40 \text{V}, V_{GS} = 0 \text{V}$	$T_J = 25^\circ\text{C}$	-	-	10	μA
			$T_J = 125^\circ\text{C}$	-	-	100	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = 20\text{V}$	-	-	100	nA	

ON CHARACTERISTICS (Note 4)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.5	-	3.5	V
$r_{DS(on)}$	Drain to Source On-Resistance	$I_D = 50 \text{A}, V_{GS} = 10 \text{V}$	-	1.1	1.3	$\text{m}\Omega$
gFS	Forward Transconductance	$V_{DS} = 15 \text{V}, I_D = 50 \text{A}$	-	145	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{V}, V_{GS} = 0 \text{V}, f = 1 \text{MHz}$	-	4300	-	pF
C_{oss}	Output Capacitance		-	2100	-	pF
C_{rss}	Reverse Transfer Capacitance		-	59	-	pF
$Q_{g(tot)}$	Total Gate Charge	$V_{GS} = 10 \text{V}, V_{DS} = 20 \text{V}, I_D = 50 \text{A}$	-	65	-	nC
$Q_{g(th)}$	Threshold Gate Charge		-	13	-	
Q_{gs}	Gate to Source Gate Charge		-	20	-	
Q_{gd}	Reverse Transfer Capacitance		-	12	-	
VGP	Plateau Voltage		-	4.7	-	V

SWITCHING CHARACTERISTICS (Note 5)

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 20 \text{V}, I_D = 50 \text{A}, V_{GS} = 10 \text{V}, R_G = 2.5 \Omega$	-	15	-	ns
t_r	Turn-On Rise Time		-	47	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	36	-	ns
t_f	Turn-Off Fall Time		-	9	-	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 50 \text{A}, V_{GS} = 0 \text{V}$	-	-	1.2	V
T_{rr}	Reverse Recovery Time	$I_{SD} = 50 \text{A}, dI_{SD}/dt = 100 \text{A}/\mu\text{s}$	-	63	-	ns
Q_{rr}	Reverse Recovery Charge		-	92	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

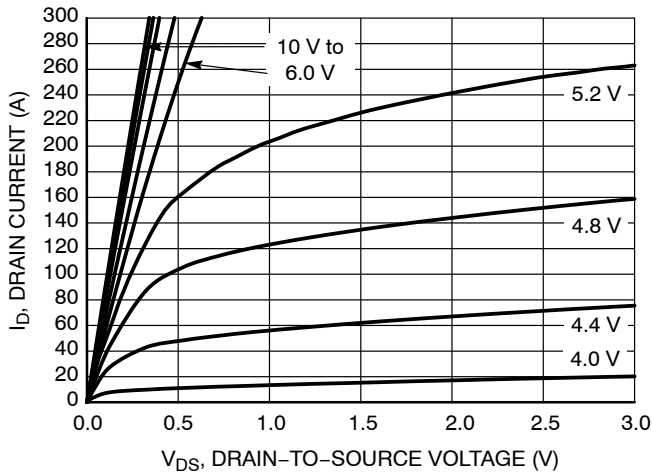


Figure 1. On-Region Characteristics

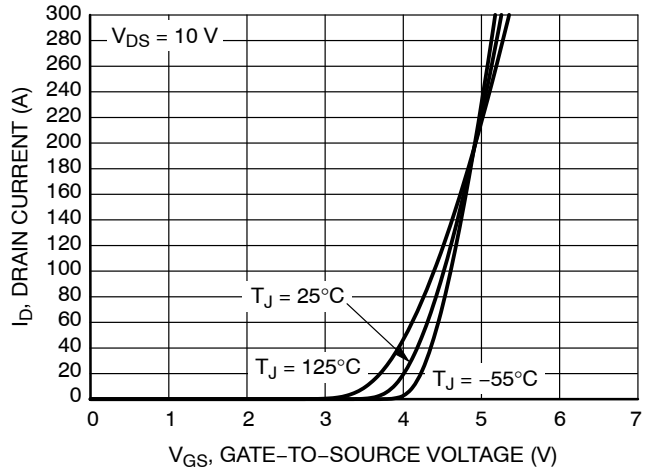


Figure 2. Transfer Characteristics

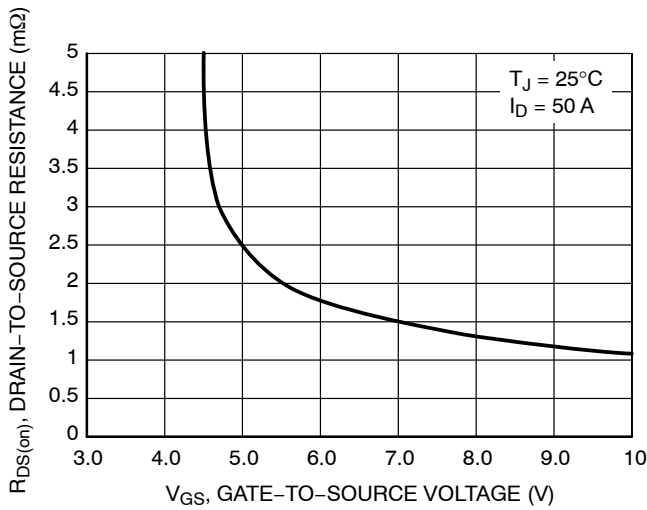


Figure 3. On-Resistance vs. Gate-to-Source Voltage

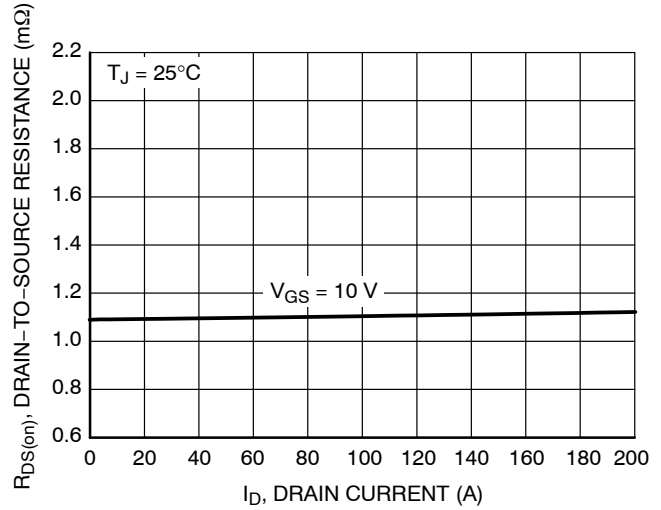


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

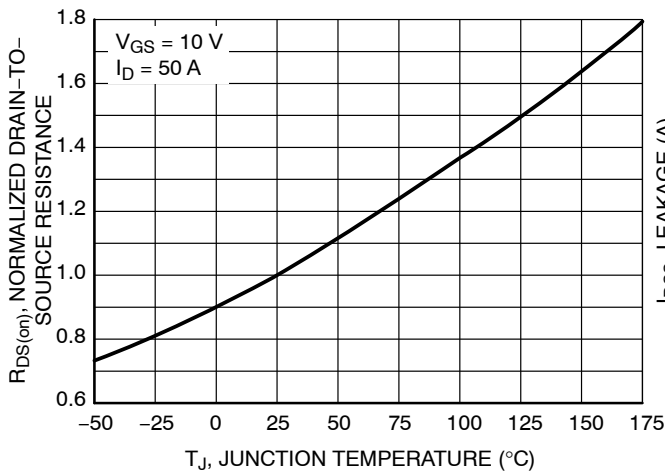


Figure 5. On-Resistance Variation with Temperature

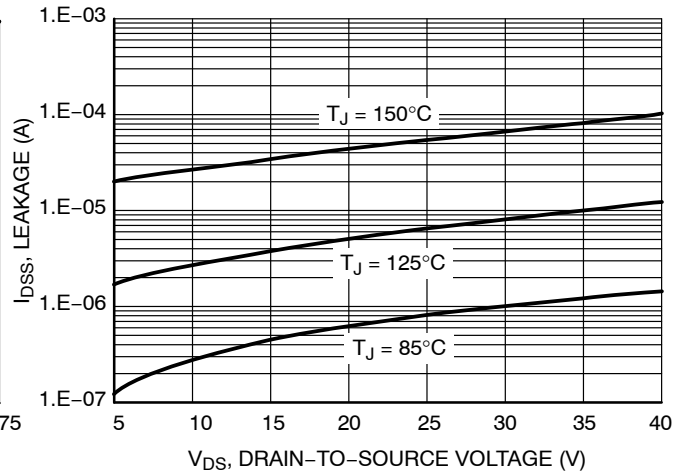


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

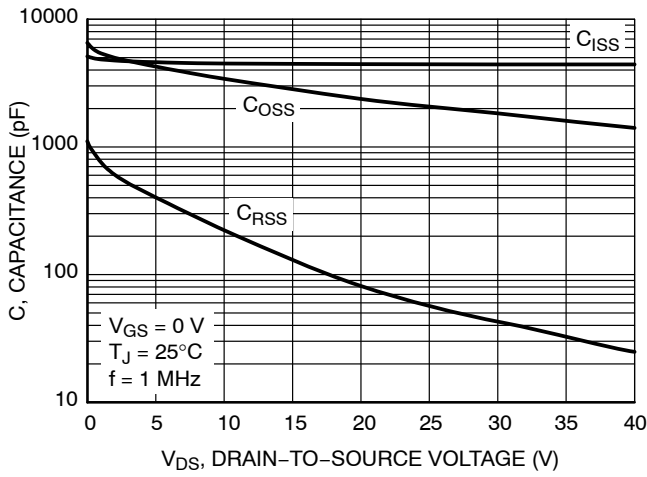


Figure 7. Capacitance Variation

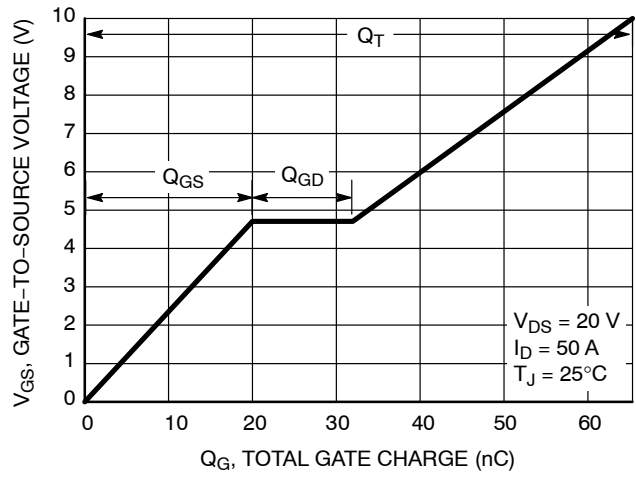


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

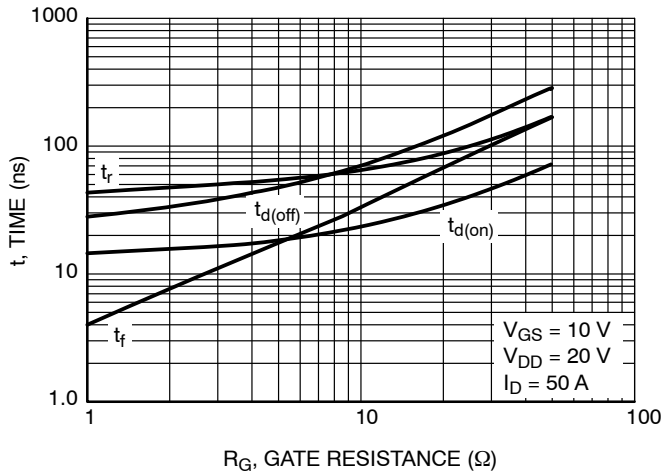


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

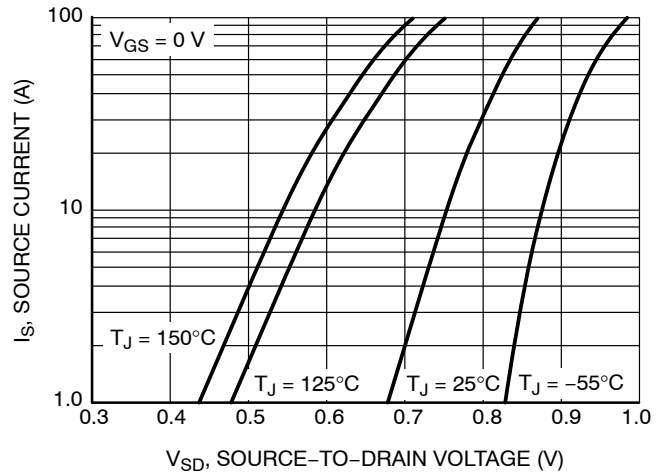


Figure 10. Diode Forward Voltage vs. Current

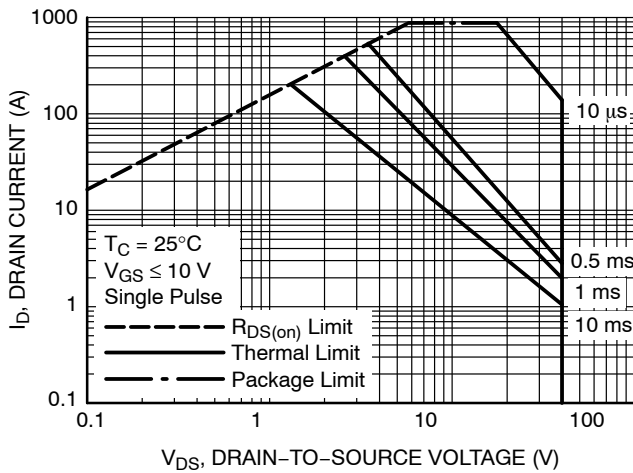


Figure 11. Safe Operating Area

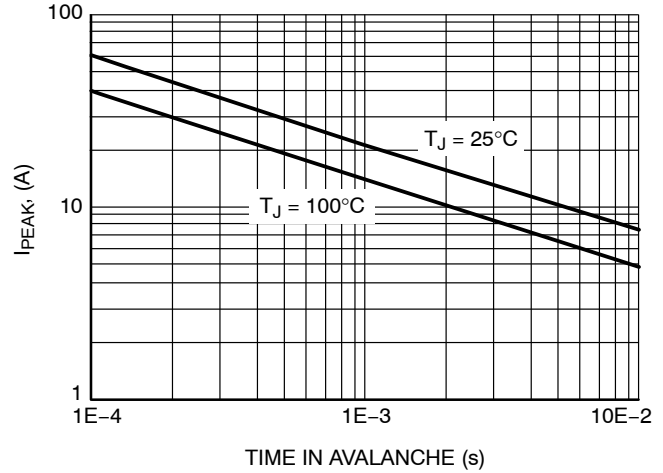


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

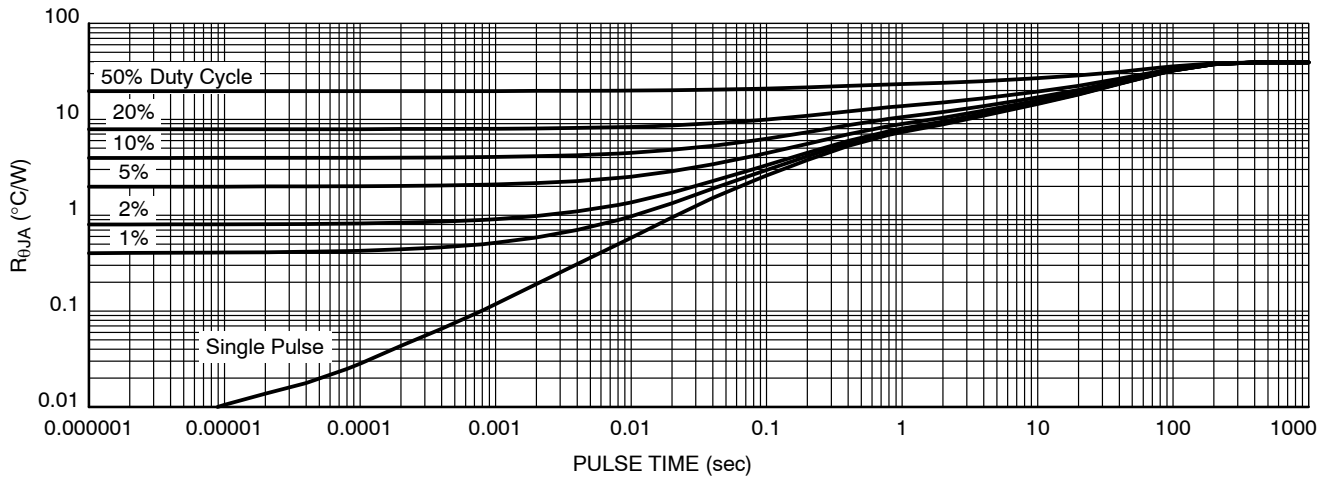
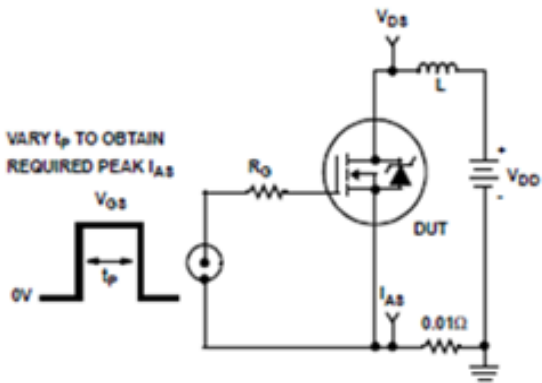
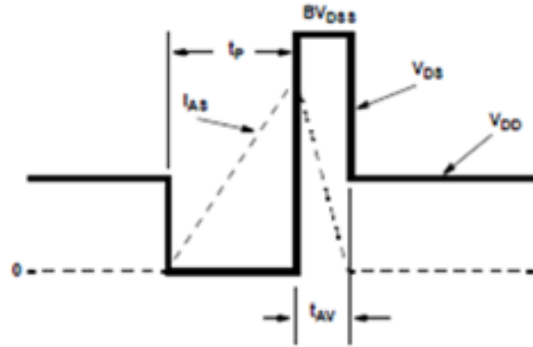


Figure 13. Thermal Characteristics

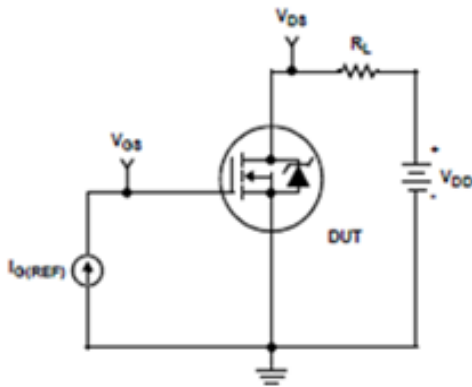
Test Circuits and Waveforms



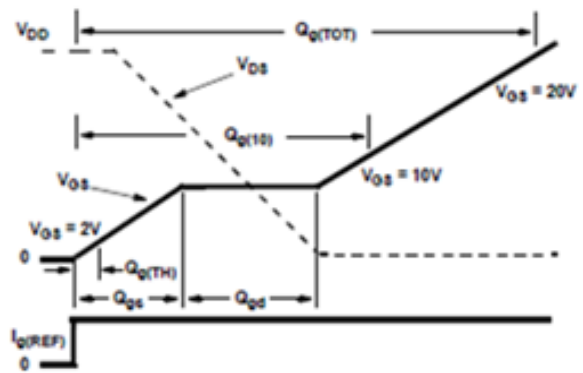
UNCLAMPED ENERGY TEST CIRCUIT



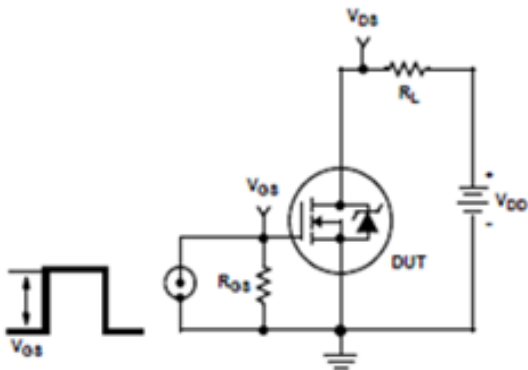
UNCLAMPED ENERGY WAVEFORMS



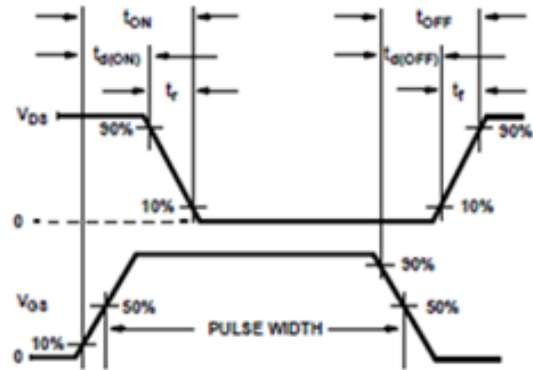
GATE CHARGE TEST CIRCUIT




GATE CHARGE WAVEFORM



SWITCHING TIME TEST CIRCUIT



RESISTIVE SWITCHING WAVEFORMS

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