

# NVGS4141N

## Product Preview

### Power MOSFET

#### 30 V, 7.7 A, Single N-Channel, TSOP-6

#### Features

- Low  $R_{DS(on)}$
- Low Gate Charge
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR-Free and are RoHS Compliant

#### Applications

- Load Switch
- Notebook PC
- Desktop PC

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DS}$	30	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	5.4	A
			$T_A = 85^\circ\text{C}$	4.2	
	$t \leq 10\text{ s}$	$T_A = 25^\circ\text{C}$	7.7		
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	1.2	W
			$t \leq 10\text{ s}$	2.4	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	3.8	A
		$T_A = 85^\circ\text{C}$	3.0		
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	$P_D$	0.61	W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}, V_{GS} = 10\text{V}$	$I_{DM}$	22	A	
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	1.2	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	125	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	248	

1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0773 in sq).

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

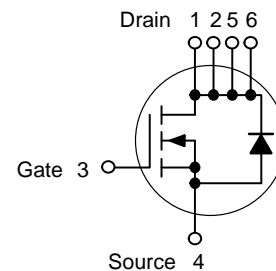


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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
30 V	21.5 m $\Omega$ @ 10 V	7.7 A
	30 m $\Omega$ @ 4.5 V	

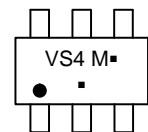
#### N-Channel



#### MARKING DIAGRAM

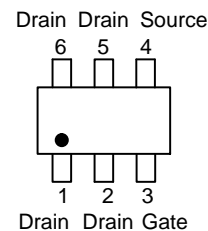


TSOP-6  
CASE 318G  
STYLE 1



VS4 = Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

#### PIN ASSIGNMENT



#### ORDERING INFORMATION

Device	Package	Shipping†
NVGS4141NT1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			18.4		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0		3.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			5.7		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.0 A		21.5	25	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.0 A		30	35	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7.0 A		30		S

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 24 V		560		pF
Output Capacitance	C <sub>OSS</sub>			115		
Reverse Transfer Capacitance	C <sub>RSS</sub>			75		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 7.0 A		12		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.85		
Gate-to-Source Charge	Q <sub>GS</sub>			1.9		
Gate-to-Drain Charge	Q <sub>GD</sub>			3.0		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 7.0 A		6.0		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.8		
Gate-to-Source Charge	Q <sub>GS</sub>			1.85		
Gate-to-Drain Charge	Q <sub>GD</sub>			3.0		
Gate Resistance	R <sub>G</sub>			2.8		Ω

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 7.0 A, R <sub>G</sub> = 3.0 Ω		6.0		ns
Rise Time	t <sub>r</sub>			15		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			18		
Fall Time	t <sub>f</sub>			4.0		

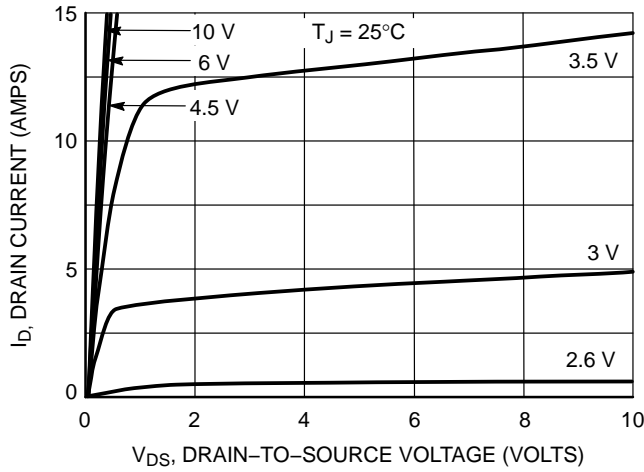
## DRAIN - SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.0 A	T <sub>J</sub> = 25°C	0.78	1.0	V
			T <sub>J</sub> = 125°C	0.63		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V di <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 2.0 A		15		ns
Charge Time	t <sub>a</sub>			9.0		
Discharge Time	t <sub>b</sub>			6.0		
Reverse Recovery Charge	Q <sub>RR</sub>			8.0		

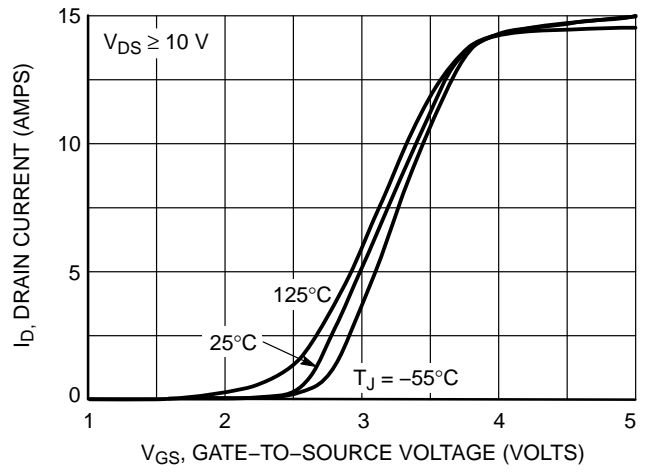
- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

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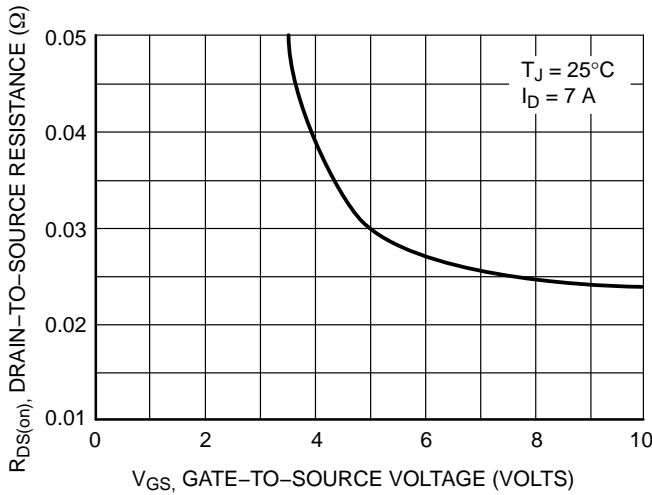
## TYPICAL PERFORMANCE CURVES



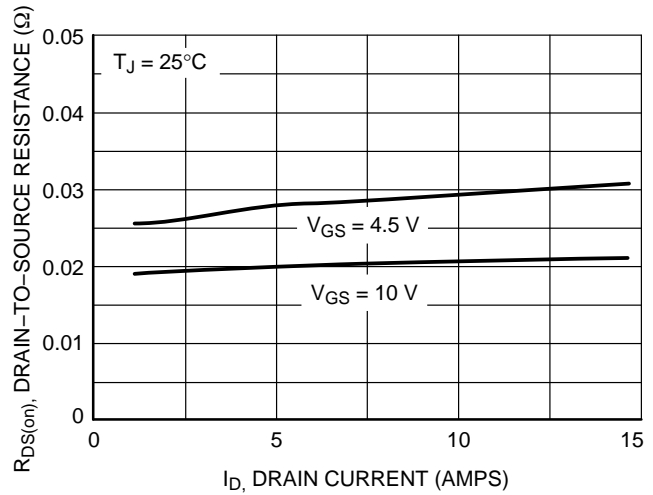
**Figure 1. On-Region Characteristics**



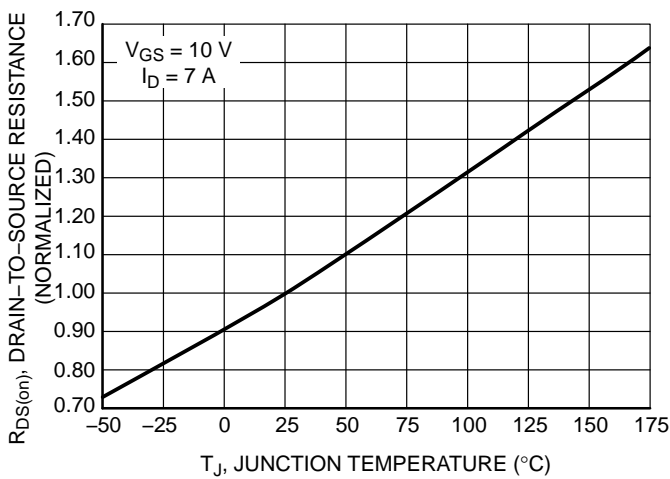
**Figure 2. Transfer Characteristics**



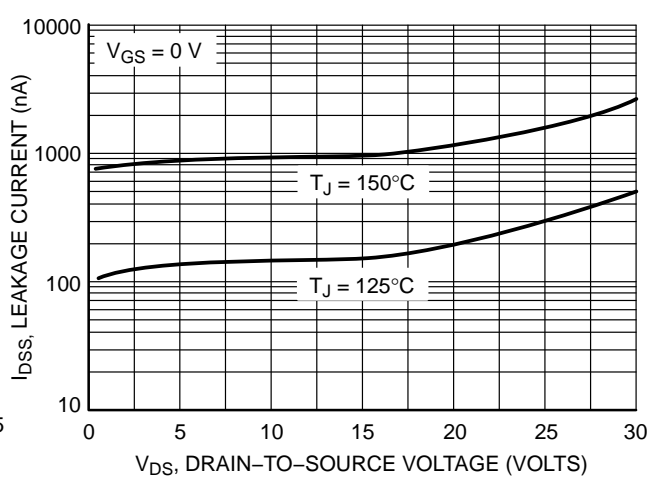
**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



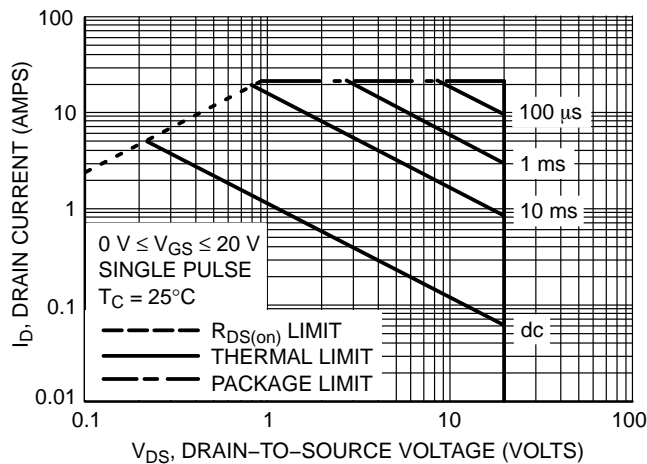
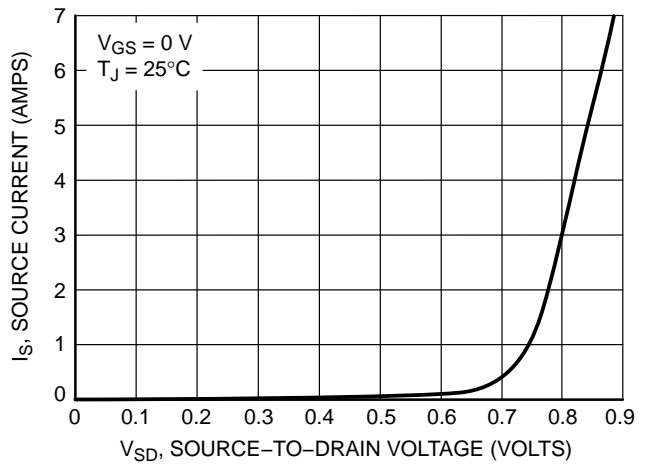
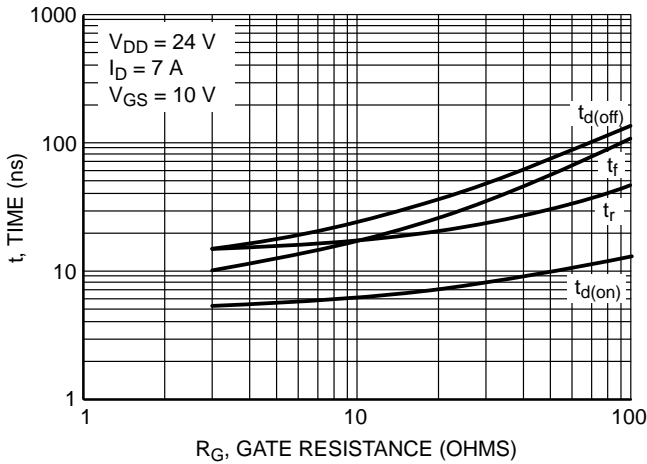
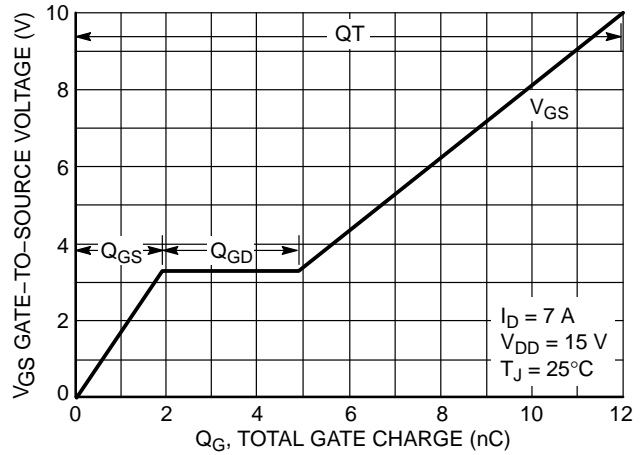
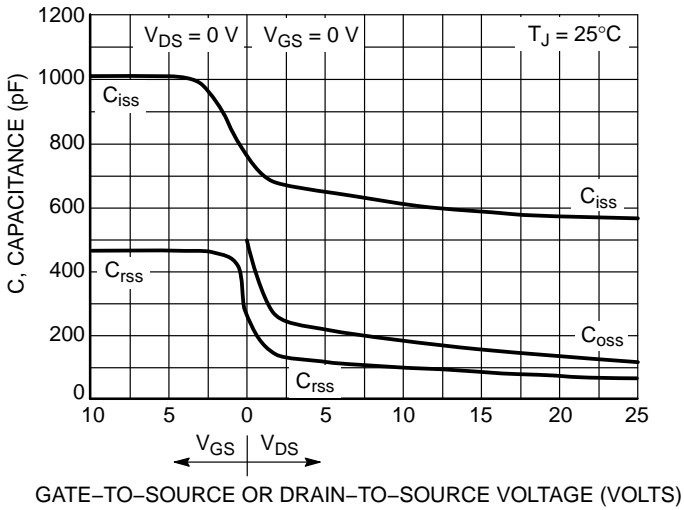
**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

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## TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES

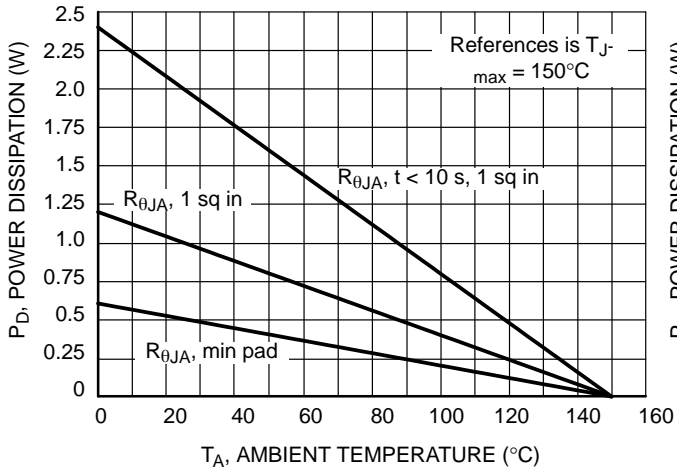


Figure 12. Maximum Power Derating Chart

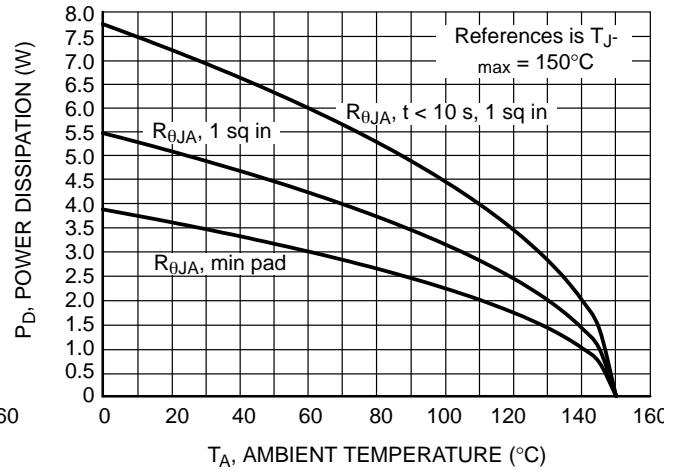


Figure 13. Current Derating Chart

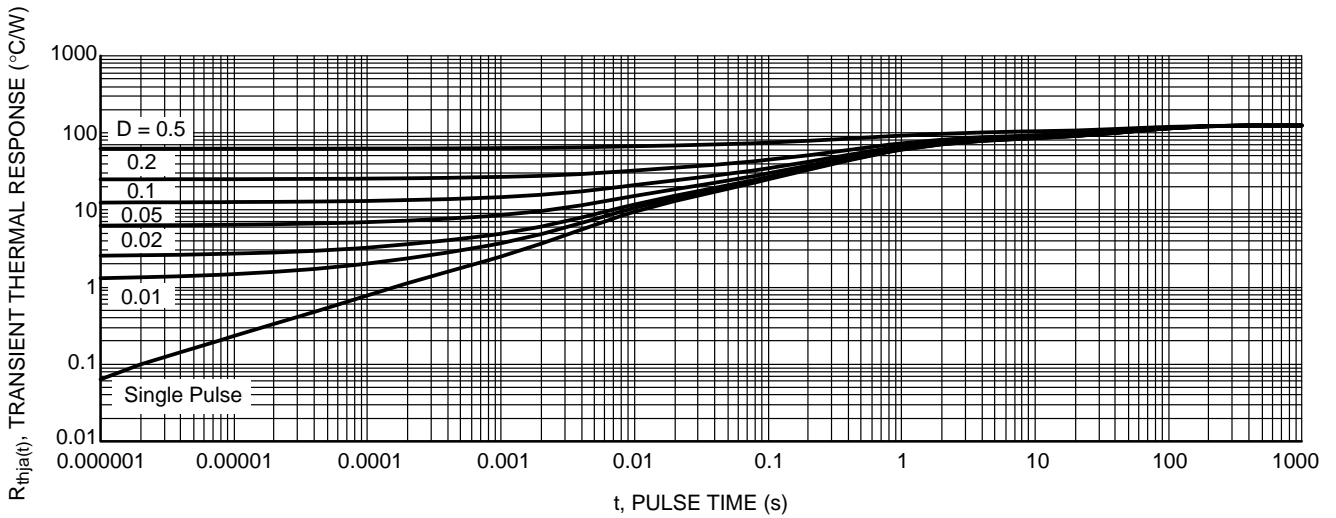
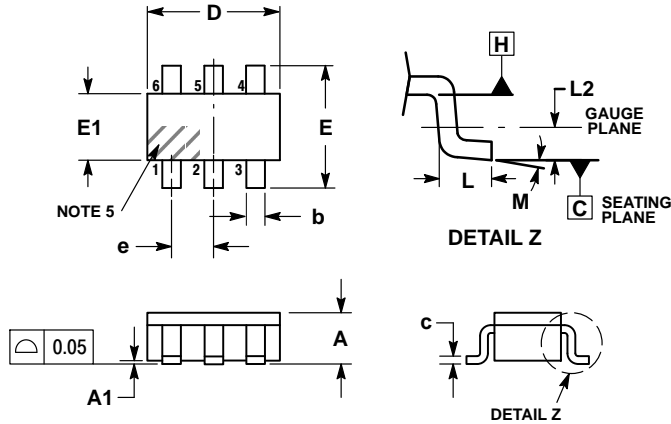


Figure 14. Thermal Response

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## PACKAGE DIMENSIONS

### TSOP-6 CASE 318G-02 ISSUE V



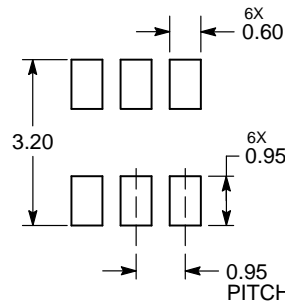
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°


- STYLE 1:  
 PIN 1: DRAIN  
 2: DRAIN  
 3: GATE  
 4: SOURCE  
 5: DRAIN  
 6: DRAIN

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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