

# NVMFS6H848NL

## Product Preview

### Power MOSFET

#### 80 V, 8.9 mΩ, 59 A, Single N-Channel

#### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFS6H848NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	80	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$ 59	A
		$T_C = 100^\circ\text{C}$	41	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$ 73	W
		$T_C = 100^\circ\text{C}$	37	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 13	A
		$T_A = 100^\circ\text{C}$	9.0	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 3.7	W
		$T_A = 100^\circ\text{C}$	1.8	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$ 317	A	
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	61	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 3.4 \text{ A}$ )	$E_{AS}$	TBA	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	2.0	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	41	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

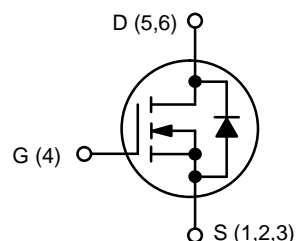
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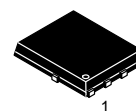
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$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
80 V	8.9 mΩ @ 10 V	59 A
	10.5 mΩ @ 4.5 V	

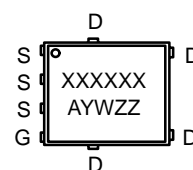


N-CHANNEL MOSFET



DFN5 (SO-8FL)  
CASE 488AA  
STYLE 1

#### MARKING DIAGRAM



XXXXXX = 6H848L  
(NVMFS6H848NL) or  
848LWF  
(NVMFS6H848NLWF)

A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 3 of this data sheet.

# NVMFS6H848NL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			TBA		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 70\ \mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			TBA		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		7.4	8.9	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		8.4	10.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		TBA		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 40\text{ V}$		TBA		pF	
Output Capacitance	$C_{OSS}$			TBA			
Reverse Transfer Capacitance	$C_{RSS}$			TBA			
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 10\text{ A}$		TBA		nC	
Threshold Gate Charge	$Q_{G(TH)}$			TBA			
Gate-to-Source Charge	$Q_{GS}$			TBA			
Gate-to-Drain Charge	$Q_{GD}$			TBA			
Plateau Voltage	$V_{GP}$		$V_{GS} = 4.5\text{ V}, V_{DS} = 40\text{ V}; I_D = 10\text{ A}$		TBA	V	
Total Gate Charge	$Q_{G(TOT)}$				TBA		nC

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 64\text{ V}, I_D = 10\text{ A}, R_G = 2.5\ \Omega$		TBA		ns
Rise Time	$t_r$			TBA		
Turn-Off Delay Time	$t_{d(OFF)}$			TBA		
Fall Time	$t_f$			TBA		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		TBA	1.2	V
			$T_J = 125^\circ\text{C}$		TBA		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 20\text{ A}$		TBA		ns	
Charge Time	$t_a$			TBA			
Discharge Time	$t_b$			TBA			
Reverse Recovery Charge	$Q_{RR}$				TBA		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

# NVMFS6H848NL

## DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS6H848NLT1G	6H848L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS6H848NLWFT1G	848LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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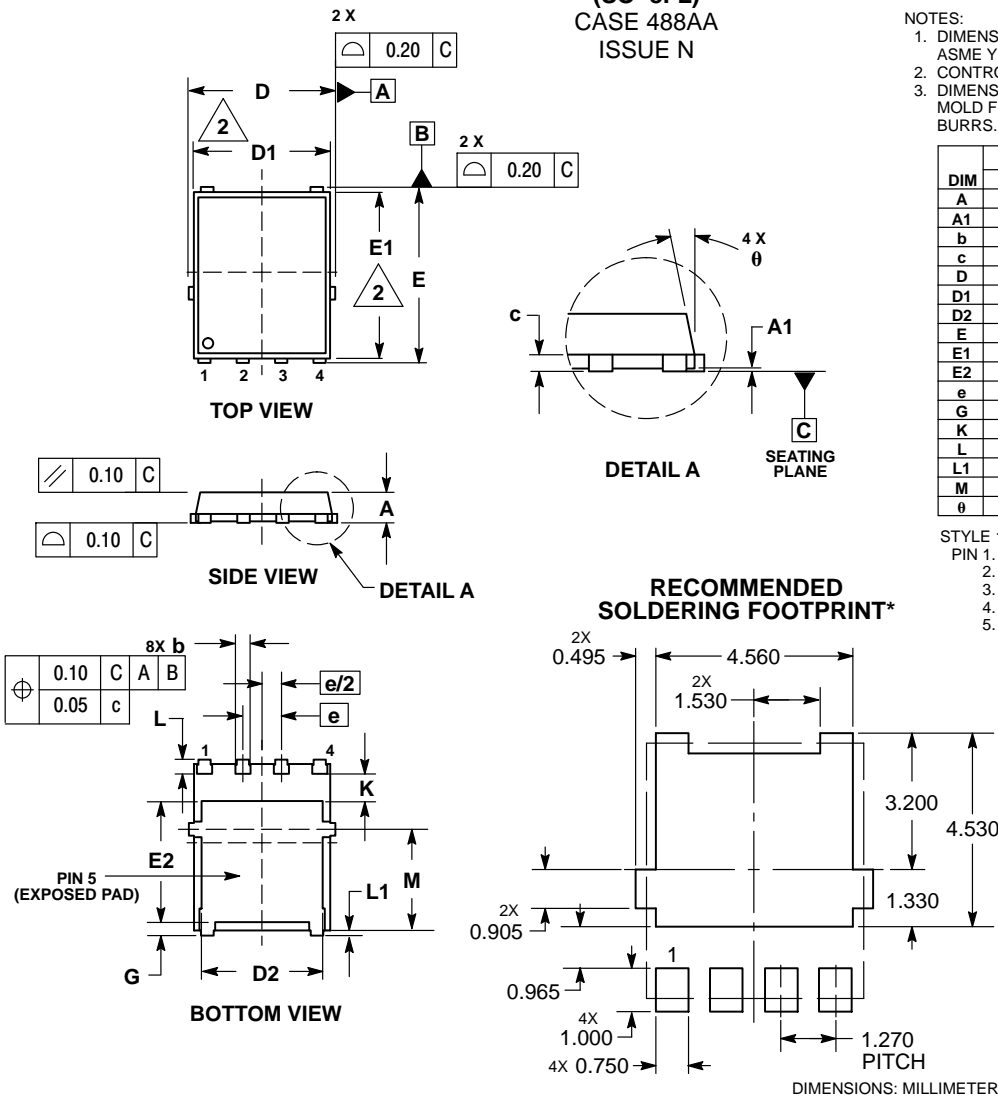
## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

- STYLE 1:
1. SOURCE
  2. SOURCE
  3. SOURCE
  4. GATE
  5. DRAIN



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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