NVMFSC0D9N04CL

MOSFET – Power, DUAL COOL® N-Channel, DFN8 5x6

40 V, 0.85 mΩ, 316 A

ON Semiconductor®

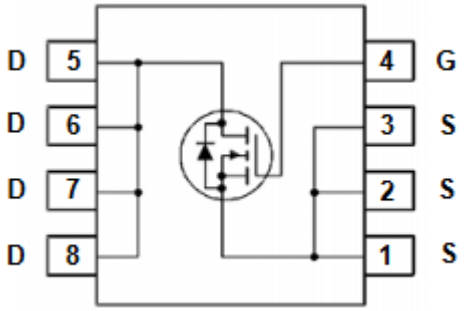
www.onsemi.com

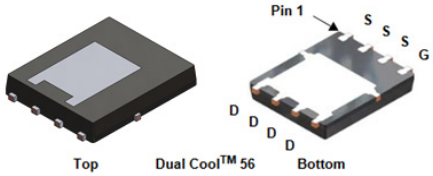
Features

- Advanced Dual−sided Cooled Packaging
- Small Footprint (5x6 mm) for Compact Design
- Ulra Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant
- MSL1 Robust Packaging Design

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	0.85 mΩ @ 10 V	316 A
	1.3 mΩ @ 4.5 V	

N−Channel MOSFET





DFN8 5x6
CASE 506EG

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	316	A
		T_C = 100°C	I_D	224	A
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	P_D	166	W
		T_C = 100°C	P_D	83	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	50	A
		T_A = 100°C	I_D	35	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	4.1	W
		T_A = 100°C	P_D	2.0	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	138	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 29 A)			E_{AS}	706	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Bottom)− Steady State (Note 2)	$R_{\theta JC}$	0.9	°C/W
Junction−to−Case (Top) − Steady State (Note 2)	$R_{\theta JC}$	1.4	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	37	

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

MARKING DIAGRAM

410LVC = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			10	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V				100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.5		3.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 250 μA, ref to 25°C			−8.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		0.69	0.87	mΩ
Forward Transconductance	g_{FS}	V_{DS} =TBD V, I_D = TBD A			190		S
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			6100		pF
Output Capacitance	C_{OSS}				3400		
Reverse Transfer Capacitance	C_{RSS}				70		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 32 V; I_D = 50 A			86		
Gate−to−Source Charge	Q_{GS}				28		
Gate−to−Drain Charge	Q_{GD}				14		
Plateau Voltage	V_{GP}				4.9		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 32 V, I_D = 50 A, R_G = 2.5 Ω			54		ns
Rise Time	t_r				160		
Turn−Off Delay Time	$t_{d(OFF)}$				220		
Fall Time	t_f				170		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = TBD A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 50 A			91		ns
Charge Time	t_a				42		
Discharge Time	t_b				49		
Reverse Recovery Charge	Q_{RR}				159		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

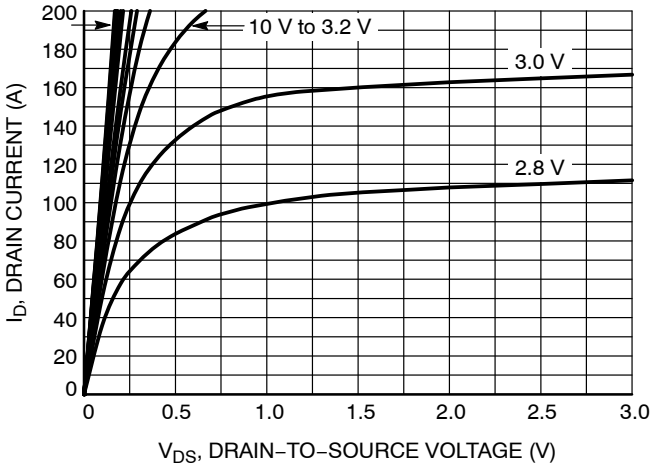


Figure 1. On−Region Characteristics

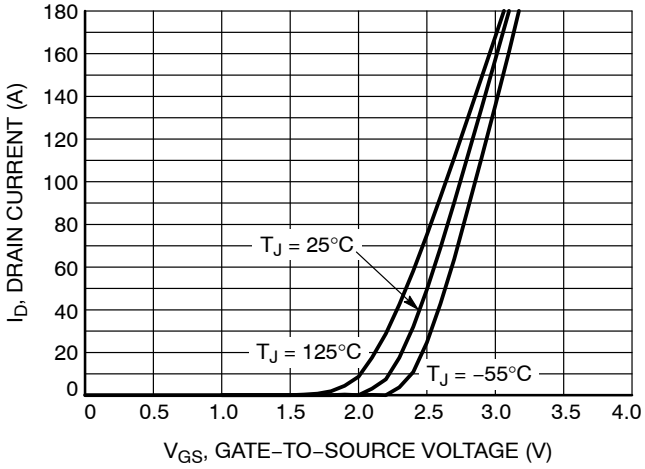


Figure 2. Transfer Characteristics

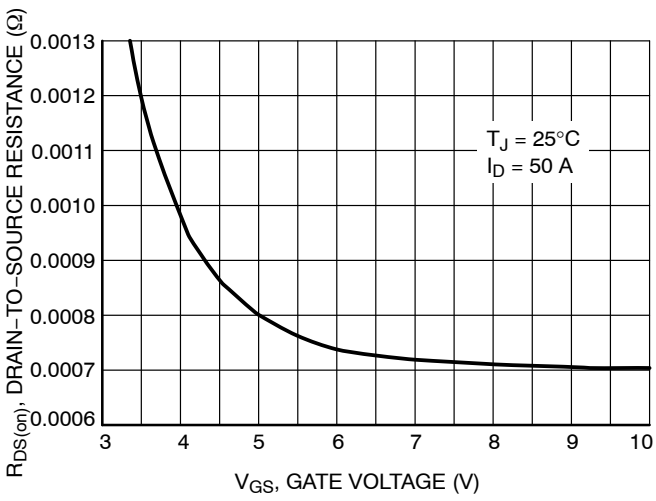


Figure 3. On−Resistance vs. Gate−to−Source Voltage

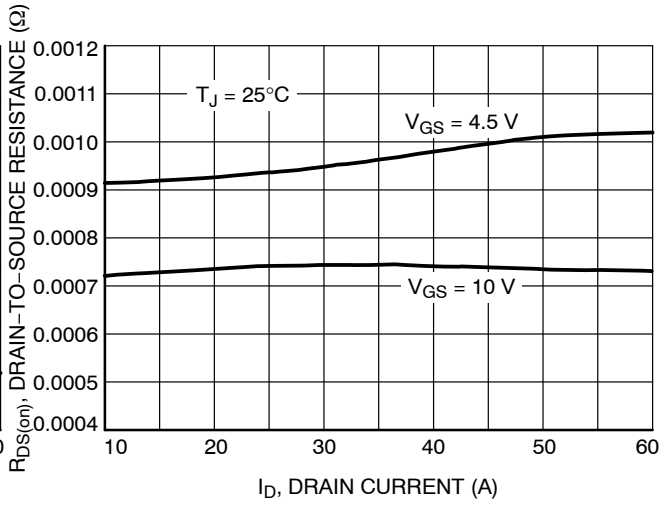


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

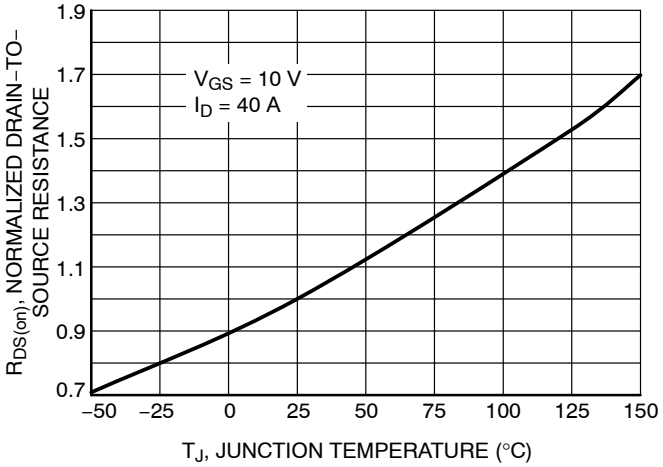


Figure 5. On−Resistance Variation with Temperature

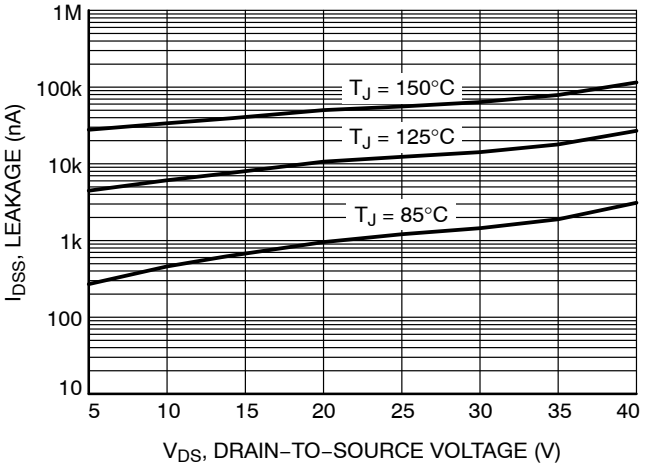


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

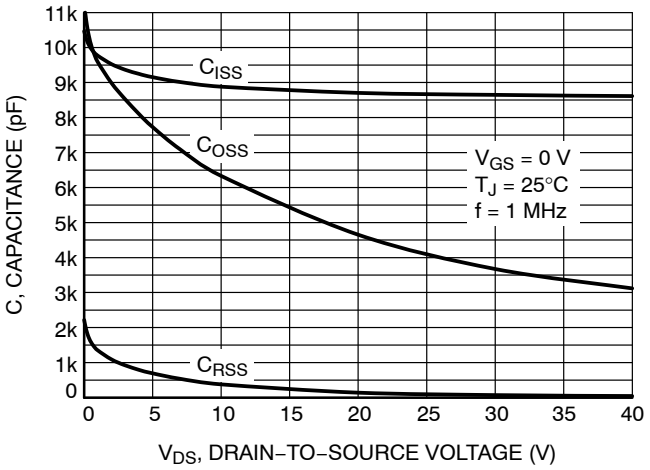


Figure 7. Capacitance Variation

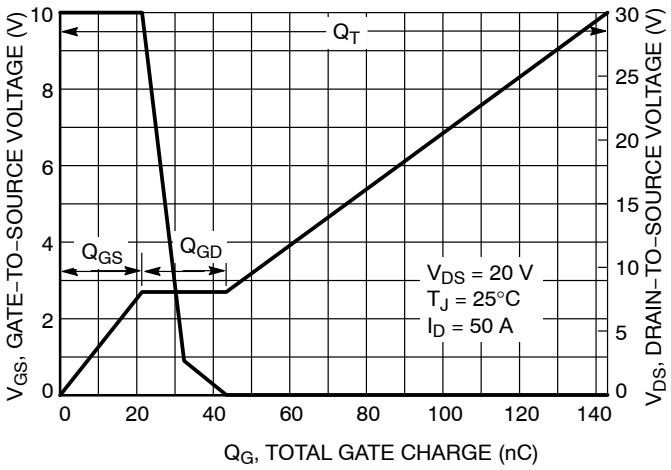


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

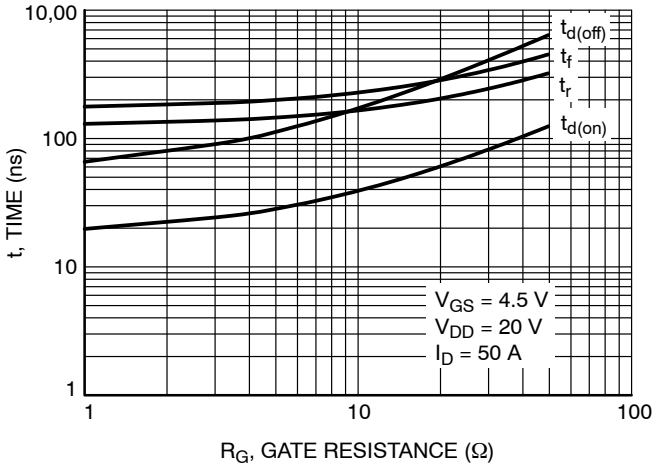


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

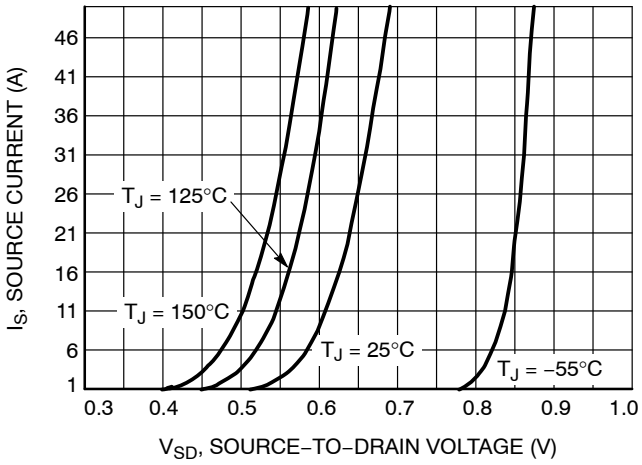


Figure 10. Diode Forward Voltage vs. Current

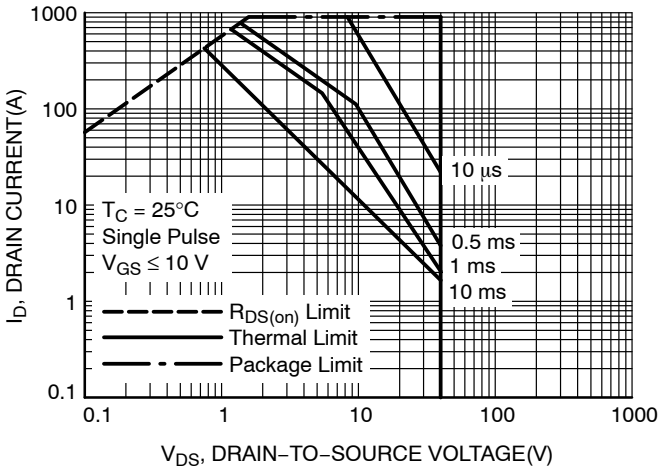


Figure 11. Safe Operating Area

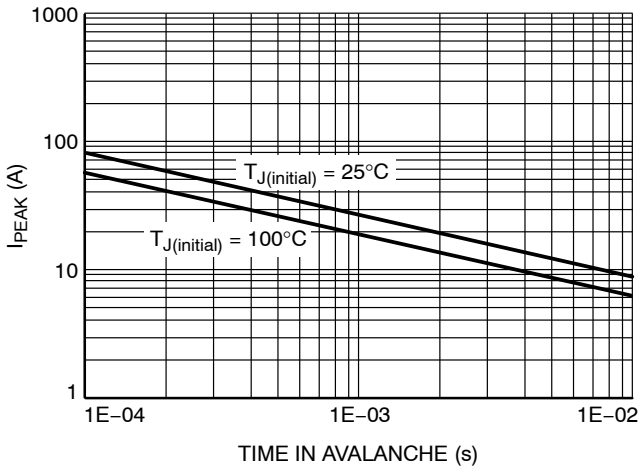


Figure 12. I_{PEAK} vs. Time in Avalanche

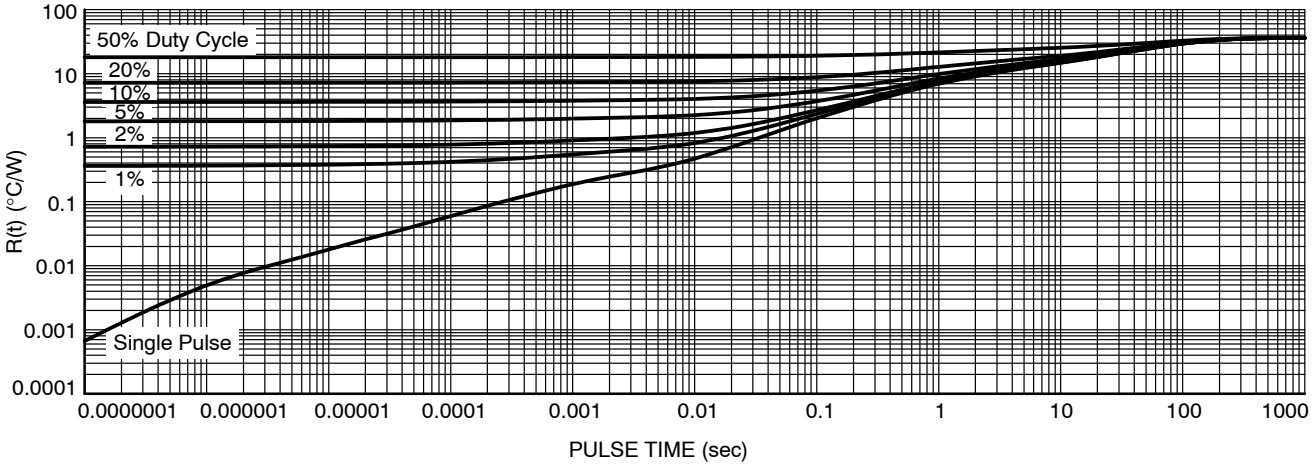


Figure 13. Thermal Characteristics

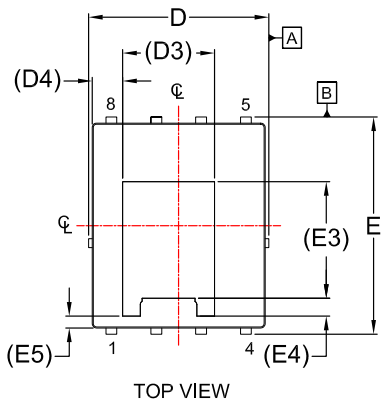
ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
NVMFSC0D9N04CL	410LVC	PQFN8 5x6 (Pb−Free/Halogen Free)	3000 / Tape & Reel

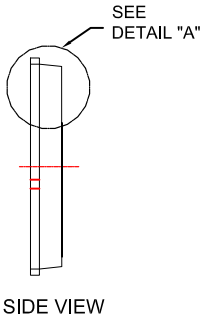
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

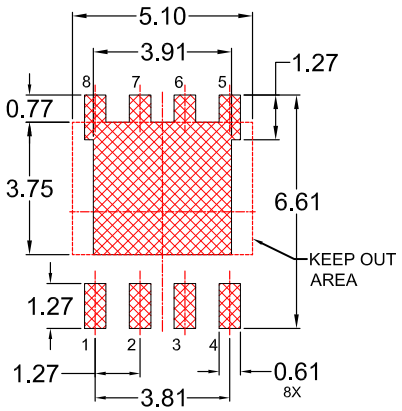
DFN8 5.1x6.15, 1.27P
CASE 506EG
ISSUE A



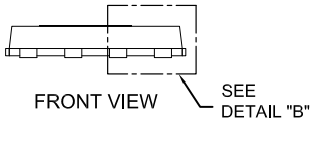
TOP VIEW

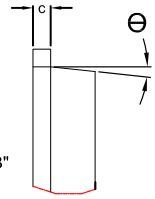


SIDE VIEW

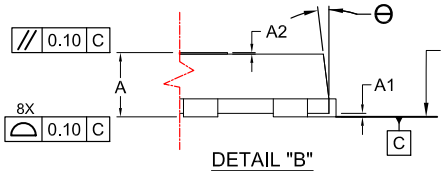


LAND PATTERN
RECOMMENDATION



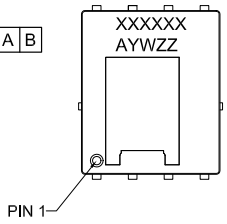


DETAIL "A"
SCALE: 2:1



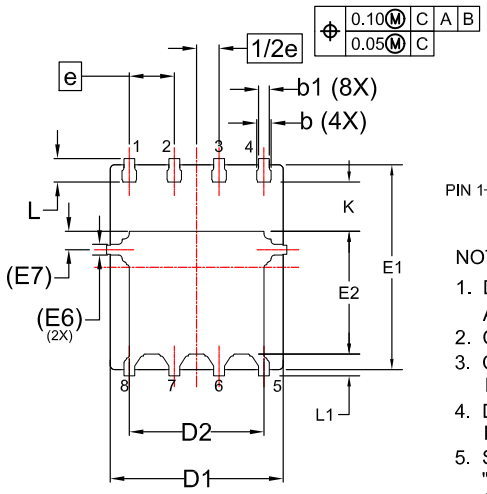
DETAIL "B"
SCALE: 2:1

GENERIC MARKING DIAGRAM



XXXXXX = DEVICE CODE
A = ASSY LOCATION
Y = YEAR CODE
W = WORK WEEK CODE
ZZ = ASSY LOT CODE

*THIS INFORMATION IS GENERIC. PLEASE REFER TO DEVICE DATA SHEET FOR ACTUAL PART MARKING.



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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