

# NVMYS003N08LH

## Product Preview

# MOSFET - Power, Single N-Channel

## 80 V, 3.5 mΩ, 128 A

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- LFPK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	80	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$ 128	A
		$T_C = 100^\circ\text{C}$	90	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$ 137	W
		$T_C = 100^\circ\text{C}$	68	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 22	A
		$T_A = 100^\circ\text{C}$	15	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 3.9	W
		$T_A = 100^\circ\text{C}$	2.0	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$ 900	A	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	114	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 9 \text{ A}$ )	$E_{AS}$	TBD	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	1.1	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	38	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

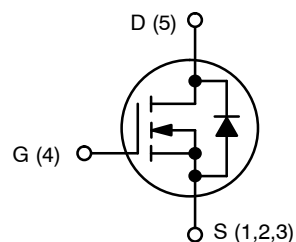
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$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
80 V	3.5 mΩ @ 10 V	128 A
	4.4 mΩ @ 4.5 V	

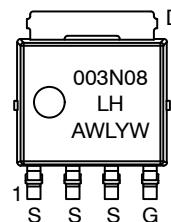


N-CHANNEL MOSFET



LFPK4 CASE 760AB

### MARKING DIAGRAM



003N08LH = Specific Device Code  
 A = Assembly Location  
 WL = Wafer Lot  
 Y = Year  
 W = Work Week

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

# NVMYS003N08LH

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			20		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 183\ \mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			TBD		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		2.9	3.5	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		3.5	4.4	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		TBD		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 40\text{ V}$		TBD		$\text{pF}$
Output Capacitance	$C_{OSS}$			TBD		
Reverse Transfer Capacitance	$C_{RSS}$			TBD		
Total Gate Charge	$Q_G(\text{TOT})$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 50\text{ A}$		TBD		nC
Total Gate Charge	$Q_G(\text{TOT})$	$V_{GS} = 4.5\text{ V}, V_{DS} = 40\text{ V}; I_D = 50\text{ A}$		TBD		nC
Threshold Gate Charge	$Q_G(\text{TH})$			TBD		
Gate-to-Source Charge	$Q_{GS}$			TBD		
Gate-to-Drain Charge	$Q_{GD}$			TBD		
Plateau Voltage	$V_{GP}$			TBD		

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 64\text{ V}, I_D = 50\text{ A}, R_G = 2.5\ \Omega$		TBD		ns
Rise Time	$t_r$			TBD		
Turn-Off Delay Time	$t_{d(OFF)}$			TBD		
Fall Time	$t_f$			TBD		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		TBD	1.2	V
			$T_J = 125^\circ\text{C}$		TBD		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$			TBD		ns
Charge Time	$t_a$				TBD		
Discharge Time	$t_b$				TBD		
Reverse Recovery Charge	$Q_{RR}$				TBD		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

### DEVICE ORDERING INFORMATION

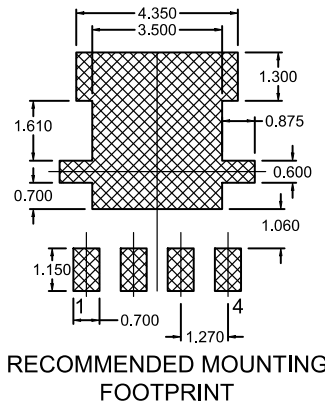
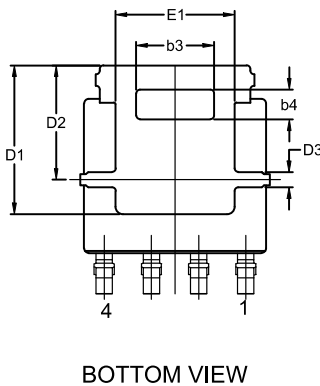
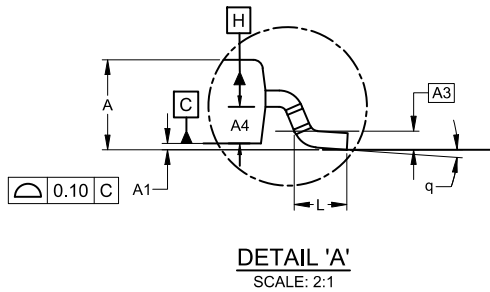
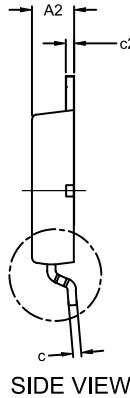
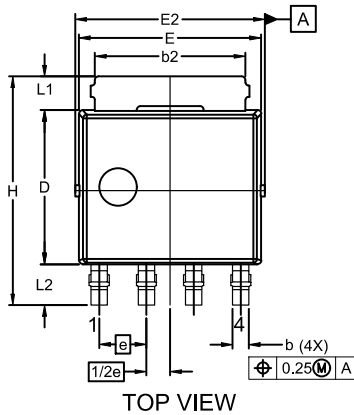
Device	Marking	Package	Shipping <sup>†</sup>
NVMYS003N08LHTWG	003N08LH	LFP4K4 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NVMYS003N08LH

## PACKAGE DIMENSIONS

### LFFPAK4 5x6 CASE 760AB ISSUE A



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3		0.25	
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b3	2.00	2.10	2.20
b4	0.70	0.80	0.90
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.05	4.15	4.25
D1	-	-	4.20
D2	3.0	3.10	3.20
D3	0.30	0.40	0.50
E	4.80	4.90	5.00
E1	3.10	3.20	3.30
E2	5.00	5.15	5.30
e	1.27 BSC		
H	6.00	6.15	6.30
L	0.40	0.65	0.85
L1	0.80	0.90	1.00
L2	0.80	1.05	1.30
q	0°	4°	8°

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