ONBCD25

Process Technology

ONBCD25: 0.25 μm Process Technology

ON Semiconductor®

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Overview

ONBCD25 from ON Semiconductor is a full−featured high voltage 0.25 μm node technology. ONBCD25 contains 5 V single−gate or 5/12 V dual−gate high voltage transistors combined with mixed−signal features including MIM capacitors, Schottky diodes, zener diodes, high resistivity poly, plus a variety of npn/pnp bipolar transistors, capacitors, diodes and resistors. The high voltage transistors include optimized NLDMOS and high voltage PMOS 40/5 V, 40/12 V, 24/5 V and 12/12 V transistors. The high−performance / low−power 5 V digital library and one−time programmable (OTP) element offered in the baseline ONC25 technology are available as well. ONBCD25 provides the flexibility to implement a variety of mixed−signal functions in a product design.

Features

- Gate Oxide Voltages: Single−Gate 5 V, Dual−Gate 5/12 V
- NLDMOS 40/5 V, 40/12 V, 24/5 V and 12/12 V (Drain to Source Voltage/Gate to Source Voltage)
- High Voltage PMOS 40/5 V, 40/12 V, 24/5 V and 12/12 V
- High Voltage Schottky Diodes: 18, 30, 40 V
- Zener Diodes: 5.15, 5.5, 6.2, and 7.4 V
- High Voltage Isolation
- Variety of npn/pnp Bipolar Transistors, Diodes and Resistors Constructed with High Voltage Process Additions
- 2 to 5 Metal Layers
- Top Metal Thickness Options: 1.0, 1.5 and 3.0 μm AI−0.5% Cu
- LV MOS Circuits can be Floated in HV Isolated Wells
- MIM Capacitors: 1.0 fF/mm^2 Located below Top Metal
- High Sheet Resistance (1.5 kΩ) Polysilicon Resistor
- Low Temperature Coefficient P−type Polysilicon Resistor
- Salicided Active and Poly with Optional Blocking
- Characterized ESD Protection Cells

PROCESS CHARACTERISTICS

Operating Voltage	5, 12, 24, 40 V
Substrate Material	200 mm P−Type, EPI
Drawn Transistor Length	0.5 μm (5 V CMOS)
Gate Oxide Thickness	125, 300 Å
Contact/Via Size	0.3 / 0.36 μm
Top Metal Thickness	1.0, 1.5, 3.0 μm (Al−0.5% Cu thickness)
Contacted Metal Pitch	
Metal 1	0.64 μm
Metal 2−4	0.94 μm
Metal Top	
1.0 μm Al−0.5% Cu	2.0 μm
1.5 μm Al−0.5% Cu	3.0 μm
3.0 μm Al−0.5% Cu	6.0 μm
Metal Composition	Al(0.5%Cu)

SAMPLE PROCESS OPTIONS

LV MOS	Mask Layers
Single Gate 5 V, 2 Metal	23
Single Gate 5 V, 5 Metal	29
Dual Gate 5 V & 12 V	+2
MIM	+1
30 V Schottky	+1
40 V Schottky	+1
5.15 V Zener	+1
5.5 V Zener	+1
1.5 kΩ /sq Poly Resistor	+1
LTC Poly Resistor	0 to +1

DEVICE CHARACTERISTICS

All Values Typical at 25°C

HV DMOS

	Max V_{ds} (V)	Typ $R_{DS(ON)}$ (mΩ/mm^2)	Typ V_t (V)
NLDMOS 12/12 V	13.2	8.5	2.22
PMOS 12/12 V	25	58.6	2.34
PMOS 12/12 V Low Threshold Voltage	25	80.5	0.82
NLDMOS 40/5 V	44	40.8	0.95
PMOS 40/5 V	44	112	0.84
NLDMOS 40/12 V	44	44.2	3.24
PMOS 40/12 V	44	110	2.33
PMOS 40/12 V Low Threshold Voltage	38	119	0.83
NLDMOS 24/5 V	47.7	28	1.3
PMOS 24/5 V	33	60	0.82

LV MOS

	Typ V_t	Typ I_{dsat}
NMOS 5 V	0.82 V	500 μA/μm
PMOS 5 V	−0.88 V	−240 μA/μm

BJTs

	Typ Beta	Typ B_{Vceo} (V)	Typ B_{Vcbo} (V)
NPNH	52	26	65
NPNL	17.4	27	27
PNPSLV	9.3	24	35
PNPS	2.6	12	19.2

FORWARD V_f DIODES

	Min B_V (V)
P+ / N−well	7
N+ / P−well	7
P+ / HVN−well	14
N+ / HVP−well	14
HVP−well / Nbl	56
P−well / HVN−well	20
Pbl / Nbl	46
18 V Schottky	22
30 V Schottky	32
40 V Schottky	44

CAPACITORS

	Max Voltage	Typical Value
MIM	15 V	1.0 fFμm^2
CPNW 5 V (5 V gate oxide to NW), V_{gs} = 5.0 V	5 V	2.46 fFμm^2

RESISTORS

	Typ Value	Temp Coef
N−well under STI	1400 Ω/sq	3600 ppm/°C
P+poly unsilicided	280 Ω/sq	−75 ppm/°C
Low Tempco Poly unsilicided	335 Ω/sq	−34.2 ppm/°C
High Rs Poly unsilicided	1500 Ω/sq	1200 ppm/°C
HV N−Well under STI	690 Ω/sq	–
HV P−Well under STI	4900 Ω/sq	–

AVALANCHE DIODES

	Typ B_V (V)
Pbody / N−well	15
5.15 V Zener	5.15
5.5 V Zener	5.5
6.2 V Zener	6.2
7.4 V Zener	7.4

ESD PROTECTION

	HBM Levels
LV ESD Diodes	2 – 8 kV
LV Supply Clamps	2 – 4 kV
HV 4 kV ESD Diodes	2 −4 kV
HV Supply Clamps	2 kV

ONBCD25

LIBRARIES

Front−End Digital Design	
Digital	Synthesis Libraries
	Simulation Libraries
Analog	Design Rules
	Parametrized Layout Cells
	Spectre Models
Standard Cell	
5 V Core Shell	398 total cells
	1−layer metal and 2−layer metal pwr rail option
	33.1 k gates/mm^2 (Routed @ 75% util)
	0.122 ns prop delay (2−input NAND, fanout = 2)

CAD TOOL COMPATIBILITY

Digital Design	Synopsys Design Compiler
	Cadence RTL Compiler
	Mentor Graphics FastScan (DFT)
Analog Design	Cadence Virtuoso, VirtuosoXL, Spectre and Eldo
	Mentor Graphics Design Architect IC, IC Station and Eldo
Place and Route	Cadence Encounter
	Synopsys Apollo
Physical Verification	Mentor Graphics Calibre

MEMORY OPTIONS

OTP	
5 V Poly Fuse	32 − 256 bit in 32 bit increments

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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