PCFG40T120SQF

IGBT Die

Trench Ultra Field Stop IGBT Die optimized for UPS and Solar applications.

Features

- Extremely Efficient Trench with Field Stop Technology
- Low $V_{CE(sat)}$ Loss Reduces System Power Dissipation
- Optimized for High Speed Switching

Typical Applications

- Solar Inverters
- UPS Systems

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V_{CE} = 1200 V
I_C = Limited by $T_{J(max)}$

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Collector−Emitter Voltage, T_J = 25°C	V_{CE}	1200	V
DC Collector Current, limited by max $T_{J(max)}$	I_C	(Note 1)	A
Pulsed Collector Current (Note 2)	$I_{C, pulse}$	160	A
Gate−Emitter Voltage	V_{GE}	±20	V
Maximum Junction Temperature	T_J	−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Depending on thermal properties of assembly.
2. T_{pulse} limited by T_{jmax}, 10 μSec pulse V_{GE} = 15 V.

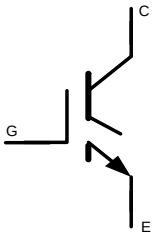
MECHANICAL DATA

Parameter	Value	Unit
Die Size	5384 x 4184	μm^2
Emitter Pad Size	See die layout	μm^2
Gate Pad Size	405 x 660	μm^2
Die Thickness	112	μm
Wafer Size	150	mm^2
Top Pad Metal	5 μm AlCu	
Back Metal	2 μm AlTiNiAg	
Passivation	1.5 μm HR NIT	
Max possible chips per wafer	551	
Reject Ink dot size	25 mils	
Recommended storage environment: In original container, in dry nitrogen, or temperature of 18−28°C, 30−65% RH	Type: Sawn wafer on tape. Storage time: <3 months	

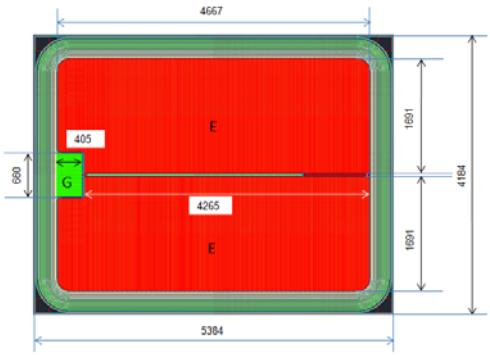
ORDERING INFORMATION

Device	Inking?	Shipping
PCFG40T120SQF	Yes	Sawn Wafer on Tape

IGBT DIE



DIE OUTLINE

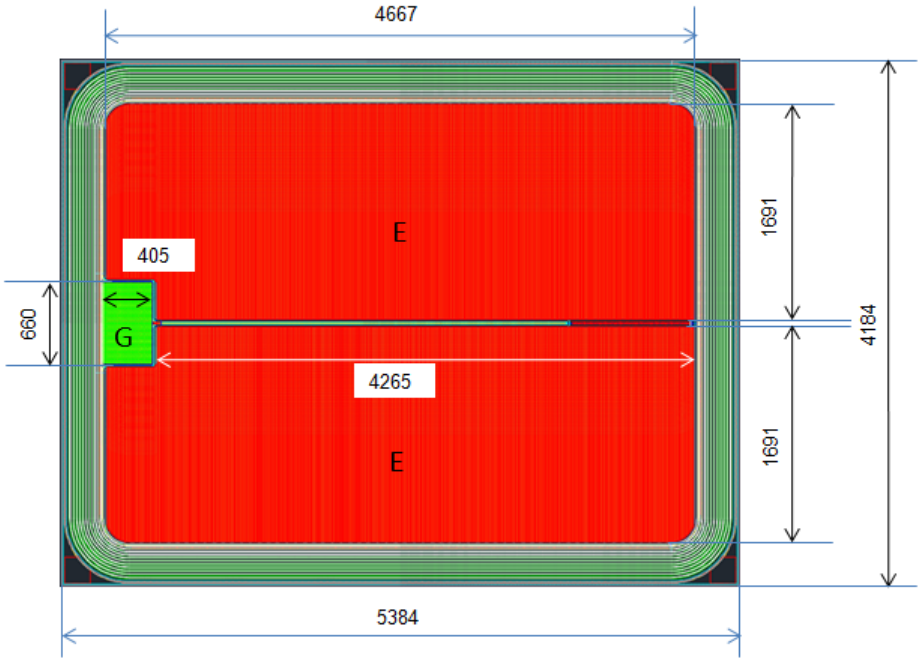


ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
STATIC CHARACTERISTICS						
Collector−Emitter Breakdown Voltage	V_{GE} = 0 V, I_C = 500 μA	$V_{(BR)CES}$	1200	–	–	V
Collector−Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 40 A	$V_{CE(sat)}$	–	1.7	1.95	V
Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 400 μA	$V_{GE(TH)}$	4.5	5.5	6.5	V
Collector−Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 1200 V	I_{CES}	–	–	400	μA
Gate Leakage Current	V_{GE} = ±20 V, V_{CE} = 0 V	I_{GES}	–	–	±200	nA
DYNAMIC CHARACTERISTICS						
Input Capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 1 MHz	C_{ies}	–	4912	–	pF
Output Capacitance		C_{oes}	–	140	–	
Reverse Transfer Capacitance		C_{res}	–	80	–	
Gate Charge Total	V_{CE} = 600 V, V_{GE} = 15 V, I_C = 40 A	Q_g	–	212	–	nC
Gate−Emitter Charge		Q_{ge}	–	43	–	
Gate−Collector Charge		Q_{gc}	–	102	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DIE LAYOUT



E = Emitter Pad
G = Gate Pad
All dimensions in μm

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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