

# PCFG75T120SQF

## IGBT Die

Trench Ultra Field Stop IGBT Die optimized for UPS and Solar applications.

### Features

- Extremely Efficient Trench with Field Stop Technology
- Low  $V_{CE(sat)}$  Loss Reduces System Power Dissipation
- Optimized for High Speed Switching

### Typical Applications

- Solar Inverters
- UPS Systems

### MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Collector-Emitter Voltage, $T_J = 25^\circ\text{C}$	$V_{CE}$	1200	V
DC Collector Current, limited by max $T_{J(max)}$	$I_C$	(Note 1)	A
Pulsed Collector Current (Note 2)	$I_{C, pulse}$	300	A
Gate-Emitter Voltage	$V_{GE}$	$\pm 20$	V
Maximum Junction Temperature	$T_J$	-55 to +175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Depending on thermal properties of assembly.
2.  $T_{pulse}$  limited by  $T_{jmax}$ , 10  $\mu\text{Sec}$  pulse  $V_{GE} = 15\text{ V}$ .

### MECHANICAL DATA

Parameter	Value	Unit
Die Size	6200 x 6200	$\mu\text{m}^2$
Emitter Pad Size	See die layout	$\mu\text{m}^2$
Gate Pad Size	405 x 660	$\mu\text{m}^2$
Die Thickness	112	$\mu\text{m}$
Wafer Size	150	$\text{mm}^2$
Top Pad Metal	5 $\mu\text{m}$ AlCu	
Back Metal	2 $\mu\text{m}$ AlTiNiAg	
Passivation	1.5 $\mu\text{m}$ HR NIT	
Max possible chips per wafer	310	
Reject Ink dot size	25 mils	
Recommended storage environment: In original container, in dry nitrogen, or temperature of 18–28 $^\circ\text{C}$ , 30–65% RH	Type: Sawn wafer on tape. Storage time: <3 months	

### ORDERING INFORMATION

Device	Inking?	Shipping
PCFG75T120SQF	Yes	Sawn Wafer on Tape

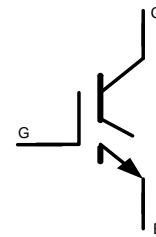


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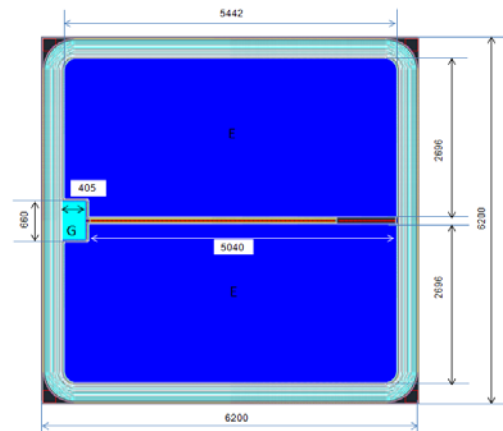
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$V_{CE} = 1200\text{ V}$   
 $I_C = \text{Limited by } T_{J(max)}$

IGBT DIE



DIE OUTLINE



# PCFG75T120SQF

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

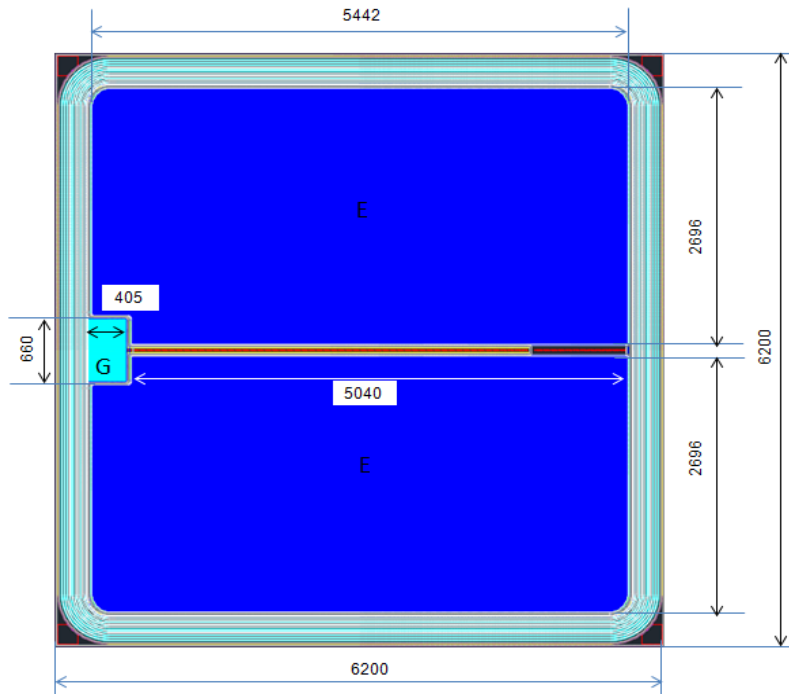
Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
<b>STATIC CHARACTERISTICS</b>						
Collector–Emitter Breakdown Voltage	$V_{GE} = 0\text{ V}, I_C = 500\ \mu\text{A}$	$V_{(BR)CES}$	1200	–	–	V
Collector–Emitter Saturation Voltage	$V_{GE} = 15\text{ V}, I_C = 40\text{ A}$	$V_{CE(sat)}$	–	1.7	1.95	V
Gate–Emitter Threshold Voltage	$V_{GE} = V_{CE}, I_C = 400\ \mu\text{A}$	$V_{GE(TH)}$	4.5	5.5	6.5	V
Collector–Emitter Cutoff Current	$V_{GE} = 0\text{ V}, V_{CE} = 1200\text{ V}$	$I_{CES}$	–	–	400	$\mu\text{A}$
Gate Leakage Current	$V_{GE} = \pm 20\text{ V}, V_{CE} = 0\text{ V}$	$I_{GES}$	–	–	$\pm 200$	nA

## DYNAMIC CHARACTERISTICS

Input Capacitance	$V_{CE} = 20\text{ V}, V_{GE} = 0\text{ V}, f = 1\text{ MHz}$	$C_{ies}$	–	9060	–	pF
Output Capacitance		$C_{oes}$	–	242	–	
Reverse Transfer Capacitance		$C_{res}$	–	137	–	
Gate Charge Total	$V_{CE} = 600\text{ V}, V_{GE} = 15\text{ V}, I_C = 75\text{ A}$	$Q_g$	–	399	–	nC
Gate–Emitter Charge		$Q_{ge}$	–	74	–	
Gate–Collector Charge		$Q_{gc}$	–	192	–	


Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## DIE LAYOUT



**E = Emitter Pad**  
**G = Gate Pad**  
 All dimensions in  $\mu\text{m}$

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