PCGA200T65NF8M1

650 V, 200 A Field Stop Trench IGBT with Solderable Top Metal

ON Semiconductor®

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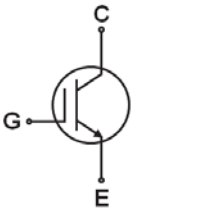
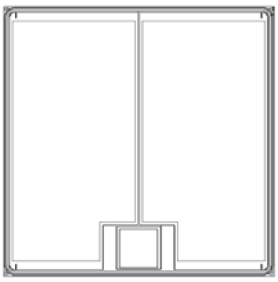
Features

- AEC−Q101 Qualified
- Maximum Junction Temperature 175°C
- Positive Temperature Coefficient
- Easy Paralleling
- Short Circuit Rated
- Very Low Saturation Voltage: $V_{CE(SAT)}$ = 1.53 V(Typ.) @ I_C = 200 A
- Optimized for Motor Control Applications
- Emitter Pad Covered with Solderable Metal Layer

Applications

- Automotive Traction Modules
- General Power Modules





ORDERING INFORMATION

Part Number	PCGA200T65NF8M1	
Packing	Water (sawn on foil)	
	mils	μm
Die Size	394 × 394	10,000 × 10,000
Emitter Attach Area	2 × (177 × 348)	2 × (4,493.5 × 8,832)
Gate / Sensor Pad Attach Area	55 × 55	1,408 × 1,406
Die Thickness	3	79
Top Metal	5 μm AlSiCu + 1.15 μm Ti/NiV/Ag (STM)	
Back Metal	0.95 μm NiV/Ag	
Topside Passivation	Silicon Nitride plus Polyimide	
Wafer Diameter	200 mm	
Max Possible Die Per Wafer	234	

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Ratings	Units
Collector−Emitter Voltage	V_{CES}	650	V
Gate−Emitter Voltage	V_{GES}	±20	V
DC Collector Current, limited by T_J max	I_C	(Note 1)	A
Pulsed Collector Current, V_{GE}=15 V, t_p limited by T_J max (Note 2)	I_{CM}	600	A
Short Circuit Withstand Time, V_{GE} = 15 V, $V_{CE} \le$ 400 V, $T_J \le$ 150°C	t_{sc}	5	μs
Operating Junction Temperature	T_J	−40 to +175	°C
Storage Temperature Range	T_{stg}	+17 to +25	°C

1. Depends on the thermal properties of assembly
2. Not subject to production test − verified by design/characterization

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min.	Typ.	Max.	Units
Static Characteristics (Tested on wafers)							
Collector−Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0 V, I_C = 1 mA		650	−	−	V
Collector−Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 A, V_{GE} = 15 V		−	1.25	1.75	V
Gate−Emitter Threshold Voltage	$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 200 mA		4.5	5.5	6.5	V
Collector Cut−Off Current	I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0 V		−	−	40	μA
Gate Leakage Current	I_{GES}	V_{GE} = V_{GES}, V_{CE} = 0 V		−	−	±400	nA
Electrical Characteristics (Not subjected to production test − verified by design/characterization)							
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 200 A, V_{GE} = 15 V	T_J = 25°C	−	1.53	1.9	V
			T_J = 175°C	−	2.04	−	V
Input Capacitance	C_{IES}	V_{CE} = 30 V, V_{GE} = 0 V, f = 1 MHz		−	9.6	−	nF
Output Capacitance	C_{OES}			−	445	−	pF
Reverse Transfer Capacitance	C_{RES}			−	78	−	pF
Internal Gate Resistance	R_G	f = 1 MHz		−	2.0	−	Ω
Total Gate Charge	$Q_{G(Total)}$	V_{CE} = 400 V, I_C = 200 A, V_{GE} = 15 V		−	229	−	nC
Gate−to−Emitter Charge	Q_{GE}			−	66	−	nC
Gate−to−Collector Charge	Q_{GC}			−	64	−	nC
Turn−On Delay Time	$t_{d(on)}$	V_{CE} = 400 V, I_C = 200 A, R_G = 15 Ω, V_{GE} = 15 V, Inductive Load, T_J = 25°C		−	67	−	ns
Rise Time	t_r			−	233	−	ns
Turn−Off Delay Time	$t_{d(off)}$			−	118	−	ns
Fall Time	t_f			−	177	−	ns
Turn−On Delay Time	$t_{d(on)}$	V_{CE} = 400 V, I_C = 200 A, R_G = 15 Ω, V_{GE} = 15 V, Inductive Load, T_J = 175°C		−	64	−	ns
Rise Time	t_r			−	236	−	ns
Turn−Off Delay Time	$t_{d(off)}$			−	124	−	ns
Fall Time	t_f			−	208	−	ns

3. For ordering, technique and other information on Onsemi automotive bare die products, please contact automotivebaredie@onsemi.com

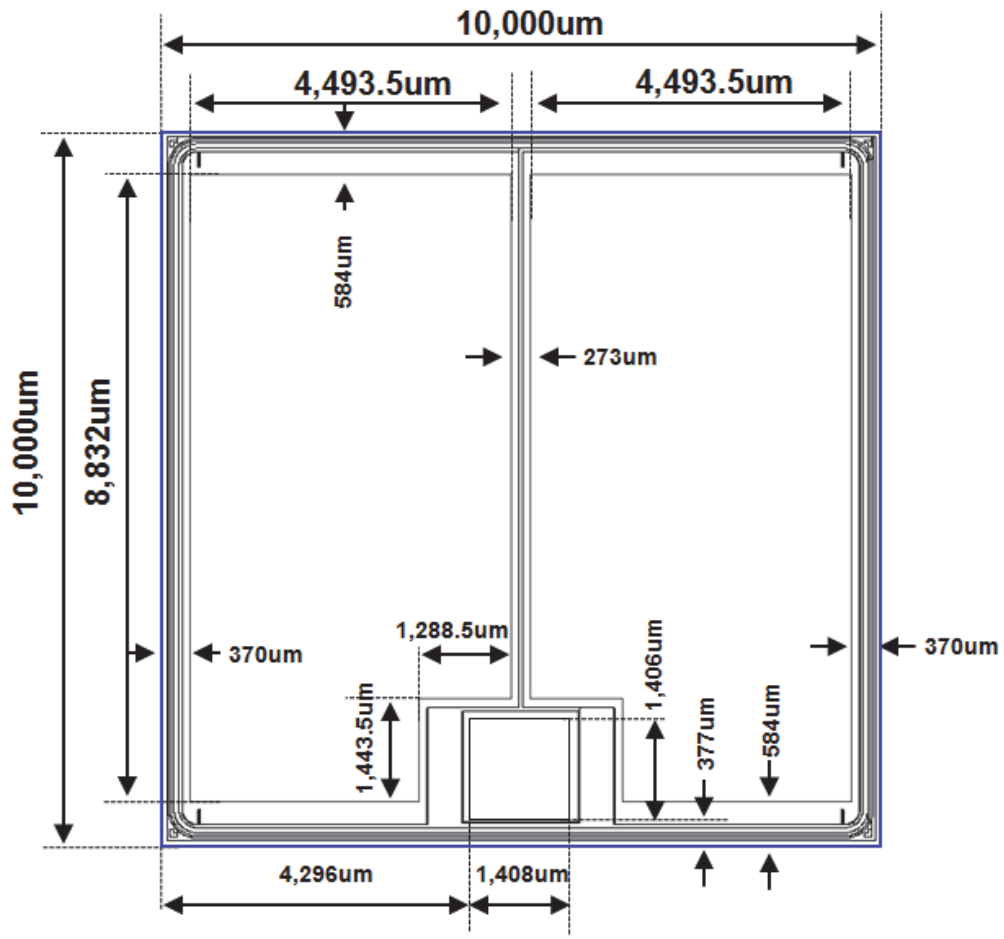


Figure 1. Dimensional Outline and Pad Layout

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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