SCY305

Voltage Detector Series

The SCY305 series is a second generation ultra−low current voltage detectors. These devices are specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is paramount.

The series features a highly accurate undervoltage detector with hysteresis which prevents erratic system reset operation as the comparator threshold is crossed.

The SCY305 series has an open drain N−Channel output with an active low reset output.

The SCY305 device series is available in a WLCSP package with standard undervoltage thresholds. Additional thresholds that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

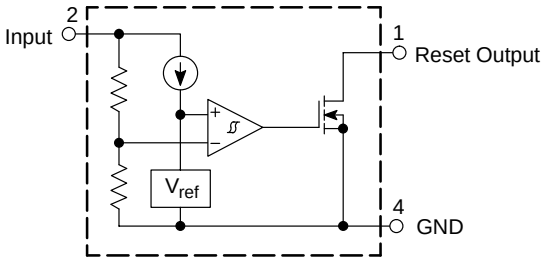
Features

- Quiescent Current of 1.0 μA Typical
- High UVLO Accuracy of 1.0% at Room Temperature
  1.5% Over Room Temperature
- Wide Operating Voltage Range of 0.8 V to 10 V
- Open Drain Reset Output
- Active Low Reset Output
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Microprocessor Reset Controller
- Low Battery Detection
- Power Fail Indicator
- Battery Backup Detection

SCY305LFCCxxTxx
Open Drain Output Configuration



This device contains 37 active transistors.

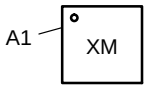
* The representative block diagram depicts active low reset output ‘L’ suffix devices. The comparator input is interchanged for the active high output ‘H’ suffix devices.

Figure 1. Representative Block Diagram

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

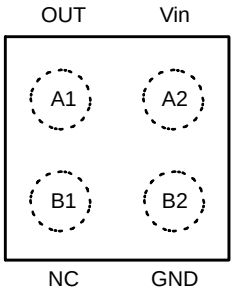
WLCSP4
FCC SUFFIX
CASE TBD

MARKING DIAGRAM



X = Specific Device Code
M = Month

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Table 1. MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Input Power Supply Voltage (Pin 2)	V_{in}	12	V
Output Voltage (Pin 1) N−Channel Open Drain, SCY305	V_{OUT}	 −0.3 to 12	V
Output Current (Pin 1) (Note 2)	I_{OUT}	70	mA
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	TBD	°C/W
Maximum Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Latchup Performance (Note 3) Positive Negative	$I_{LATCHUP}$	 500 170	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V.
2. The maximum package power dissipation limit must not be exceeded.
$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$
3. Maximum Ratings per JEDEC standard JESD78.

Table 2. ELECTRICAL CHARACTERISTICS (For all values T_A = 25°C, unless otherwise noted.)

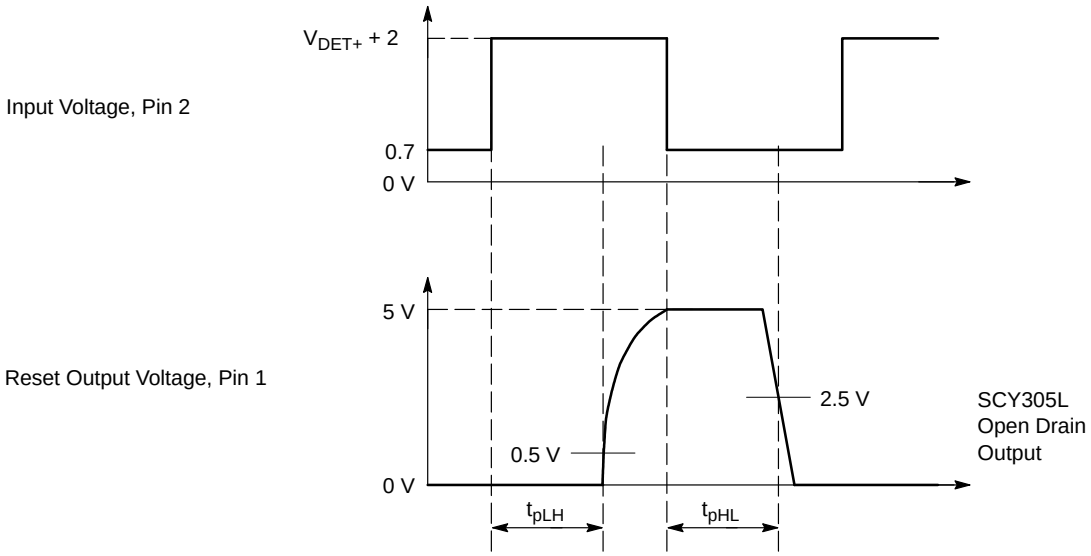
Characteristic	Symbol	Min	Typ	Max	Unit
SCY305 − 2.7					
Detector Threshold (Pin 2, V_{in} Decreasing)	V_{DET-}	2.673 2.660	2.700 2.700	2.727 2.741	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.081	0.135	0.189	V
Supply Current (Pin 2) (V_{in} = 2.6 V) (V_{in} = 4.7 V)	I_{in}	 − −	 0.9 1.1	 2.7 3.3	μA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	−	−	10	V
Minimum Operating Voltage (Pin 2) (T_A = −40°C to 85°C)	$V_{in(min)}$	− −	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) N−Channel Sink Current, SCY305 (V_{OUT} = 0.05 V, V_{in} = 0.70 V) (V_{OUT} = 0.50 V, V_{in} = 1.5 V)	I_{OUT}	 0.01 1.0	 0.05 2.0	 − −	mA
Reset Output Current (Pin 1, Active High 'H' Suffix Devices) N−Channel Sink Current, SCY305 (V_{OUT} = 0.5 V, V_{in} = 5.0 V)	I_{OUT}	 6.3	 11	 −	mA
Propagation Delay Input to Output (Figure 2) N−Channel Open Drain SCY305 Series Output Transition, High to Low (Note 4) Output Transition, Low to High (Note 4)	 t_{pHL} t_{pLH}	 − −	 12 −	 − 70	μs
SCY305 − 2.9					
Detector Threshold (Pin 2, V_{in} Decreasing)	V_{DET-}	2.871 2.857	2.900 2.900	2.929 2.944	V

4. In the case of CMOS Output Type: The time interval between the rising edge of V_{DD} input pulse from 0.7 V to ($+V_{DET}$) +2.0 V and output voltage level becoming to V_{DD}/2. In the case of N−Channel Open Drain Output Type: Output pin is pulled up with a resistance of 470 kΩ to 5.0 V, the time interval between the rising edge of V_{DD} input pulse from 0.7 V to ($+V_{DET}$) +2.0 V and output voltage level becoming to 2.5 V.

Table 2. ELECTRICAL CHARACTERISTICS (continued) (For all values T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
SCY305 − 2.9					
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.087	0.145	0.203	V
Supply Current (Pin 2) (V_{in} = 2.8 V) (V_{in} = 4.9 V)	I_{in}	 − −	 0.9 1.1	 2.9 3.5	μA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	−	−	10	V
Minimum Operating Voltage (Pin 2) (T_A = −40°C to 85°C)	$V_{in(min)}$	− −	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) N−Channel Sink Current, SCY305 (V_{OUT} = 0.05 V, V_{in} = 0.70 V) (V_{OUT} = 0.50 V, V_{in} = 1.5 V)	I_{OUT}	 0.01 1.0	 0.05 2.0	 − −	mA
Reset Output Current (Pin 1, Active High 'H' Suffix Devices) N−Channel Sink Current, SCY305 (V_{OUT} = 0.5 V, V_{in} = 5.0 V)	I_{OUT}	 6.3	 11	 −	mA
Propagation Delay Input to Output (Figure 2) N−Channel Open Drain SCY305 Series Output Transition, High to Low (Note 4) Output Transition, Low to High (Note 4)	 t_{pHL} t_{pLH}	 − −	 12 −	 − 70	μs
SCY305 − 3.0					
Detector Threshold (Pin 2, V_{in} Decreasing)	V_{DET-}	2.970 2.955	3.00 3.00	3.030 3.045	V
Detector Threshold Hysteresis (Pin 2, V_{in} Increasing)	V_{HYS}	0.09	0.15	0.21	V
Supply Current (Pin 2) (V_{in} = 2.87 V) (V_{in} = 5.0 V)	I_{in}	 − −	 1.0 1.2	 3.0 3.6	μA
Maximum Operating Voltage (Pin 2)	$V_{in(max)}$	−	−	10	V
Minimum Operating Voltage (Pin 2) (T_A = −40°C to 85°C)	$V_{in(min)}$	− −	0.55 0.65	0.70 0.80	V
Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) N−Channel Sink Current, SCY305 (V_{OUT} = 0.05 V, V_{in} = 0.70 V) (V_{OUT} = 0.50 V, V_{in} = 1.5 V)	I_{OUT}	 0.01 1.0	 0.05 2.0	 − −	mA
Reset Output Current (Pin 1, Active High 'H' Suffix Devices) N−Channel Sink Current, SCY305 (V_{OUT} = 0.5 V, V_{in} = 5.0 V)	I_{OUT}	 6.3	 11	 −	mA
Propagation Delay Input to Output (Figure 2) N−Channel Open Drain SCY305 Series Output Transition, High to Low (Note 4) Output Transition, Low to High (Note 4)	 t_{pHL} t_{pLH}	 − −	 12 −	 − 70	μs

4. In the case of CMOS Output Type: The time interval between the rising edge of V_{DD} input pulse from 0.7 V to ($+V_{DET}$) +2.0 V and output voltage level becoming to V_{DD}/2. In the case of N−Channel Open Drain Output Type: Output pin is pulled up with a resistance of 470 kΩ to 5.0 V, the time interval between the rising edge of V_{DD} input pulse from 0.7 V to ($+V_{DET}$) +2.0 V and output voltage level becoming to 2.5 V.



The SCY305 series is measured with a 10 pF capacitive load. The SCY305 has an additional 470 k pullup resistor connected from the reset output to +5.0 V. The reset output voltage waveforms are shown for the active low ‘L’ devices. The upper detector threshold, V_{DET+} is the sum of the lower detector threshold, V_{DET-} plus the input hysteresis, V_{HYS}.

Figure 2. Propagation Delay Measurement Conditions

Table 3. SCY305 SERIES ELECTRICAL CHARACTERISTIC TABLE FOR 0.9 − 4.9 V, T_A = 25°C

Part Number	Detector Threshold V_{DET-} (V)			Detector Threshold Hysteresis V_{HYS} (V)			Supply Current		N−Channel Sink Current	
							V_{in} Low	V_{in} High	V_{in} Low	V_{in} High
							I_{in} (μA) (Note 5)	I_{in} (μA) (Note 6)	I_{OUT} (mA) (Note 7)	I_{OUT} (mA) (Note 8)
	Min	Typ	Max	Min	Typ	Max	Typ	Typ	Typ	Typ
SCY305LFCC09TBG	0.891	0.9	0.909	0.027	0.045	0.063	0.8	0.9	0.05	0.5
SCY305LFCC15TBG	1.485	1.5	1.515	0.045	0.075	0.105				
SCY305LFCC16TBG	1.584	1.6	1.616	0.048	0.080	0.112				2.0
SCY305LFCC17TBG	1.683	1.7	1.717	0.051	0.085	0.119				
SCY305LFCC18TBG	1.782	1.8	1.818	0.054	0.090	0.126				
SCY305LFCC20TBG	1.980	2.0	2.020	0.060	0.100	0.140	0.9	1.1		
SCY305LFCC22TBG	2.178	2.2	2.222	0.066	0.110	0.154				
SCY305LFCC23TBG	2.277	2.3	2.323	0.069	0.115	0.161				
SCY305LFCC24TBG	2.376	2.4	2.424	0.072	0.120	0.168				
SCY305LFCC25TBG	2.475	2.5	2.525	0.075	0.125	0.175				
SCY305LFCC26TBG	2.574	2.6	2.626	0.078	0.130	0.182				
SCY305LFCC27TBG	2.673	2.7	2.727	0.081	0.135	0.189				
SCY305LFCC28TBG	2.772	2.8	2.828	0.084	0.140	0.196				
SCY305LFCC29TBG	2.871	2.9	2.929	0.087	0.145	0.203				
SCY305LFCC30TBG	2.970	3.0	3.030	0.090	0.150	0.210	1.0	1.2		
SCY305LFCC31TBG	3.069	3.1	3.131	0.093	0.155	0.217				
SCY305LFCC32TBG	3.168	3.2	3.232	0.096	0.160	0.224				
SCY305LFCC33TBG	3.267	3.3	3.333	0.099	0.165	0.231				
SCY305LFCC34TBG	3.366	3.4	3.434	0.102	0.170	0.238				
SCY305LFCC35TBG	3.465	3.5	3.535	0.105	0.175	0.245				
SCY305LFCC36TBG	3.564	3.6	3.636	0.108	0.180	0.252				
SCY305LFCC37TBG	3.663	3.7	3.737	0.111	0.185	0.259				
SCY305LFCC40TBG	3.960	4.0	4.040	0.120	0.200	0.280	1.1	1.3		
SCY305LFCC44TBG	4.356	4.4	4.444	0.132	0.220	0.308				
SCY305LFCC45TBG	4.455	4.5	4.545	0.135	0.225	0.315				
SCY305LFCC47TBG	4.653	4.7	4.747	0.141	0.235	0.329				
SCY305LFCC49TBG	4.851	4.9	4.949	0.147	0.245	0.343				

5. Condition 1: 0.9 − 2.9 V, $V_{in} = V_{DET-} - 0.10$ V; 3.0 − 3.9 V, $V_{in} = V_{DET-} - 0.13$ V; 4.0 − 4.9 V, $V_{in} = V_{DET-} - 0.16$ V
6. Condition 2: 0.9 − 4.9 V, $V_{in} = V_{DET-} + 2.0$ V
7. Condition 3: 0.9 − 4.9 V, V_{in} = 0.7 V, V_{OUT} = 0.05 V, Active Low ‘L’ Suffix Devices
8. Condition 4: 0.9 − 1.0 V, V_{in} = 0.85 V, V_{OUT} = 0.5 V; 1.1 − 1.5 V, V_{in} = 1.0 V, V_{OUT} = 0.5 V; 1.6 − 4.9 V, V_{in} = 1.5 V, V_{OUT} = 0.5 V, Active Low ‘L’ Suffix Devices

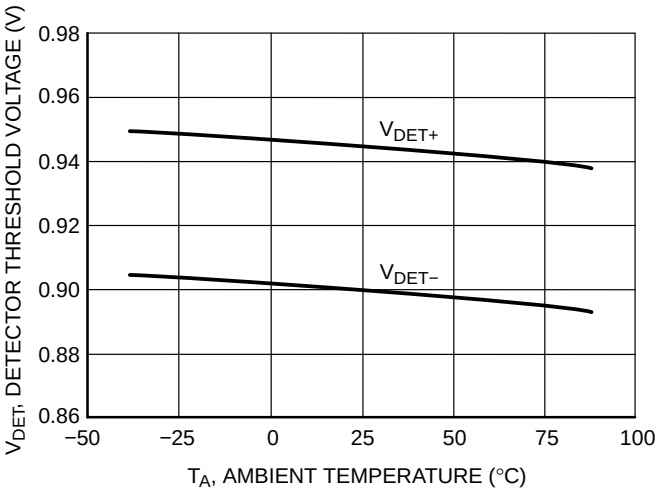


Figure 3. SCY305 Series 0.9 V Detector Threshold Voltage vs. Temperature

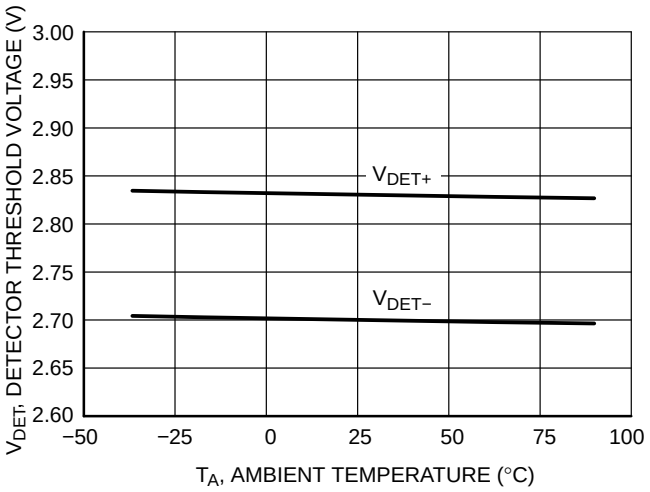


Figure 4. SCY305 Series 2.7 V Detector Threshold Voltage vs. Temperature

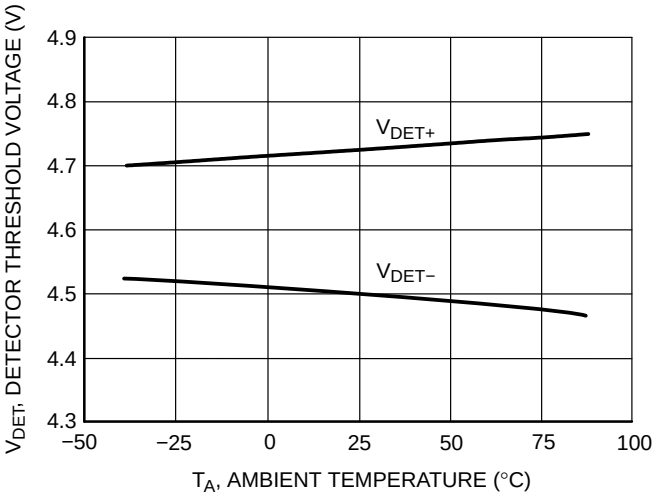


Figure 5. SCY305 Series 4.5 V Detector Threshold Voltage vs. Temperature

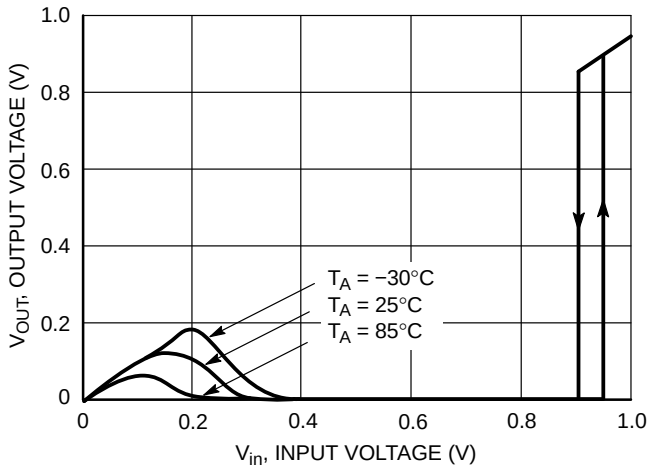


Figure 6. SCY305L Series 0.9 V Reset Output Voltage vs. Input Voltage

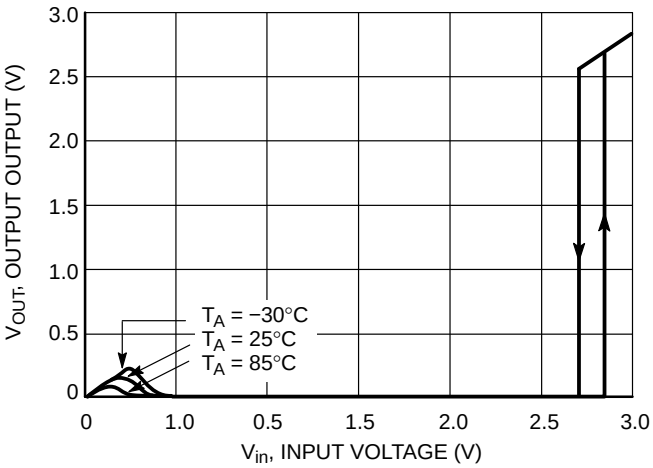


Figure 7. SCY305L Series 2.7 V Reset Output Voltage vs. Input Voltage

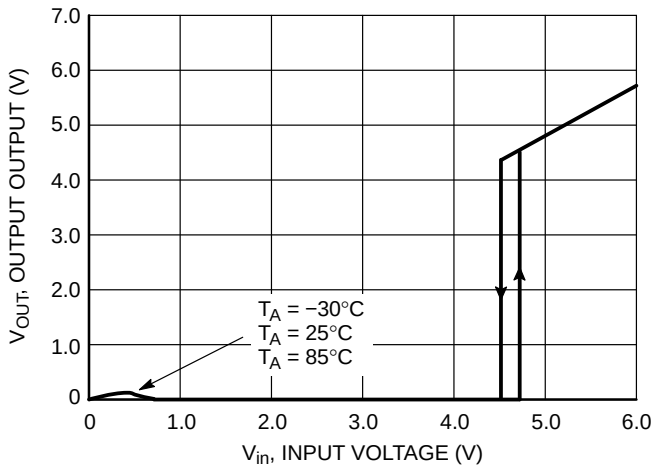


Figure 8. SCY305L Series 4.5 V Reset Output Voltage vs. Input Voltage

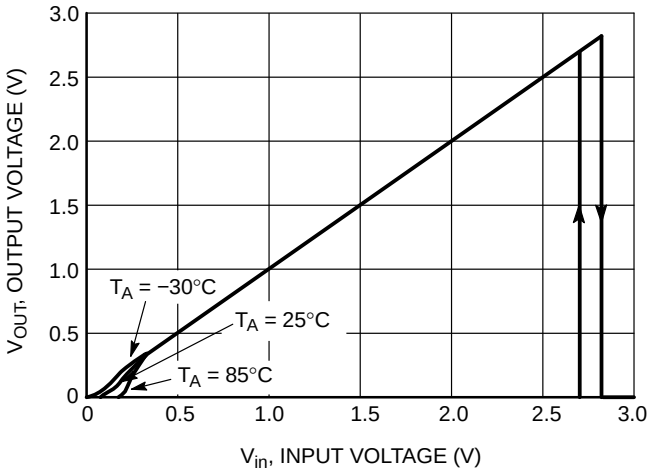


Figure 9. SCY305H Series 2.7 V Reset Output Voltage vs. Input Voltage

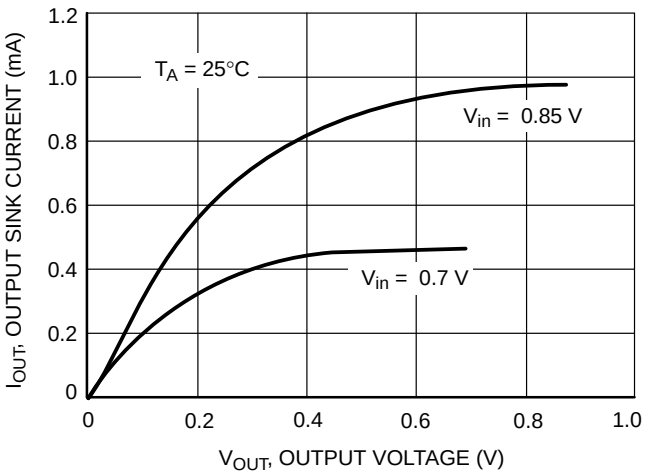


Figure 10. SCY305L Series 0.9 V Reset Output Sink Current vs. Output Voltage

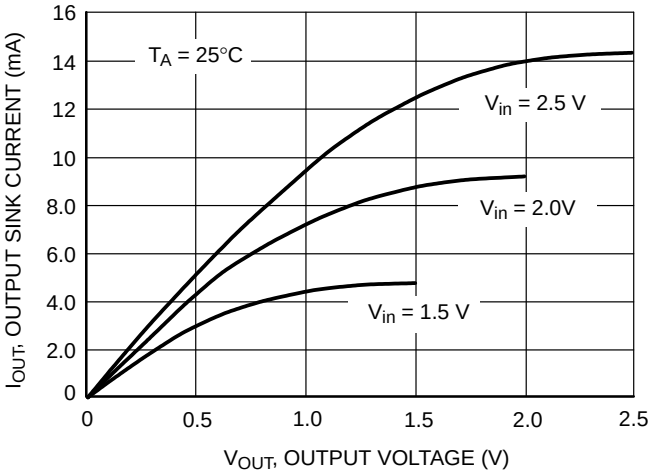


Figure 11. SCY305L Series 2.7 V Reset Output Sink Current vs. Output Voltage

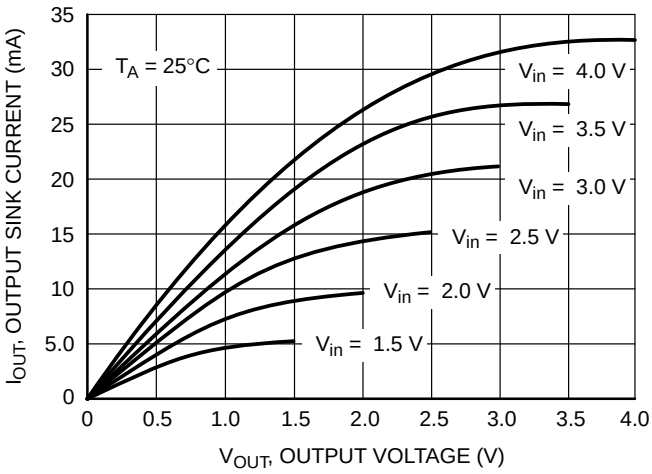


Figure 12. SCY305L Series 4.5 V Reset Output Sink Current vs. Output Voltage

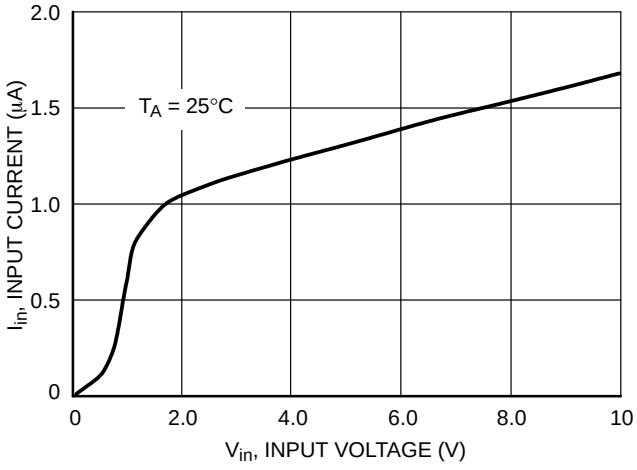


Figure 13. SCY305 Series 0.9 V Input Current vs. Input Voltage

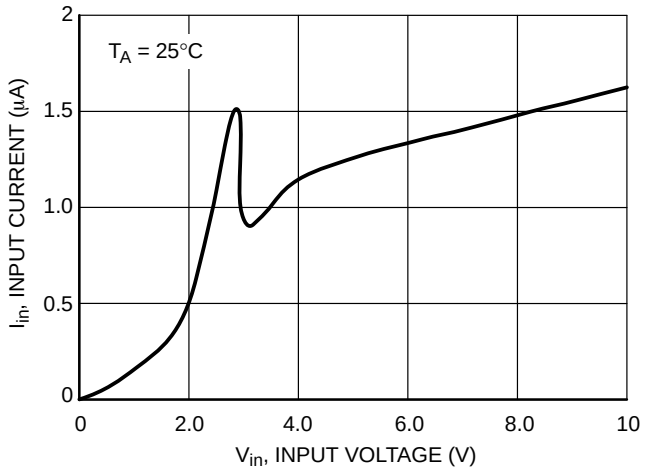


Figure 14. SCY305 Series 2.7 V Input Current vs. Input Voltage

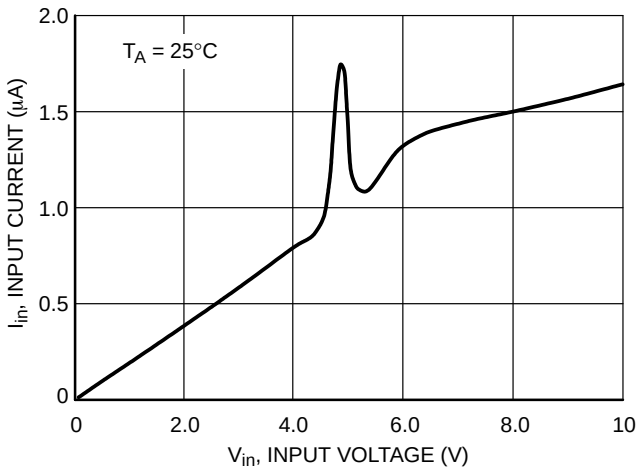


Figure 15. SCY305 Series 4.5 V Input Current vs. Input Voltage

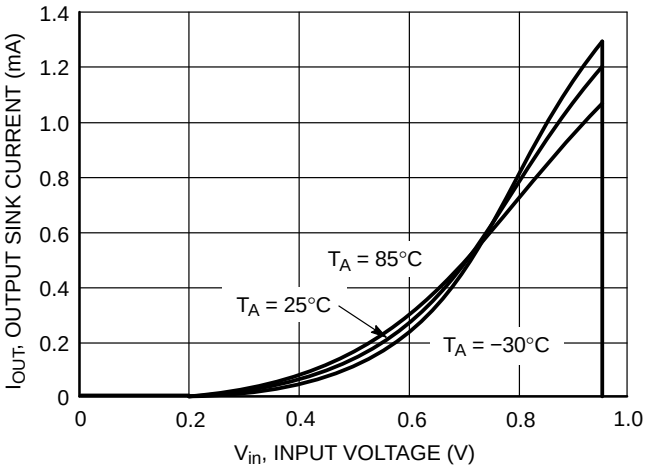


Figure 16. SCY305L Series 0.9 V Reset Output Sink Current vs. Input Voltage

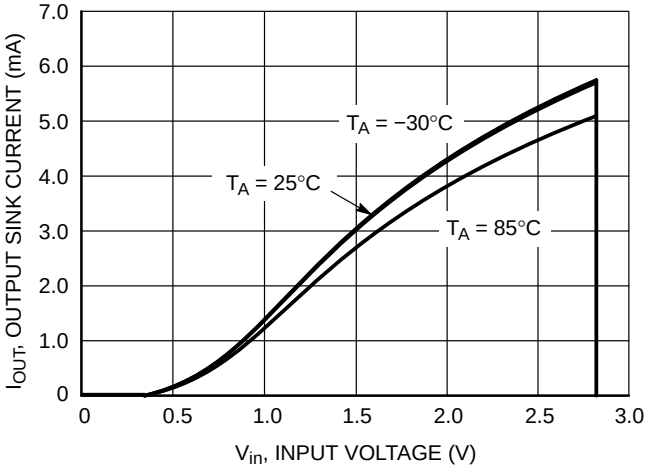


Figure 17. SCY305L Series 2.7 V Reset Output Sink Current vs. Input Voltage

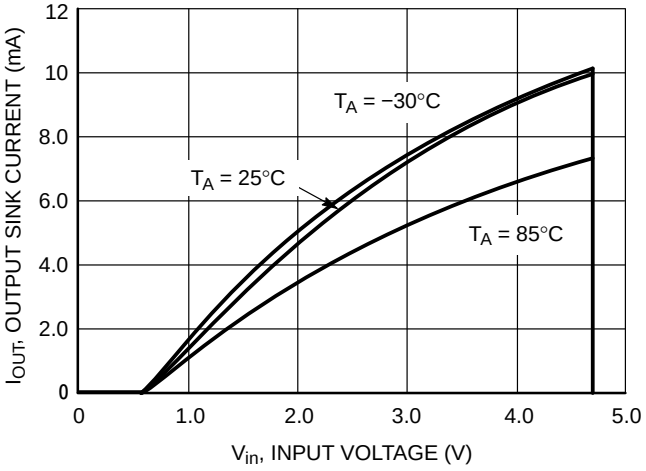


Figure 18. SCY305L Series 4.5 V Reset Output Sink Current vs. Input Voltage

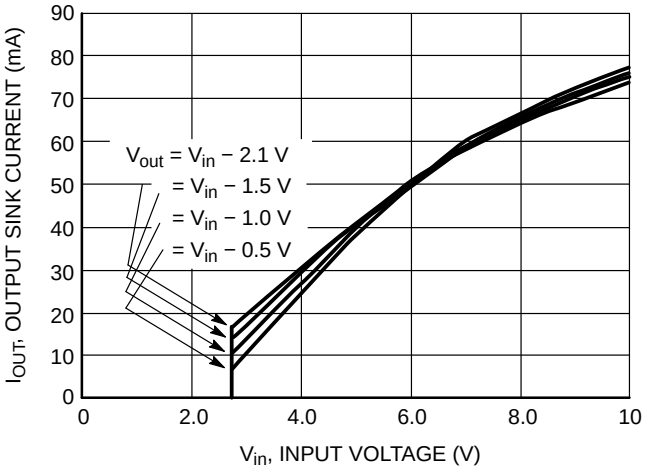


Figure 19. SCY305H Series 2.7 V Reset Output Sink Current vs. Input Voltage

OPERATING DESCRIPTION

The SCY305 series devices are second generation ultra−low current voltage detectors. Figures 20 and 21 show a timing diagram and a typical application. Initially consider that input voltage V_{in} is at a nominal level and it is greater than the voltage detector upper threshold (V_{DET+}), and the reset output (Pin 1) will be in the high state for active low devices, or in the low state for active high devices. If there is a power interruption and V_{in} becomes significantly deficient, it will fall below the lower detector threshold ($V_{DET−}$). This sequence of events causes the Reset output to be in the low state for active low devices, or in the high state for active high devices. After completion of the power interruption, V_{in} will again return to its nominal level and become greater than the V_{DET+}. The voltage detector has built−in hysteresis to prevent erratic reset operation as the comparator threshold is crossed.

Although these device series are specifically designed for use as reset controllers in portable microprocessor based systems, they offer a cost−effective solution in numerous applications where precise voltage monitoring is required. Figure 21 through Figure 27 shows various application examples.

“L” in Part Name	“H” in Part Name
Function: active Low Reset Output	Function: active High Reset Output
Input < Vdet−, Reset Output is Low	Input < Vdet−, Reset Output is High
Input > Vdet+, Reset Output is High	Input > Vdet+, Reset Output is Low

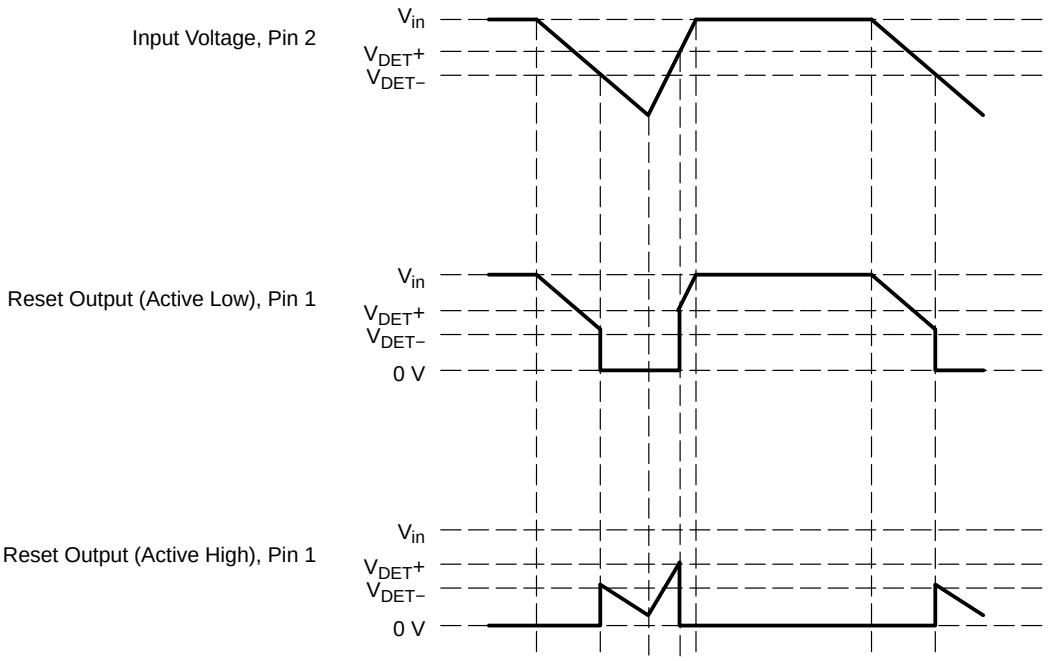


Figure 20. Timing Waveforms

APPLICATION CIRCUIT INFORMATION

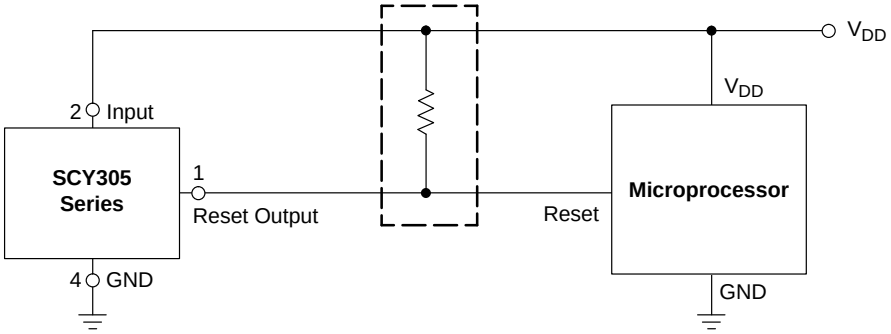


Figure 21. Microprocessor Reset Circuit

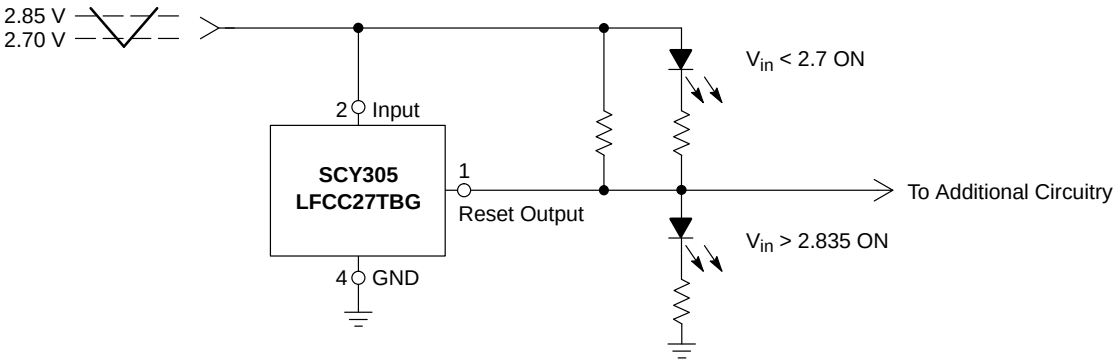


Figure 22. Battery Charge Indicator

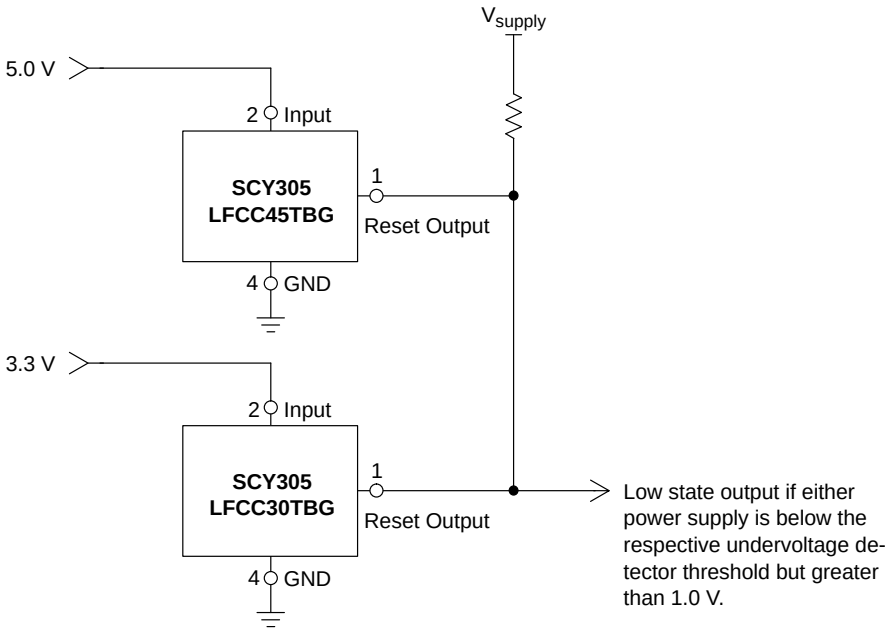


Figure 23. Dual Power Supply Undervoltage Supervision

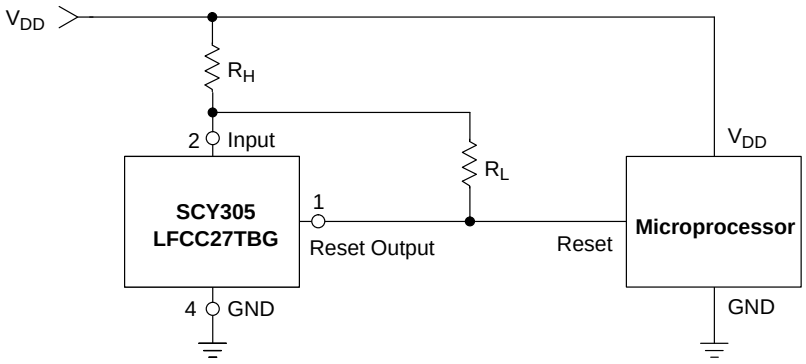


Figure 24. Microprocessor Reset Circuit with Additional Hysteresis

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equations have been simplified and do not account for the change of input current I_{in} as V_{in} crosses the comparator threshold. The internal resistance, R_{in} is simply calculated using I_{in} = 0.26 μA at 2.6 V.

V_{in} Decreasing:

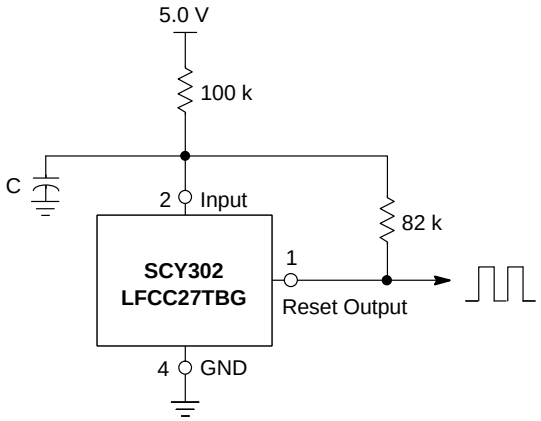
$$V_{th} = \left(\frac{R_H}{R_{in}} + 1\right)(V_{DET-})$$

V_{in} Increasing:

$$V_{th} = \left(\frac{R_H}{R_{in} \parallel R_L} + 1\right)(V_{DET-} + V_{HYS})$$

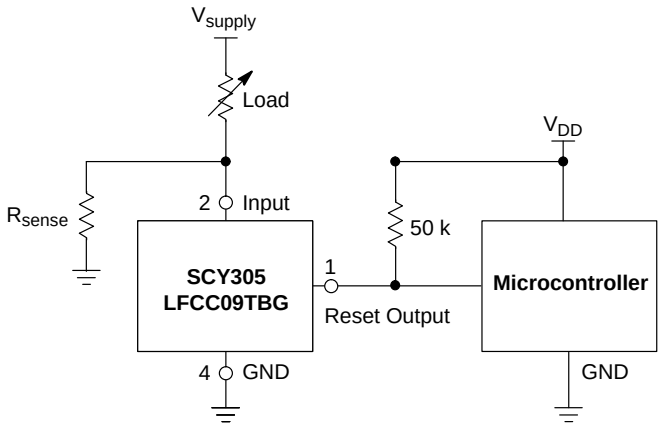
V_{HYS} = V_{in} Increasing − V_{in} Decreasing

Test Data				
V_{th} Decreasing (mV)	V_{th} Increasing (mV)	V_{HYS} (mV)	R_H (Ω)	R_L (kΩ)
2.70	2.84	0.135	0	–
2.70	2.87	0.17	100	10
2.70	2.88	0.19	100	6.8
2.70	2.91	0.21	100	4.3
2.70	2.90	0.20	220	10
2.70	2.94	0.24	220	6.8
2.70	2.98	0.28	220	4.3
2.70	2.70	0.27	470	10
2.70	3.04	0.34	470	6.8
2.70	3.15	0.35	470	4.3



Test Data		
C (μF)	f_{OSC} (kHz)	I_Q (μA)
0.01	2590	21.77
0.1	490	21.97
1.0	52	22.07

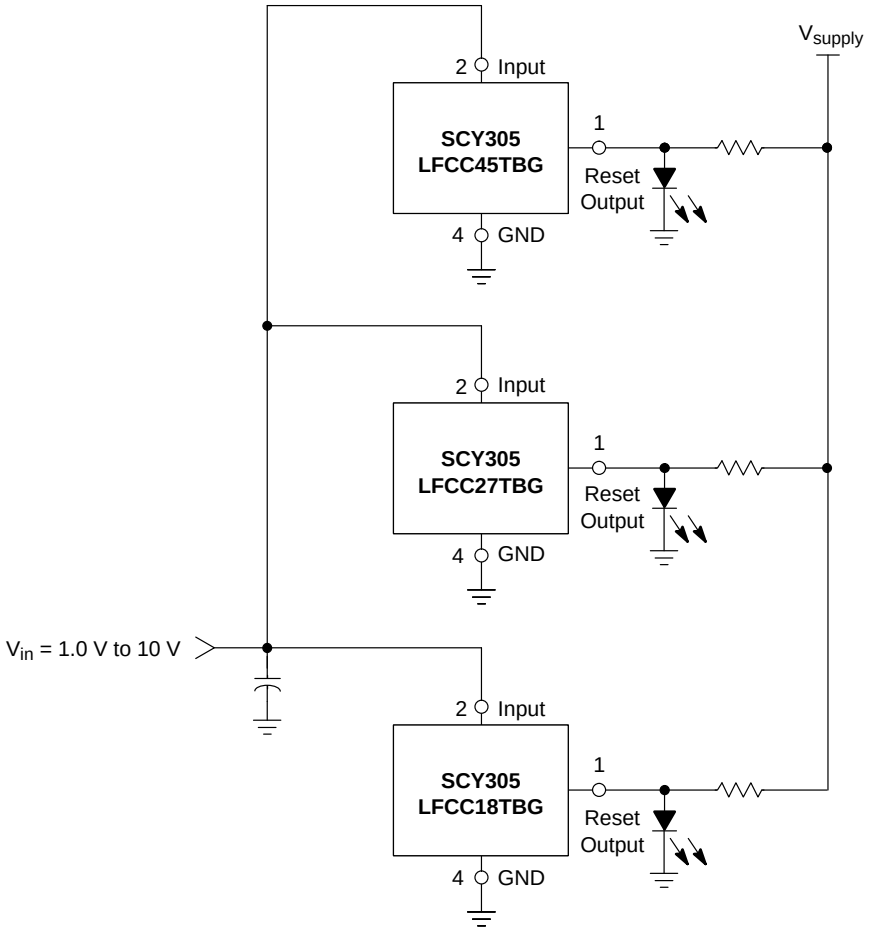
Figure 25. Simple Clock Oscillator



This circuit monitors the current at the load. As current flows through the load, a voltage drop with respect to ground appears across R_{sense} where $V_{sense} = I_{load} * R_{sense.}$ The following conditions apply:

If:	Then:
$I_{Load} < V_{DET-}/R_{sense}$	Reset Output = 0 V
$I_{Load} \geq (V_{DET-}+V_{HYS})/R_{sense}$	Reset Output = V_{DD}

Figure 26. Microcontroller Systems Load Sensing



A simple voltage monitor can be constructed by connecting several voltage detectors as shown above. Each LED will sequentially turn on when the respective voltage detector threshold (V_{DET-} +V_{HYS}) is exceeded. Note that detector thresholds (V_{DET-}) that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

Figure 27. LED Bar Graph

ORDERING INFORMATION

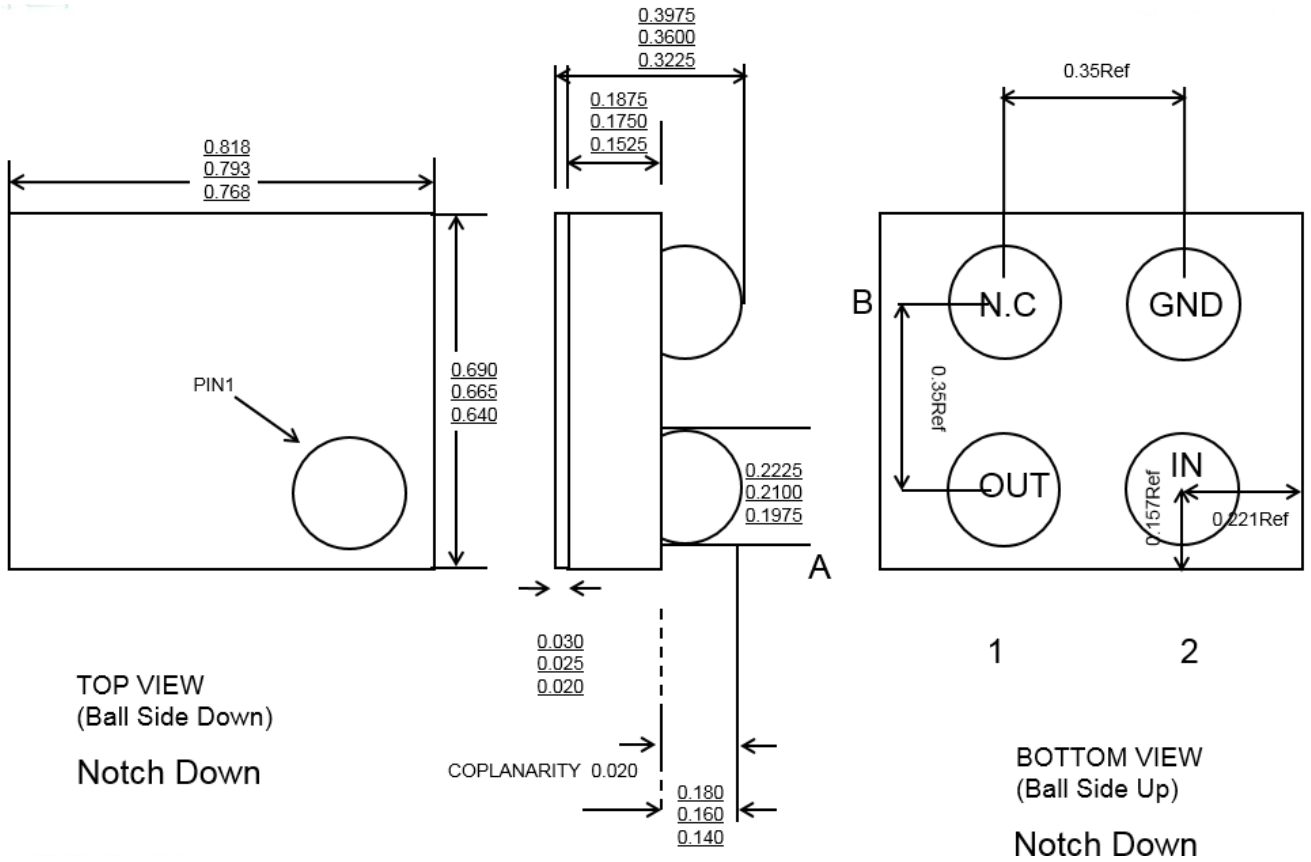
Device	Threshold Voltage	Output Type	Reset	Marking	Package	Shipping†	T&R Orientation
SCY305LFCC32TBG	3.2	Open Drain	Active Low	TBD	WLCSP	3000 / Tape & Reel	Pin 1 Upper Right Quadrant toward sprocket hole

NOTE: The ordering information lists standard undervoltage thresholds with active low outputs. Additional active low threshold devices, ranging from 0.9 V to 4.9 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability. The electrical characteristics of these additional devices are shown in Tables 2 and 3.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

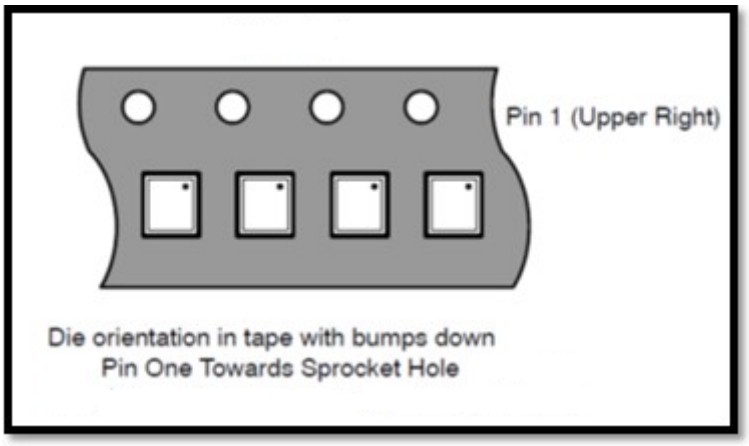
PACKAGE DIMENSIONS

WLCSP4
CASE TBD
ISSUE O



SCY305

WLCSP Tape and Reel Orientation



Package	Tape Width mm	Pitch mm (Dimension P1) (inch)	Reel Size		Devices Per Reel & Min Order Quantity	T&R Suffix
			(mm)	(in)		
WLCSP 4−Bump 0.69x0.82mm	8	2.0+−0.05 (0.079+−0.002)	178	7	3000	TB

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