SCY99254C

Single 1 A High-Speed, Low-Side Gate Driver

Description

The SCY99254C 1 A gate driver is designed to drive an N−channel enhancement−mode MOSFET in low−side switching applications.

SCY99254C has dual CMOS inputs with thresholds referenced to V_{DD} for use with PWM controllers and other input−signal sources that operate from the same supply voltage as the driver.

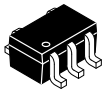
The SCY99254C is available in a lead−free finish industry−standard 5−pin SOT23.

Features

- 1.4 A Peak Sink / Source at V_{DD} = 12 V
- 1.1 A Sink / 0.9 A Source at V_{OUT} = 6 V
- 4.5 to 18 V Operating Range
- Two Input Configurations:
  - Dual CMOS Inputs Allow Configuration as Non−Inverting or Inverting with Enable Function
  - Single Non−Inverting, Low−Voltage Input for Compatibility with Low−Voltage Controllers
- Small Footprint Facilitates Distributed Drivers for Parallel Power Devices
- 15 ns Typical Delay Times
- 9 ns Typical Rise / 8 ns Typical Fall Times with 470 pF Load
- 5−Pin SOT23 Package
- Rated from –40°C to 125°C Ambient

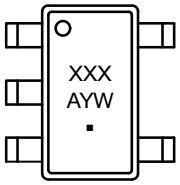
Applications

- Switch−Mode Power Supplies
- Synchronous Rectifier Circuits
- Pulse Transformer Driver
- Logic to Power Buffer
- Motor Control



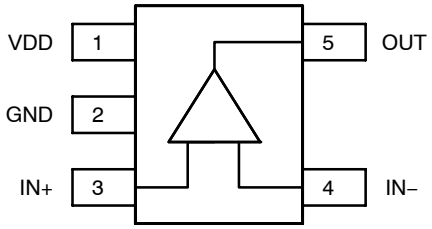
SOT−23
5−LEAD
CASE 527AH

MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN ASSIGNMENT



SCY99254C (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Input Threshold	Package	Packing Method	Quantity per Reel
SCY99254CSX	CMOS	5−Pin SOT23	Tape & Reel	3,000

Table 1. THERMAL CHARACTERISTICS (Note 1)

Package	Θ_{JL} (Note 2)	Θ_{JT} (Note 3)	Θ_{JA} (Note 4)	Ψ_{JB} (Note 5)	Ψ_{JT} (Note 6)	Units
5−Pin SOT23	58	102	161	53	6	°C/W

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top−side heatsink.
4. Theta_JA (θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board,, as specified in JEDEC standards JESD51−2, JESD51−5, and JESD51−7, as appropriate.
5. Psi_JB (ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the MLP−8 package, the board reference is defined as the pcb copper connected to the thermal pad and protruding from either end of the package. For the SOIC−8 package, the board reference is defined as the pcb copper adjacent to pin 6.
6. Psi_JT (ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

Table 2. PIN DEFINITIONS

Pin #	Name	Description
1	VDD	Supply Voltage. Provides power to the IC.
2	GND	Ground. Common ground reference for input and output circuits.
3	IN+	Non−Inverting Input. Connect to VDD to enable output.
4	IN−	SCY99254C Inverting Input. Connect to GND to enable output.
5	OUT	Gate Drive Output. Held low unless required inputs are present.

Table 3. OUTPUT LOGIC WITH DUAL−INPUT CONFIGURATION

IN+	IN−	OUT
0 (Note 7)	0	0
0 (Note 7)	1 (Note 7)	0
1	0	1
1	1 (Note 7)	0

7. Default input signal if no external connection is made.

Block Diagrams

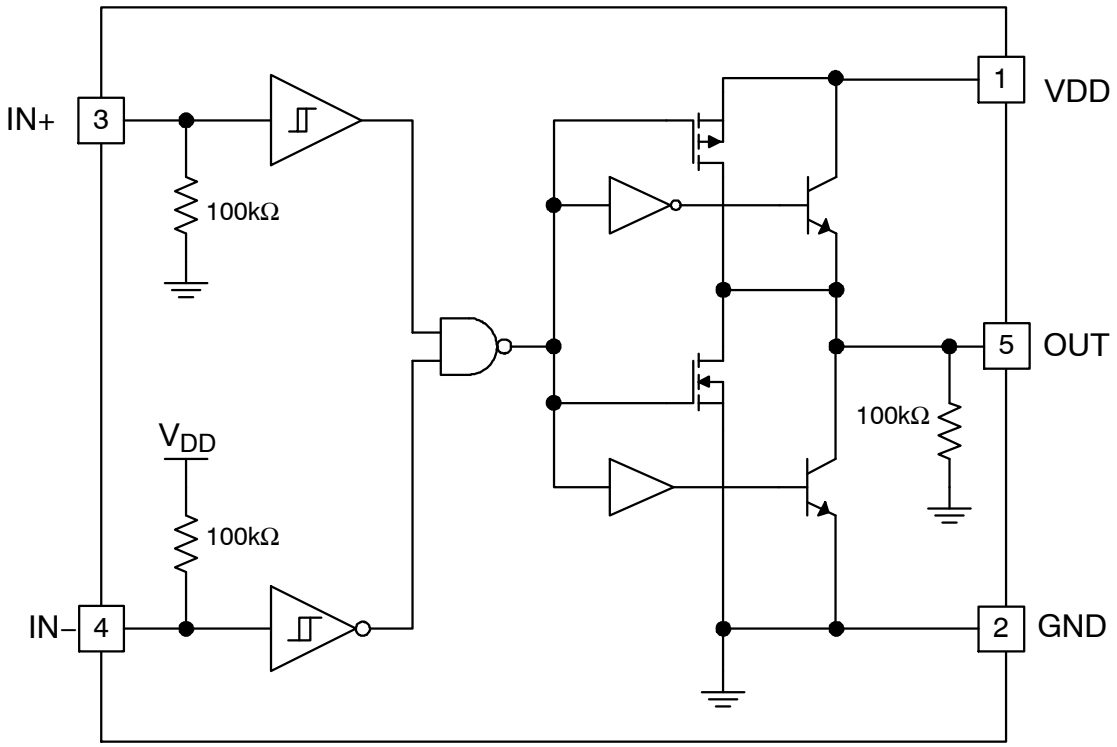


Figure 1. SCY99254C Simplified Block Diagram

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	VDD to GND	−0.3	20.0	V
V_{IN}	Voltage on IN to GND	−0.3	V_{DD} + 0.3	V
V_{OUT}	Voltage on OUT to GND	−0.3	V_{DD}+0.3	V
T_L	Lead Soldering Temperature (10 Seconds)		+260	°C
T_J	Junction Temperature		+150	°C
T_{STG}	Storage Temperature	−65	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{IN}	Input Voltage IN	0	V_{DD}	V
T_A	Operating Ambient Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ELECTRICAL CHARACTERISTICS Unless otherwise noted, V_{DD} = 12 V, V_{XREF} = 3.3 V, T_J = −40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	Operating Range		4.5		18.0	V
I_{DD}	Static Supply Current	Inputs Not Connected		5	10	μA
INPUTS						
V_{IL_C}	IN Logic, Low−Voltage Threshold		30	38		$\%V_{DD}$
V_{IH_C}	IN Logic, High−Voltage Threshold			55	70	$\%V_{DD}$
I_{INL}	IN Current, Low	IN from 0 to V_{DD}	−1		175	μA
I_{INH}	IN Current, High	IN from 0 to V_{DD}	−175		1	μA
V_{HYS_C}	Input Hysteresis Voltage			17		$\%V_{DD}$
OUTPUT						
I_{SINK}	OUT Current, Mid−Voltage, Sinking (Note 8)	OUT at V_{DD}/2, C_{LOAD} = 47 nF, f = 1 KHz		1.1		A
I_{SOURCE}	OUT Current, Mid−Voltage, Sourcing (Note 8)	OUT at V_{DD}/2, C_{LOAD} = 47 nF, f = 1 KHz		−0.9		A
I_{PK_SINK}	OUT Current, Peak, Sinking (Note 8)	C_{LOAD} = 47 nF, f = 1 KHz		1.4		A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing (Note 8)	C_{LOAD} = 47 nF, f = 1 KHz		−1.4		A
t_{RISE}	Output Rise Time (Note 9)	C_{LOAD} = 470 pF		9	18	ns
t_{FALL}	Output Fall Time (Note 9)	C_{LOAD} = 470 pF		8	17	ns
t_{D1}, t_{D2}	Output Prop. Delay (Note 9)	0 − 12V_{IN}, 1V/ns Slew Rate		15	30	ns
I_{RVS}	Output Reverse Current Withstand (Note 8)			250		mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Not tested in production.
9. See Timing diagrams.

Timing Diagrams

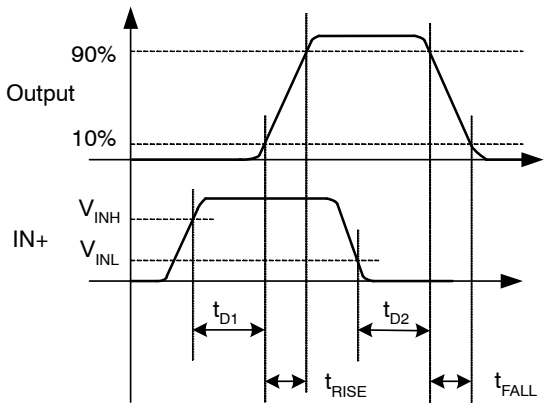


Figure 2. Non−Inverting Waveforms

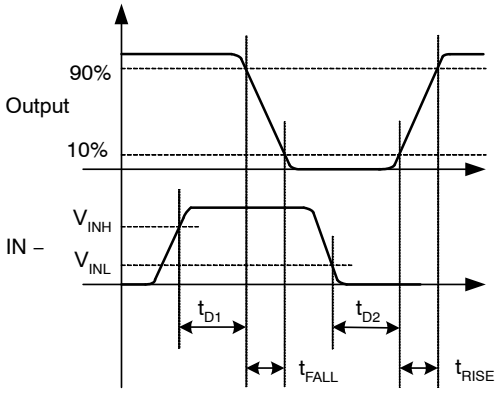


Figure 3. Inverting Waveforms

Typical Performance Characteristics

Typical characteristics are provided at 25°C, V_{DD} = 12 V, and V_{XREF} = 3.3 V unless otherwise noted.

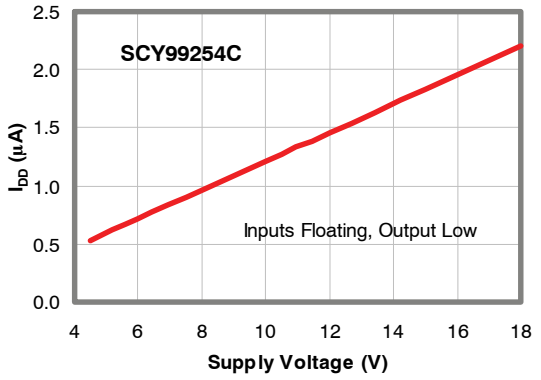


Figure 4. I_{DD} (Static) vs. Supply Voltage

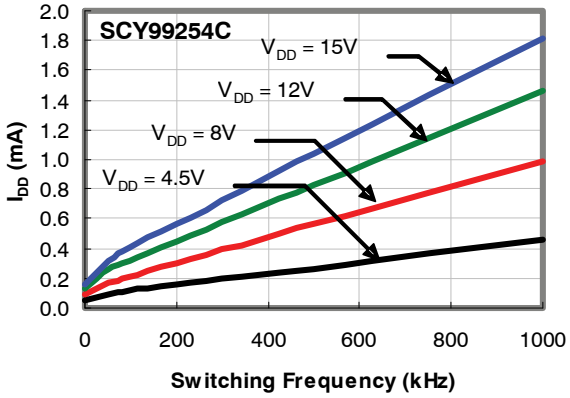


Figure 5. I_{DD} (No−Load) vs. Frequency

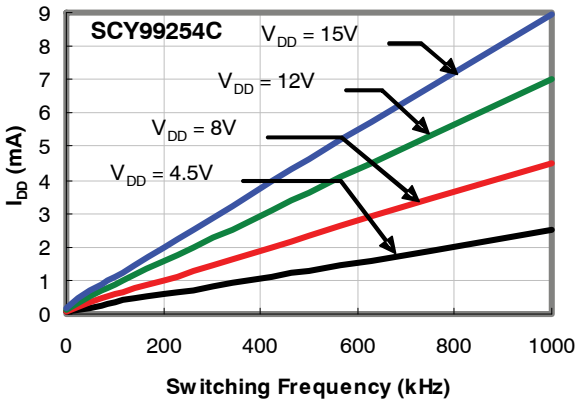


Figure 6. I_{DD} (470 pF Load) vs. Frequency

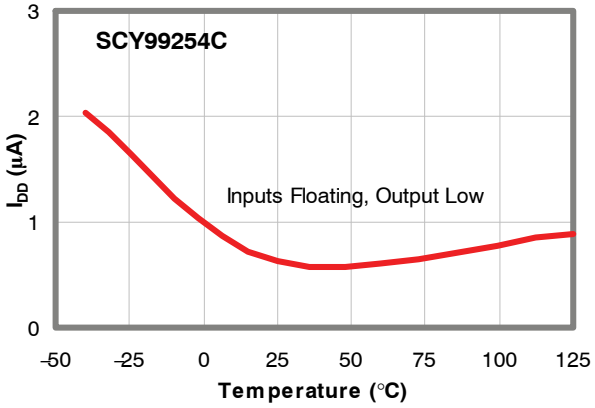


Figure 7. I_{DD} (Static) vs. Temperature

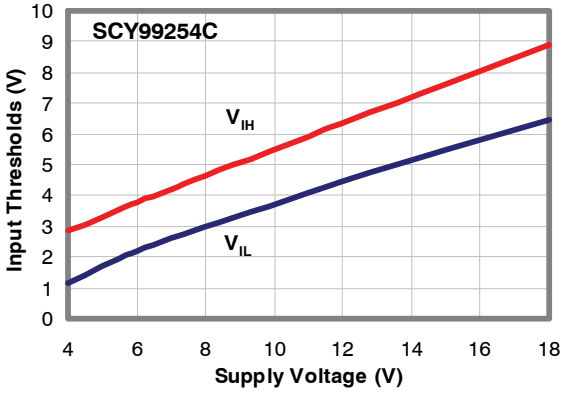


Figure 8. Input Thresholds vs. Supply Voltage

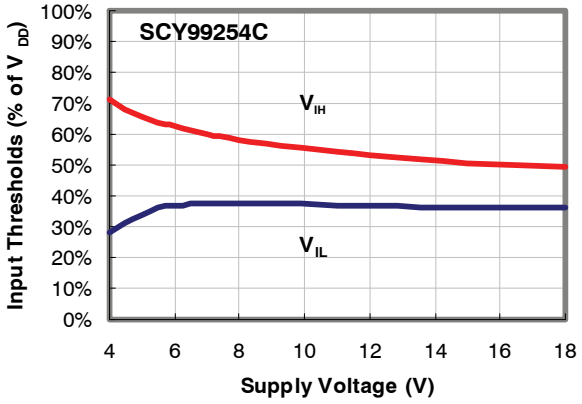


Figure 9. Input Thresholds % vs. Supply Voltage

Typical Performance Characteristics

Typical characteristics are provided at 25°C, V_{DD} = 12 V, and V_{XREF} = 3.3 V unless otherwise noted.

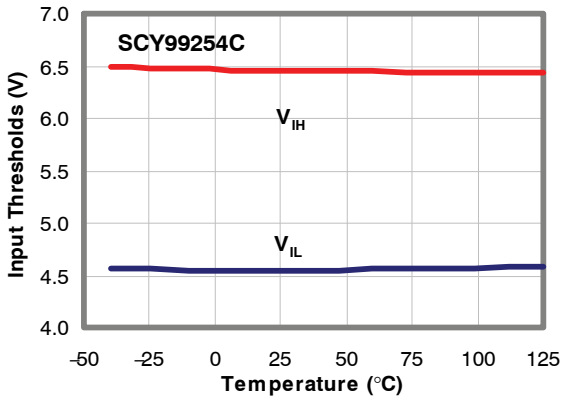


Figure 10. Input Threshold vs. Temperature

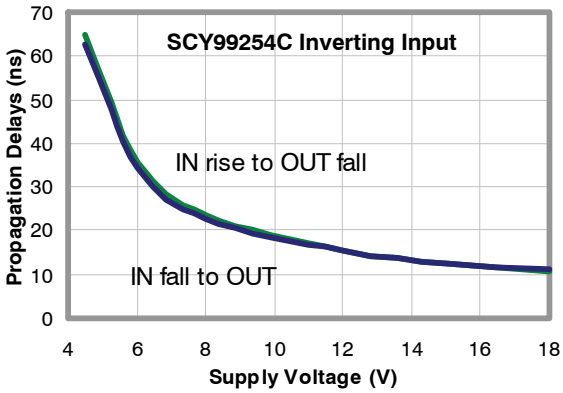


Figure 11. Propagation Delay vs. Supply Voltage

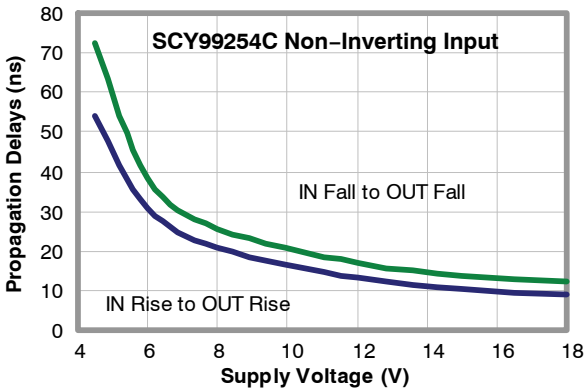


Figure 12. Propagation Delay vs. Supply Voltage

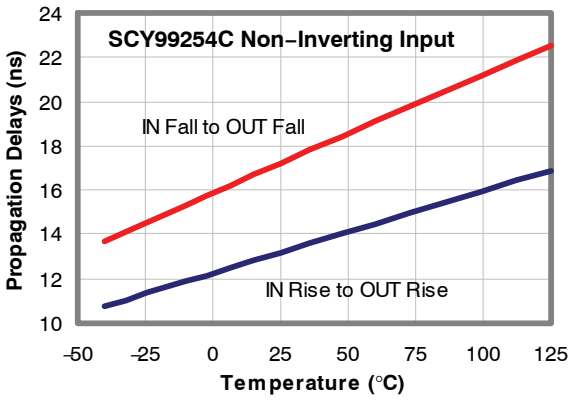


Figure 13. Propagation Delay vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at 25°C, V_{DD} = 12 V, and V_{XREF} = 3.3 V unless otherwise noted.

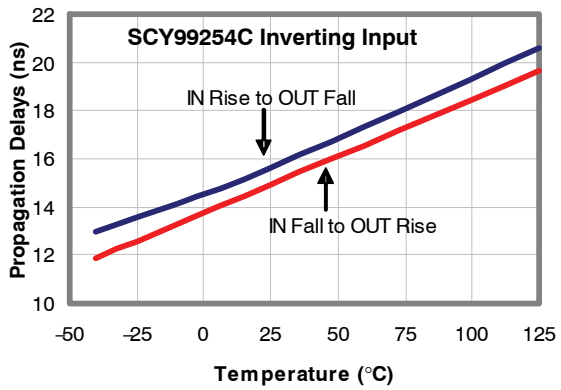


Figure 14. Propagation Delays vs. Temperature

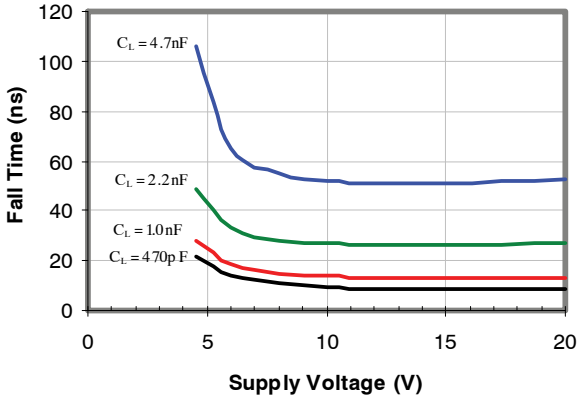


Figure 15. Fall Time vs. Supply Voltage

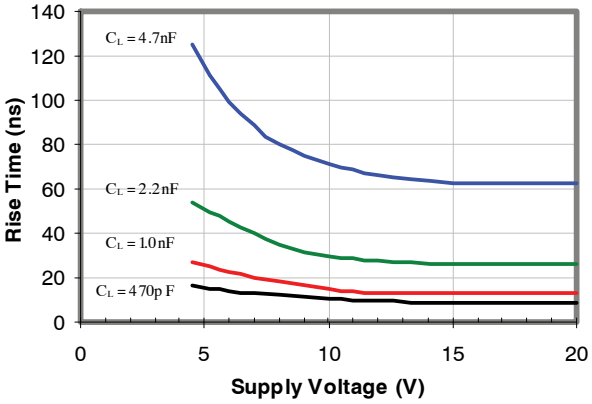


Figure 16. Rise Time vs. Supply Voltage

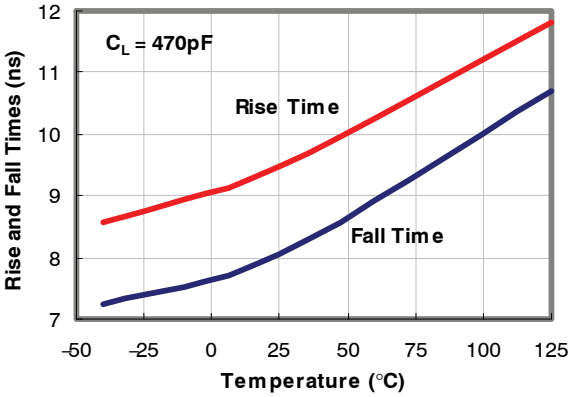


Figure 17. Rise and Fall Time vs. Temperature

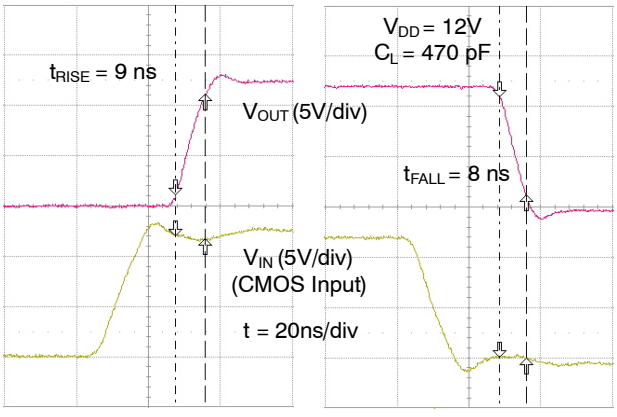


Figure 18. Rise and Fall Waveforms (470 pF)

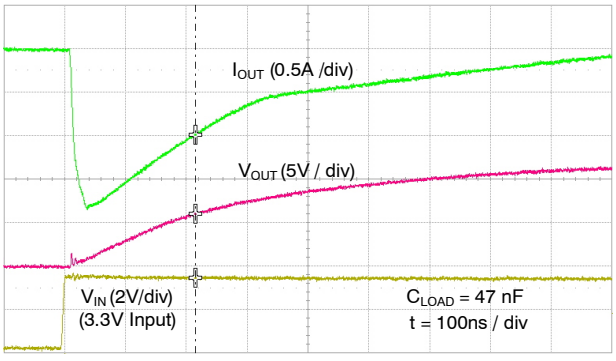


Figure 19. Quasi−Static Source Current (V_{DD} = 12 V)

Typical Performance Characteristics

Typical characteristics are provided at 25°C, V_{DD} = 12 V, and V_{XREF} = 3.3 V unless otherwise noted.

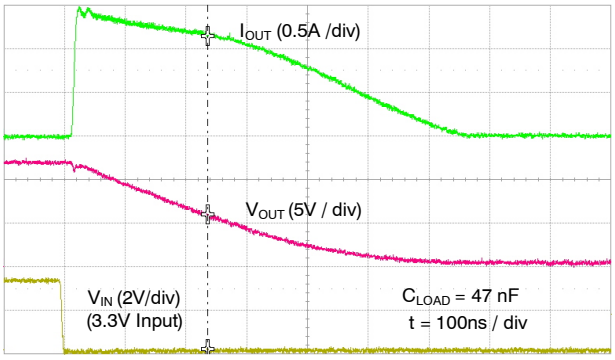


Figure 20. Quasi−Static Sink Current (V_{DD} = 12 V)

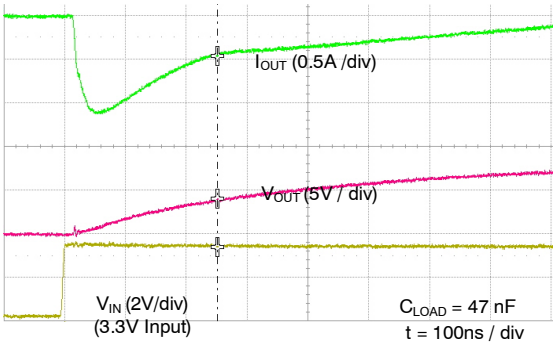


Figure 21. Quasi−Static Source Current (V_{DD} = 8 V)

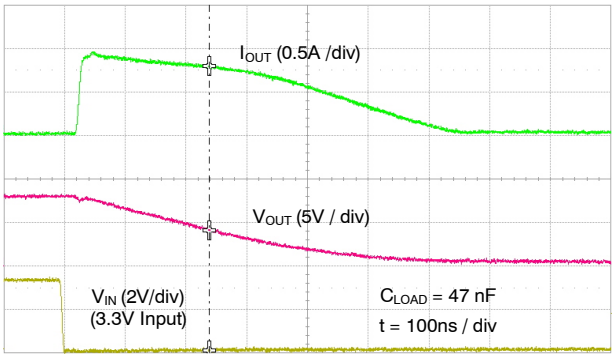


Figure 22. Quasi−Static Sink Current (V_{DD} = 8 V)

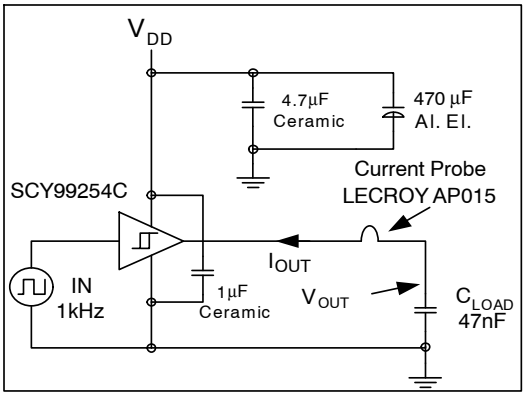


Figure 23. Quasi−Static I_{OUT} / V_{OUT} Test Circuit

Applications Information

The SCY99254C offers CMOS− or logic−level−compatible input thresholds. In the SCY99254C, the logic input thresholds are dependent on the V_{DD} level and, with V_{DD} of 12 V, the logic rising−edge threshold is approximately 55% of V_{DD} and the input falling−edge threshold is approximately 38% of V_{DD}. The CMOS input configuration offers a hysteresis voltage of approximately 17% of V_{DD}. The CMOS inputs can be used with relatively slow edges (approaching DC) if good decoupling and bypass techniques are incorporated in the system design to prevent noise from violating the input−voltage hysteresis window. This allows setting precise timing intervals by fitting an R−C circuit between the controlling signal and the IN pin of the driver. The slow rising edge at the IN pin of the driver introduces a delay between the controlling signal and the OUT pin of the driver.

Startup Operation

The SCY99254C internal logic is optimized to drive ground referenced N−channel MOSFETs as V_{DD} supply voltage rises during startup operation. As V_{DD} rises from 0V to approximately 2 V, the OUT pin is held LOW by an internal resistor, regardless of the state of the input pins. When the internal circuitry becomes active at approximately 2 V, the output assumes the state commanded by the inputs.

Figure 24 illustrates SCY99254C startup operation with V_{DD} increasing from 0 to 12 V, with the output commanded to the low level (IN+ and IN− tied to ground). Note that OUT is held LOW to maintain an N−channel MOSFET in the OFF state.

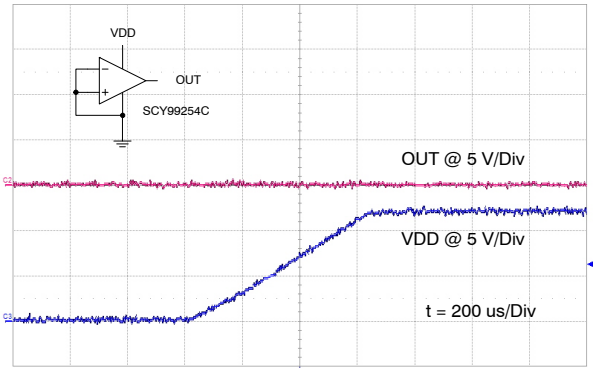


Figure 24. SCY99254C Startup Operation

Figure 25 illustrates startup operation as V_{DD} increases from 0 to 12 V with the output commanded to the high level (IN+ tied to VDD, IN− tied to GND). This configuration might not be suitable for driving high−side P−channel MOSFETs because the low output voltage of the driver would attempt to turn the P−channel MOSFET on with low V_{DD} levels.

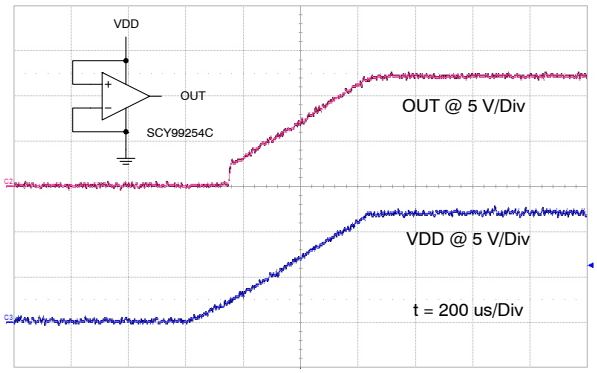


Figure 25. Startup Operation as V_{DD} Increases

MillerDrive Gate Drive Technology

SCY99254C drivers incorporate the MillerDrive architecture shown in Figure 26 for the output stage, a combination of bipolar and MOS devices capable of providing large currents over a wide range of supply−voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive architecture is to speed up switching by providing the highest current during the Miller plateau region when the gate−drain capacitance of the MOSFET is being charged or discharged as part of the turn−on / turn−off process. For applications with zero voltage switching during the MOSFET turn−on or turn−off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output−pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but if a slower rise or fall time at the MOSFET gate is needed, a series resistor can be added.

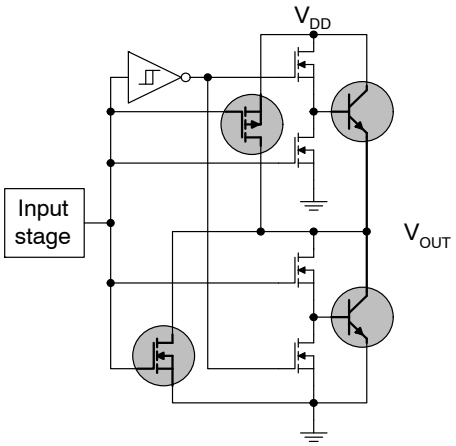


Figure 26. MillerDrive Output Architecture

V_{DD} Bypass Capacitor Guidelines

To enable this IC to turn a power device on quickly, a local, high−frequency, bypass capacitor C_{BYP} with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 μF to 47 μF often found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply ≤5%. Often this is achieved with a value ≥ 20 times the equivalent load capacitance C_{EQV}, defined here as Q_{gate}/V_{DD}. Ceramic capacitors of 0.1 μF to 1 μF or larger are common choices, as are dielectrics, such as X5R and X7R, which have good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50−100 times the C_{EQV} or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1−10 nF, mounted closest to the VDD and GND pins to carry the higher−frequency components of the current pulses.

Layout and Connection Guidelines

The SCY99254C incorporates fast reacting input circuits, short propagation delays, and output stages capable of delivering current peaks over 1 A to facilitate voltage transition times from under 10 ns to over 100 ns. The following layout and connection guidelines are strongly recommended:

- Keep high−current output and power ground paths separate from logic input signals and signal ground paths. This is especially critical when dealing with TTL−level logic thresholds.
- Keep the driver as close to the load as possible to minimize the length of high−current traces. This reduces the series inductance to improve high−speed switching, while reducing the loop area that can radiate EMI to the driver inputs and other surrounding circuitry.
- Many high−speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re−triggering. These effects can be especially obvious if the circuit is tested in breadboard or non−optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn−on and turn−off current paths should be minimized as discussed in the following sections.

Figure 27 shows the pulsed gate−drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, C_{BYP}, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak−current pulses within this driver−MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

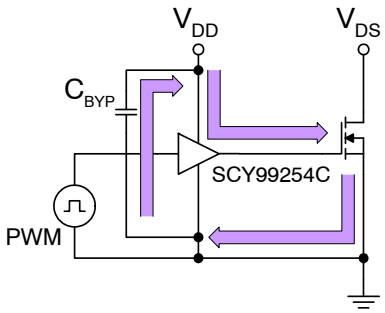


Figure 27. Current Path for MOSFET Turn−On

Figure 28 shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn−off times, the resistance and inductance in this path should be minimized.

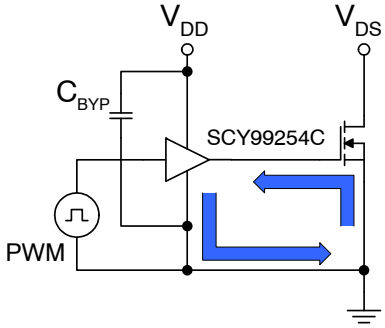


Figure 28. Current Path for MOSFET Turn−Off

Truth Table of Logic Operation

The SCY99254C truth table indicates the operational states using the dual−input configuration. In a non−inverting driver configuration, the IN− pin should be a logic low signal. If the IN− pin is connected to logic high, a disable function is realized, and the driver output remains low regardless of the state of the IN+ pin.

Table 7. SCY99254C TRUTH TABLE

IN+	IN−	OUT
0	0	0
0	1	0
1	0	1
1	1	0

In the non−inverting driver configuration in Figure 29, the IN− pin is tied to ground and the input signal (PWM) is applied to the IN+ pin. The IN− pin can be connected to logic high to disable the driver and the output remains low, regardless of the state of the IN+ pin.

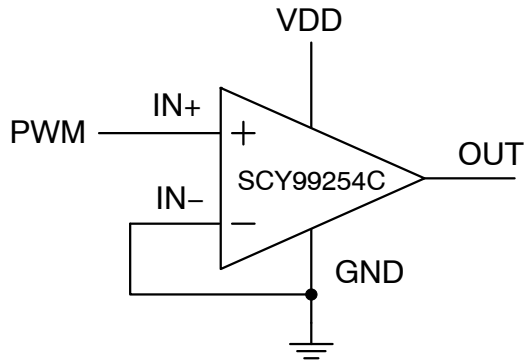


Figure 29. Dual−Input Driver Enabled, Non−Inverting Configuration

In the inverting driver application shown in Figure 30, the IN+ pin is tied high. Pulling the IN+ pin to GND forces the output low, regardless of the state of the IN− pin.

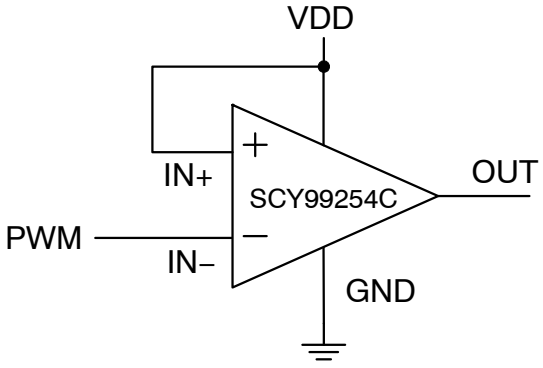


Figure 30. Dual−Input Driver Enabled, Inverting Configuration

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of three components; P_{GATE}, $P_{QUIESCENT}$, and $P_{DYNAMIC}$:

$$P_{total} = P_{gate} + P_{Dynamic} \quad \text{(eq. 1)}$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate−source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \cdot V_{GS} \cdot f_{SW} \quad \text{(eq. 2)}$$

Dynamic Pre−drive / Shoot−through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull−up / pull−down resistors, can be obtained using the graphs in Figure 6 in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \cdot V_{DD} \quad \text{(eq. 3)}$$

Once the power dissipated in the driver is determined, the driver junction temperature rise with respect to the device lead can be evaluated using thermal equation:

$$T_J = P_{TOTAL}\,\theta_{JL} + T_C \quad \text{(eq. 4)}$$

where:

T_J = driver junction temperature;

Θ_{JL} = thermal resistance from junction to lead; and

T_L = lead temperature of device in application.

The power dissipated in a gate−drive circuit is independent of the drive−circuit resistance and is split proportionately among the resistances present in the driver, any discrete series resistor present, and the gate resistance internal to the power switching MOSFET. Power dissipated in the driver may be estimated using the following equation:

$$P_{PKG} = P_{TOTAL}\left(\frac{R_{OUT,Driver}}{R_{OUT,DRIVER} + R_{EXT} + R_{GATE,FET}}\right) \quad \text{(eq. 5)}$$

where:

P_{PKG} = power dissipated in the driver package;

$R_{OUT,DRIVER}$ = estimated driver impedance derived from I_{OUT} vs. V_{OUT} waveforms;

R_{EXT} = external series resistance connected between the driver output and the gate of the MOSFET; and

$R_{GATE,FET}$ = resistance internal to the load MOSFET gate and source connections.

Typical Application Diagrams

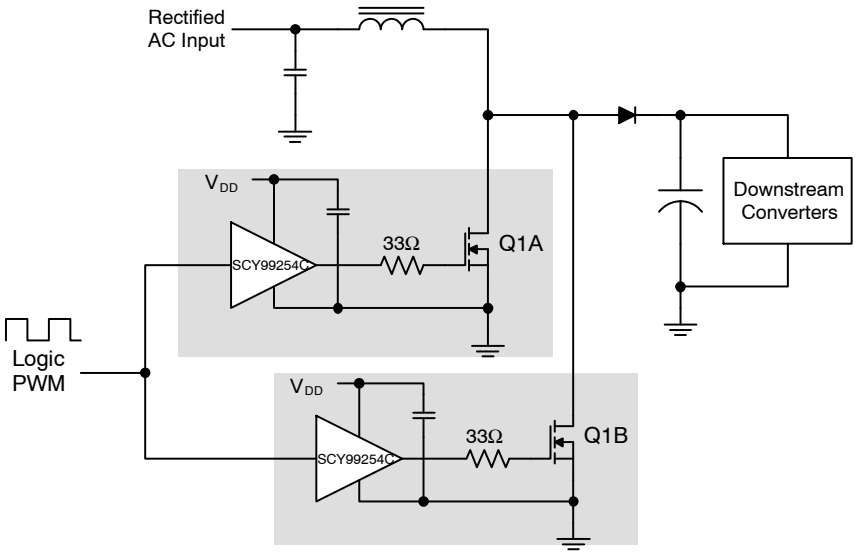


Figure 31. PFC Boost Circuit Utilizing Distributed Drivers for Parallel Power Switches Q1A and Q1B

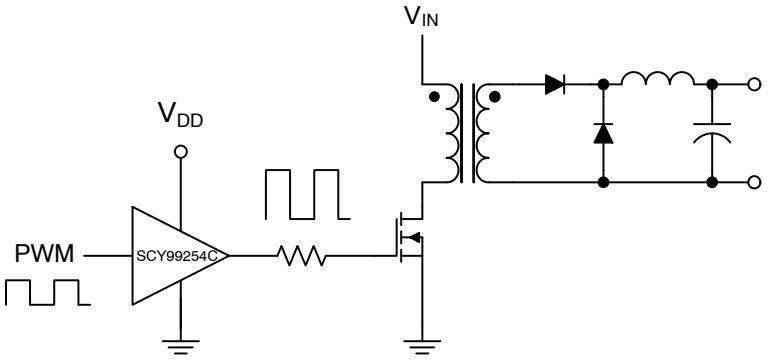


Figure 32. Driver for Forward Converter Low−Side Switch

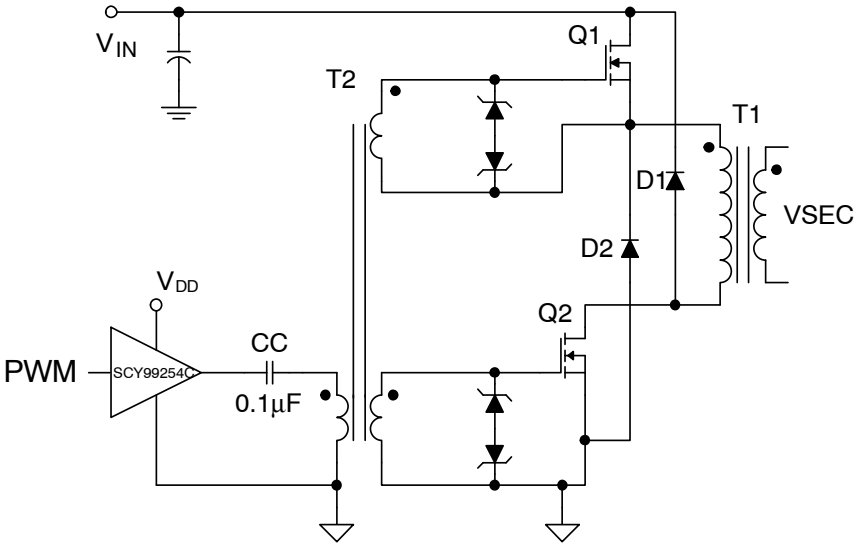
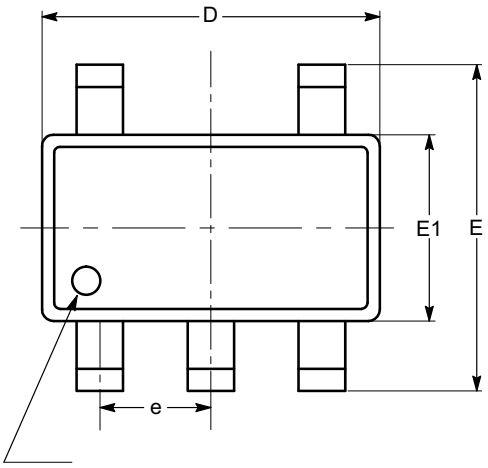


Figure 33. Driver for Two−Transistor, Forward−Converter Gate Transformer

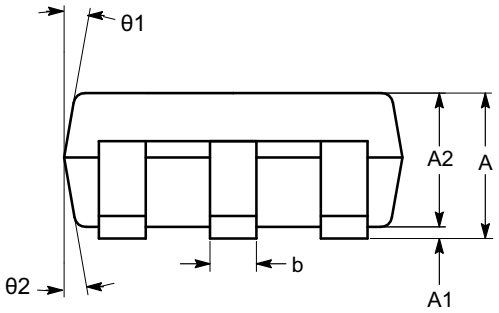
PACKAGE DIMENSIONS

SOT−23, 5 Lead
CASE 527AH−01
ISSUE O

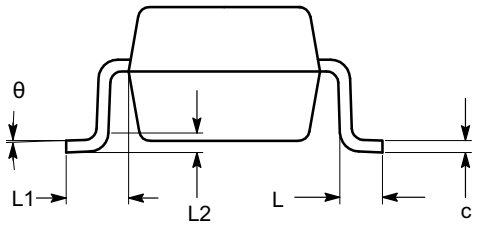


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.15	1.30
b	0.30		0.50
c	0.08		0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	5°	10°	15°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

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