

SN74LS166

8-Bit Shift Registers

The SN74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

GUARANTEED OPERATING RANGES

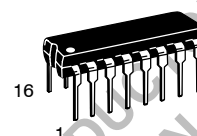
Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High			-0.4	mA
I _{OL}	Output Current – Low			8.0	mA



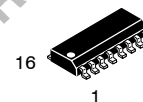
ON Semiconductor™

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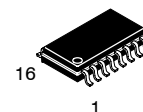
LOW
POWER
SCHOTTKY



PLASTIC
N SUFFIX
CASE 648



SOIC
D SUFFIX
CASE 751B



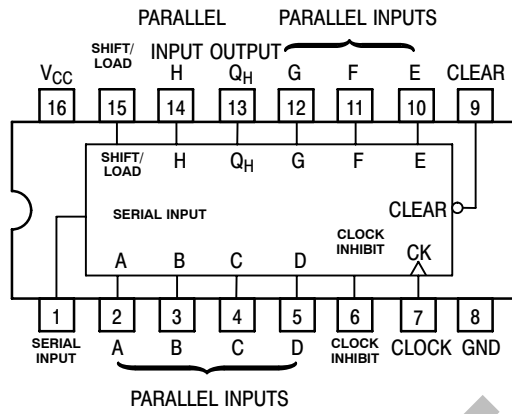
SOEIAJ
M SUFFIX
CASE 966

ORDERING INFORMATION

Device	Package	Shipping
SN74LS166N	16 Pin DIP	2000 Units/Box
SN74LS166D	SOIC-16	38 Units/Rail
SN74LS166DR2	SOIC-16	2500/Tape & Reel
SN74LS166M	SOEIAJ-16	See Note 1
SN74LS166MEL	SOEIAJ-16	See Note 1

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

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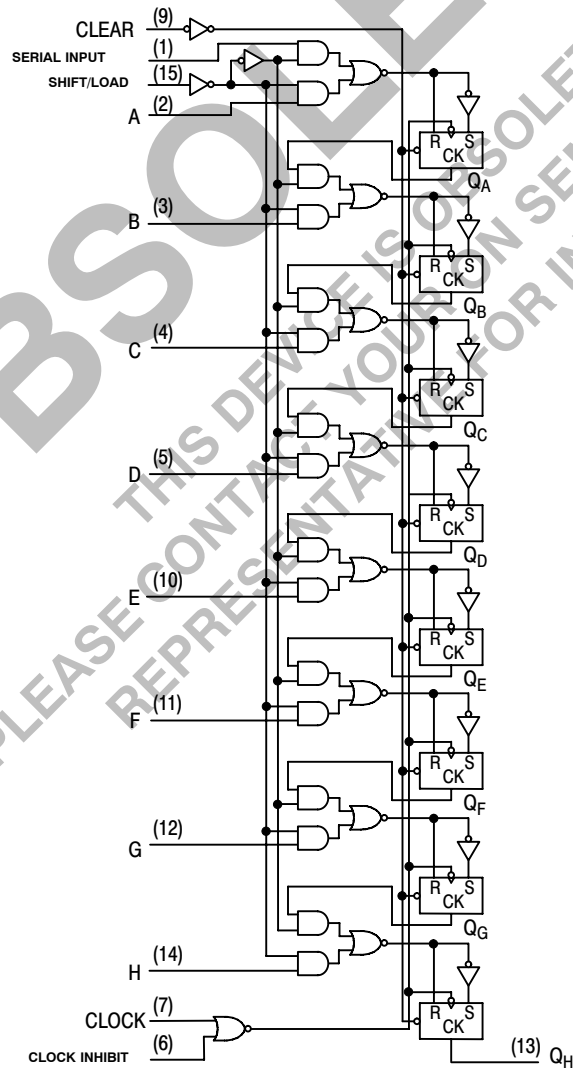
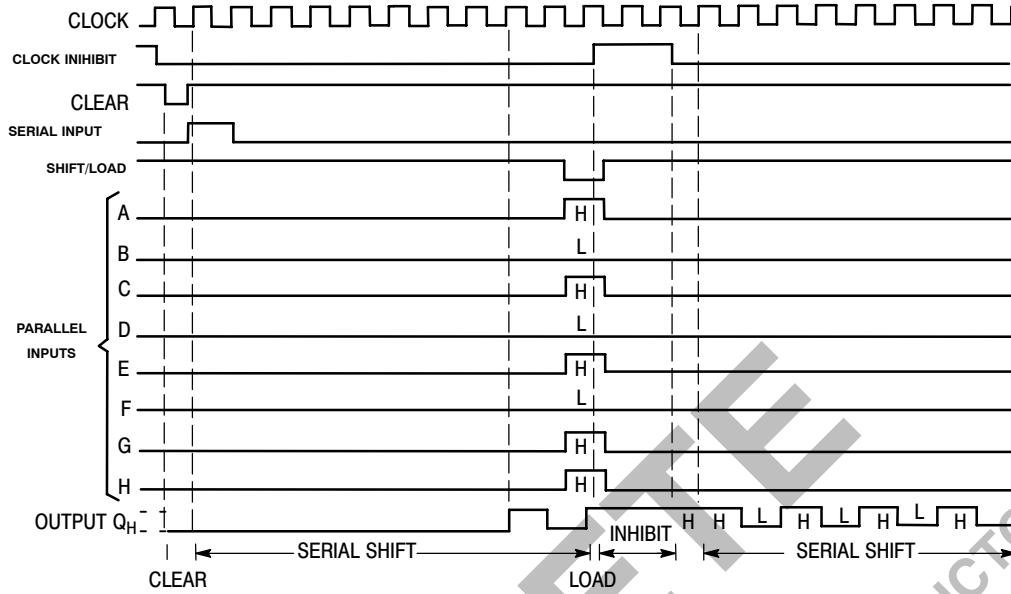


FUNCTION TABLE

INPUTS					PARALLEL A . . . H	INTERNAL OUTPUTS		OUTPUT QH
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL		QA	QB	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	↑	X	X	QA0	QB0	QH0

SN74LS166

Typical Clear, Shift, Load, Inhibit, and Shift Sequences



SN74LS166

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 2)	-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			38	mA	$V_{CC} = \text{MAX}$

2. Not more than one output should be shorted at a time, nor for more than 1 second.

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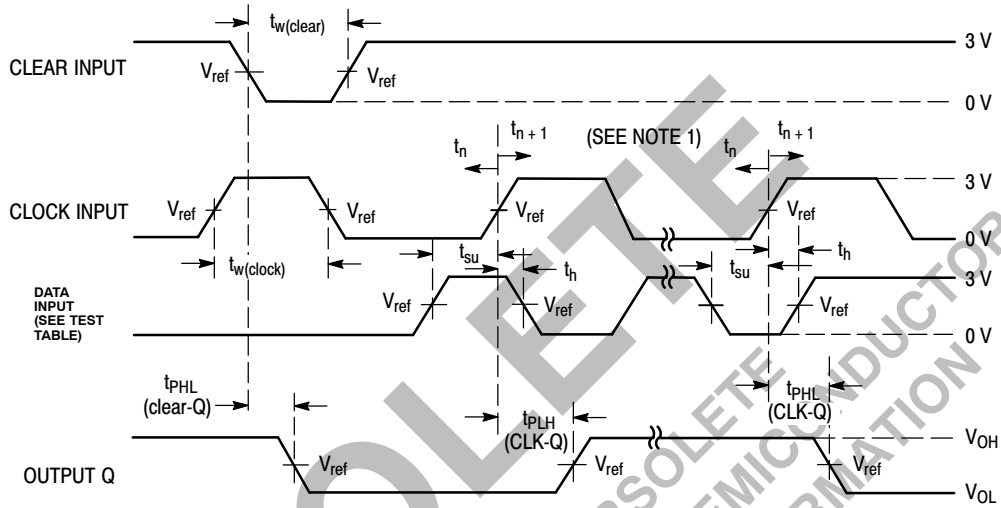
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TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}

AC WAVEFORMS



NOTE 1. t_n = bit time before clocking transition
 NOTE 2. t_{n+1} = bit time after one clocking transition
 t_{n+8} = bit time after eight clocking transition
 LS166 $V_{\text{ref}} = 1.3 \text{ V}$.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	35		MHz	$V_{\text{CC}} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PHL}	Clear to Output		19	30	ns	
t_{PLH} t_{PHL}	Clock to Output		23 24	35 35	ns	

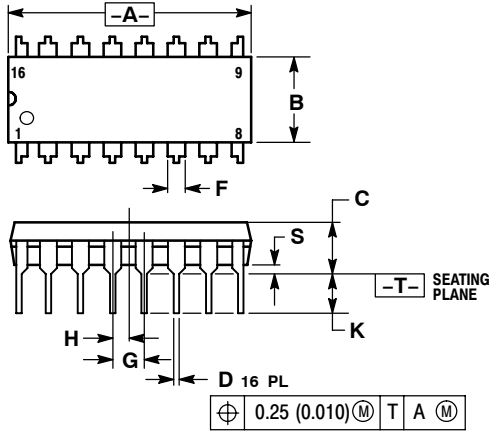
AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_w	Clock Clear Pulse Width	30			ns	$V_{\text{CC}} = 5.0 \text{ V}$
t_s	Mode Control Setup Time	30			ns	
t_s	Data Setup Time	20			ns	
t_h	Hold Time, Any Input	15			ns	

SN74LS166

PACKAGE DIMENSIONS

N SUFFIX
 PLASTIC PACKAGE
 CASE 648-08
 ISSUE R



\oplus	0.25 (0.010)	M	T	A	M
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

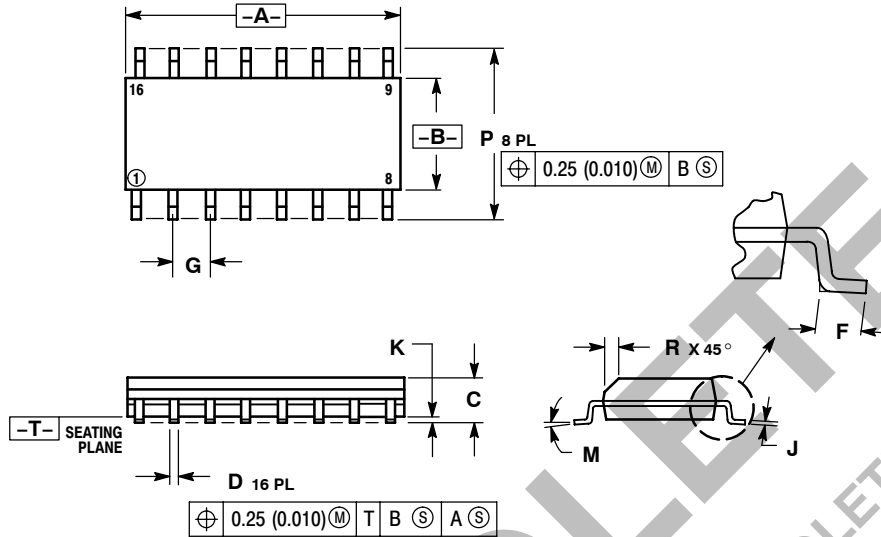
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PACKAGE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

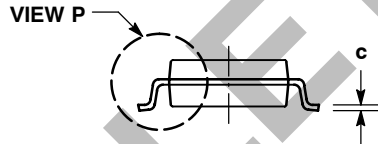
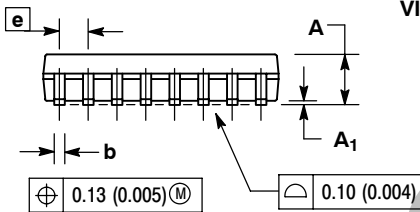
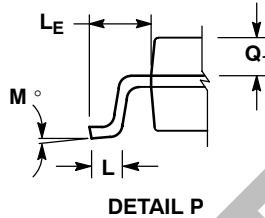
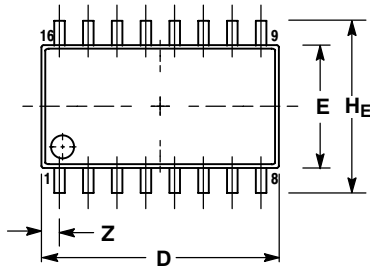
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SN74LS166

PACKAGE DIMENSIONS

M SUFFIX
SOEIAJ PACKAGE
CASE 966-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0° 10°		0° 10°	
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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