BCD to 7-Segment Decoder/Driver

The SN74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 μ A. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Open Collector Outputs
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effects

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Тур	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High BI/RBO			-50	μΑ
I _{OL}	Output Current – Low BI/RBO BI/RBO			3.2	mA
V _{O(off)}	Off-State Output Voltage a to g			15	V
I _{O(on)}	On–State Output Current a to g			24	mA



ON Semiconductor®

http://onsemi.com

LOW POWER SCHOTTKY

1 PLASTIC

N SUFFIX CASE 648

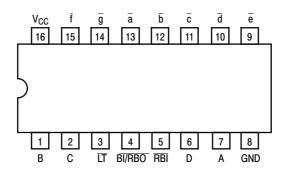


SOIC D SUFFIX CASE 751B

ORDERING INFORMATION

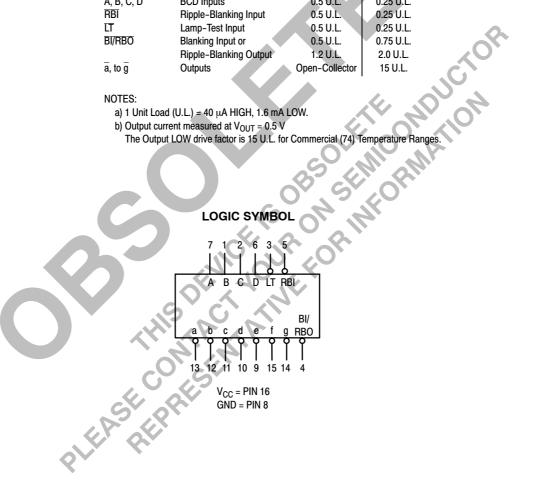
Device	Package	Shipping
SN74LS47N	16 Pin DIP	2000 Units/Box
SN74LS47D	16 Pin	2500/Tape & Reel

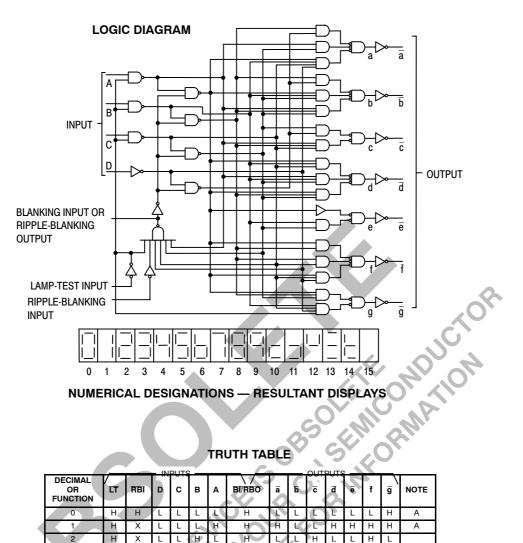
CONNECTION DIAGRAM DIP (TOP VIEW)



		LOADING	(Note a)	_
PIN NAMES		HIGH	LOW	
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.	
RBI	Ripple-Blanking Input	0.5 U.L.	0.25 U.L.	
LT	Lamp-Test Input	0.5 U.L.	0.25 U.L.	
BI/RBO	Blanking Input or	0.5 U.L.	0.75 U.L.	
	Ripple-Blanking Output	1.2 U.L.	2.0 U.L.	
a, to g	Outputs	Open-Collector	15 U.L.	
-			1	

NOTES:





				INI		· · · ·									_	
	DECIMAL OR FUNCTION	Г	RBĪ	D	c	в	A	\ ∕ BI/RBO	ia	đ	<u> </u>	đ	0	Ŧ	<u>a</u> /	NOTE
Ī	0	H	Н	Ľ	L	L	Ł	ЪН	L	L	L	L	L	L	Н	А
	1	Н	Х	L	L	L	Н	H	H	L	Ţ	Ή	Н	Н	Н	Α
	2	Н	Х	L	L	H	Ľ	Н	L	L	H	L	L	Н	L	
	3	Н	Х	L	Ļ	H	Н	H	L	L	L	L	Н	Н	L	
	4	Н	Х	L.	Н	L	L.	Н	Н	L	L	Н	Н	L	L	
	5	Н	X	L.	Н	L	H	H	Ľ	Н	L	L	Н	L	L	
	6	Н	X	Ľ	Н	H	►L _	Н	Н	Н	L	L	L	L	L	
	7	Н	X	L	Н	Ĥ	H	Ĥ	L	L	L	Н	Η	Н	Н	
	8	Н	Х	H	H	L	L	Н	L	L	L	L	L	L	L	
	9	Н	X	H	L	÷	Н	Н	L	L	L	Н	Н	L	L	
	10	Н	X)н	Ľ	H	L	Н	Н	Н	Н	L	L	Н	L	
	11	H	X	Н	L	Н	Н	Н	Н	Н	L	L	Η	Н	L	
	12	H	Х	Η	H	L	L	Н	Н	L	Н	Н	Н	L	L	
	13	Н	X	Н	Н	L	Н	Н	L	Н	Н	L	Н	L	L	
	14	Н	X	Н	Н	Н	L	Н	Н	Н	Н	L	L	L	L	
	15	H)	X	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	
	BI	Х	Х	Х	Х	Х	Х	L	Н	Н	Н	Н	Н	Н	Н	В
	RBI	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	С
	LT	L	Х	Х	Х	Х	Х	Н	L	L	L	L	L	L	L	D

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

NOTES:

(A) BI/RBO is wire-AND logic serving as blanking Input (BI) and/or ripple-blanking output (RBO). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input (RBI) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output (BI/RBO) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

			Limits					
Symbol	Parameter	Min	Тур	Max	Unit	Test	Conditions	
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input for All Inputs	HIGH Theshold Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Threshold Voltag		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -$	-18 mA	
V _{OH}	Output HIGH Voltage, BI/RBO	2.4	4.2		V	$V_{CC} = MIN, I_{OH} = V_{IN} = V_{IN} \text{ or } V_{IL} p$		
V.	Output LOW Voltage		0.25	0.4	V		$V_{CC} = MIN, V_{IN} = V_{IN}$	
V _{OL}	BI/RBO		0.35	0.5	V	I _{OL} = 3.2 mA	or V _{IL} per Truth Table	
I _{O (off)}	Off-State Output Current \overline{a} thru \overline{g}			250	μA	V _{CC} = MAX, V _{IN} = Table, V _{O (off)} = 1	₌ V _{IN} or V _{IL} per Truth 5 V	
Maria	On-State Output Voltage		0.25	0.4	V	I _{O (on)} = 12 mA	V_{CC} = MAX, V_{IN} = V_{IH}	
V _{O (on)}	\overline{a} thru \overline{g}		0.35	0.5	>	I _{O (on)} = 24 mA	or V _{IL} per Truth Table	
lu.	Input HIGH Current			20	μΑ	$V_{CC} = MAX, V_{IN} =$	= 2.7 V	
I _{IH}				0.1	mA	$V_{CC} = MAX, V_{IN} =$	= 7.0 V	
IIL	Input LOW Current BI/RBO Any Input except BI/RBO			-1.2 -0.4	mA	V _{CC} = MAX, V _{IN} =	= 0.4 V	
I _{OS} BI/RBO	Output Short Circuit Current (Note 1)	-0.3		-2.0	mA	V _{CC} = MAX, V _{OU}	Γ = 0 V	
I _{CC}	Power Supply Current		7.0	13	mA	V _{CC} = MAX	<u>`O`</u>	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^{\circ}C$)

			Limits	0		
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
t _{PHL} t _{PLH}	Propagation Delay, Address Input to Segment Output			100 100	ns ns	V _{CC} = 5.0 V
t _{PHL} t _{PLH}	Propagation Delay, RBI Input To Segment Output		C ^V	100 100	ns ns	C _L = 15 pF

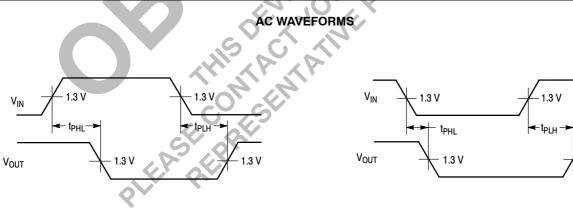
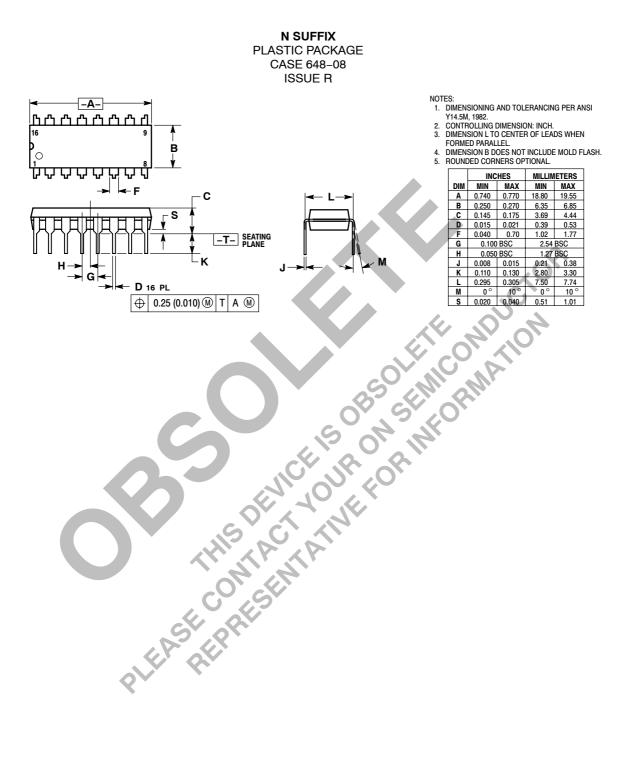


Figure 1.

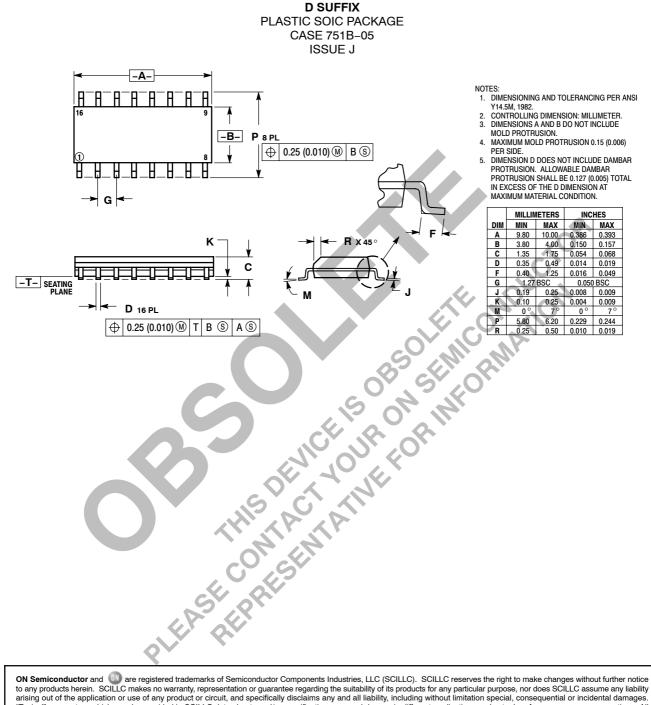
Figure 2.

1.3 V

PACKAGE DIMENSIONS



PACKAGE DIMENSIONS



ON Semiconductor and use registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death agsociated with such unintended or unauthorized use payers that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunit//Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81–3–5773–3850 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative