STK5DFU350D-E

Advance Information

2-in-1 PFC and Inverter Intelligent Power Module (IPM), 600 V, 8 A

The STK5DFU350D-E is a fully-integrated PFC and inverter power stage consisting of a high-voltage driver, six motor drive IGBT's, one PFC IGBT, one PFC rectifier and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3-phase bridge with an integrated single shunt which is connected to an internal over-current protection comparator. A second comparator is used for detecting faults in the combined PFC and inverter circuit.
The intelligent power module has a full range of protection functions including cross-conduction protection, external shutdown and under-voltage lockout functions.

Features

- Simple thermal design with PFC and inverter stage in one package.
- PFC operating frequency up to 40 kHz
- Cross-conduction protection
- Internal inverter shunt for compact design
- PFC and inverter fault detection with negative reference voltage
- Integrated bootstrap diodes and resistors
- Multiplexed fault and thermistor pin (FAULT/TH)

Typical Applications

- Industrial Pumps
- Industrial Fans
- Industrial Automation
- Home Appliances

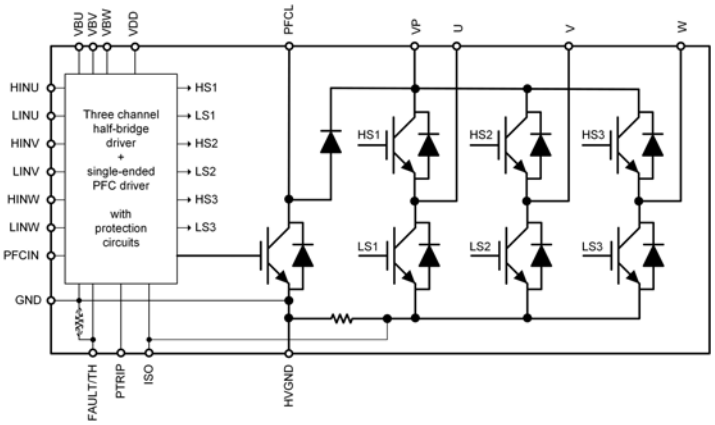

Figure 1. Functional Diagram

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PACKAGE PICTURE

32-pin DIP05 with exposed pad

MARKING DIAGRAM

TBD

STK5DFU350D = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot Code
Device marking is on package underside

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5DFU350D-E	DIP32 44 x 26.5 (Pb-Free)	11 / Tube

This document contains information on a new product. Specifications and information herein are subject to change without notice.

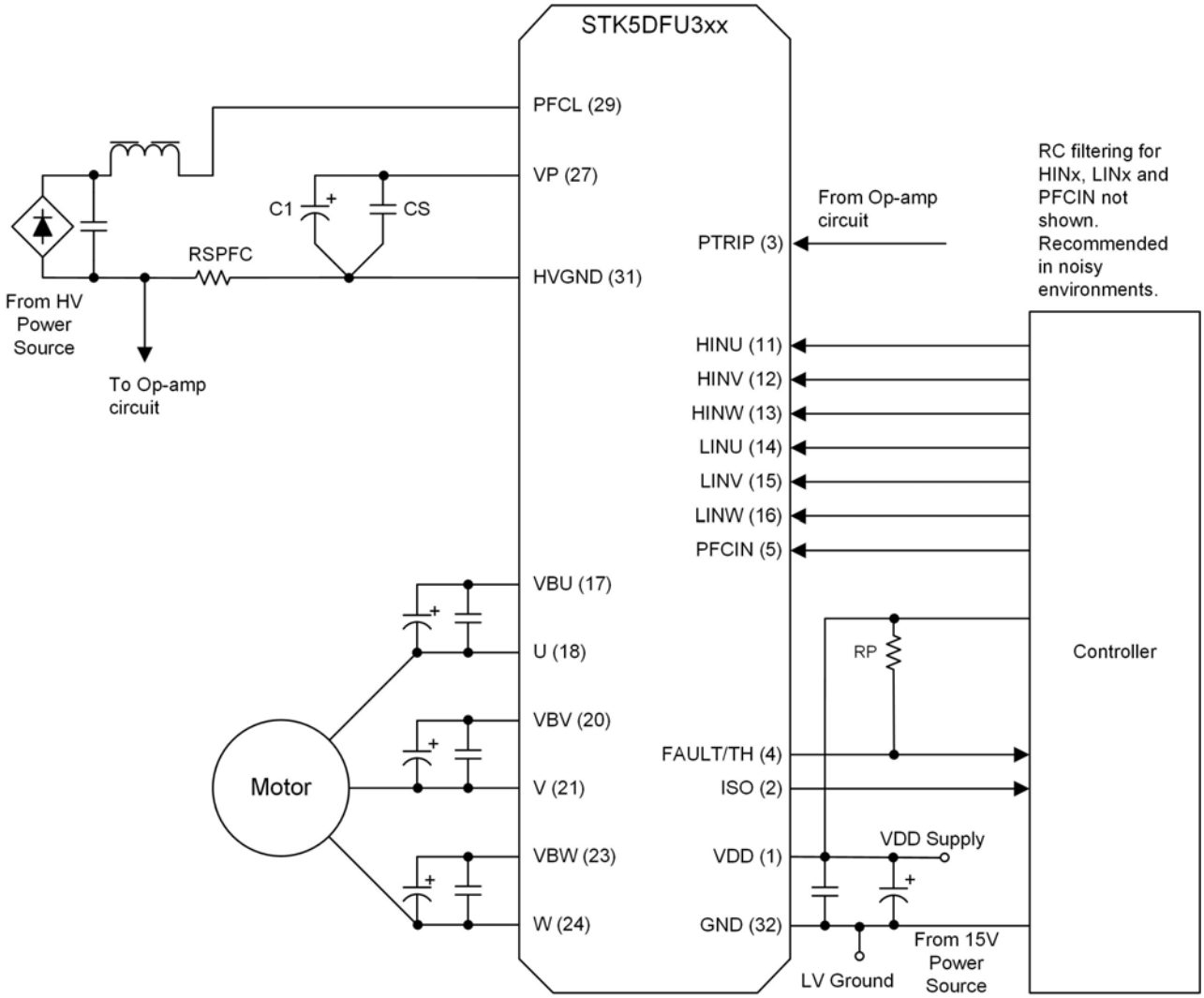


Figure 2. Application Schematic

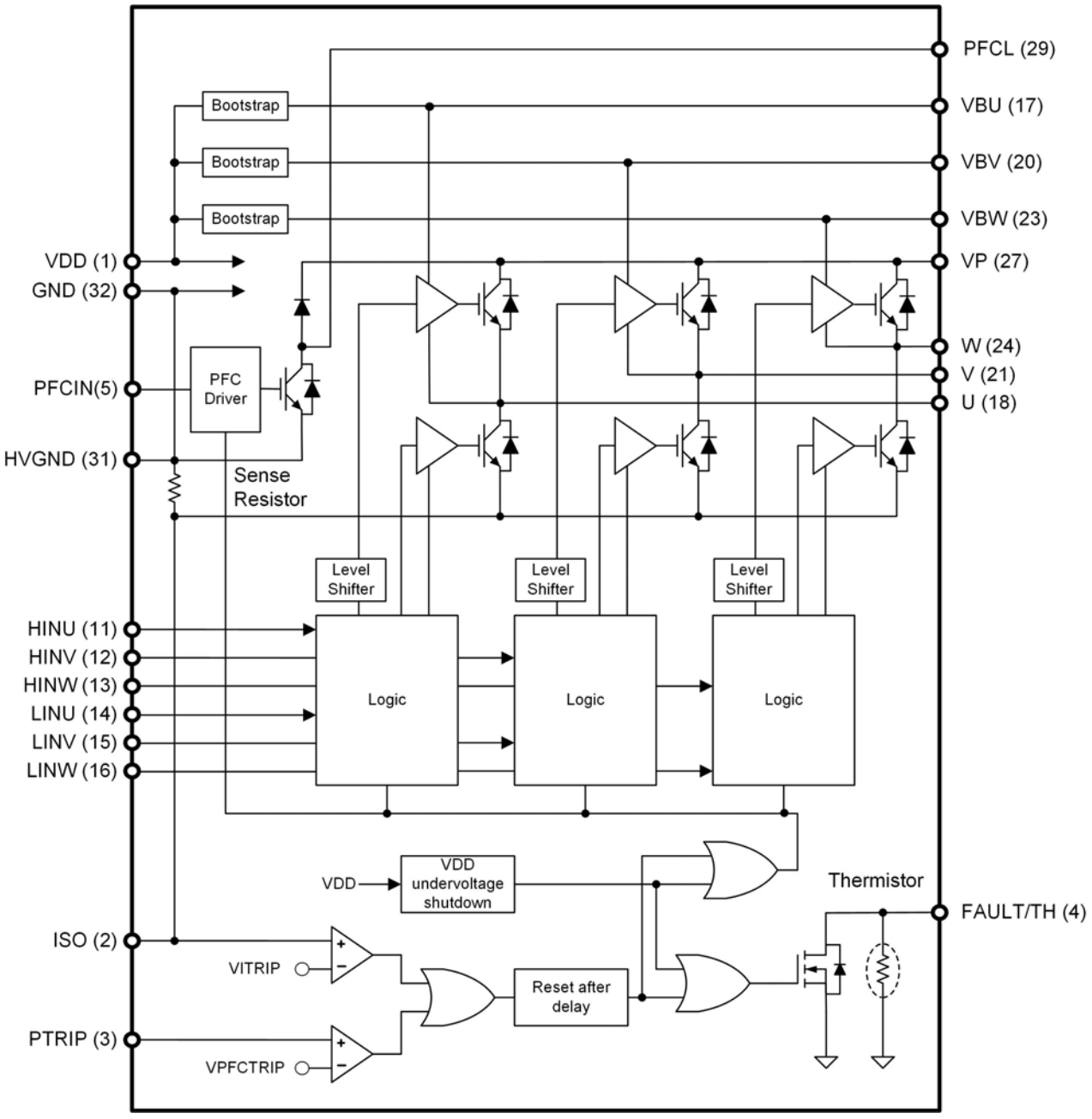


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	VDD	+15 V Main Supply
2	ITRIP	Current protection for inverter, connected to internal shunt
3	PTRIP	Current protection for PFC
4	FAULT/TH	Fault pin connected to thermistor
5	PFCIN	Logic Input PFC Gate Driver
11	HINU	Logic Input High Side Gate Driver - Phase U
12	HINV	Logic Input High Side Gate Driver - Phase V
13	HINW	Logic Input High Side Gate Driver - Phase W
14	LINU	Logic Input Low Side Gate Driver - Phase U
15	LINV	Logic Input Low Side Gate Driver - Phase V
16	LINW	Logic Input Low Side Gate Driver - Phase W
17	VBU	High Side Floating Supply voltage for U phase
18	U	U phase output. Internally connected to U phase high side driver ground
20	VBV	High Side Floating Supply voltage for V phase
21	V	V phase output. Internally connected to V phase high side driver ground
23	VBW	High Side Floating Supply Voltage for W phase
24	W	W phase output. Internally connected to W phase high side driver ground
27	VP	Positive PFC Output Voltage
29	PFCL	PFC Inductor Connection to IGBT and Rectifier node
31	HVGND	Negative PFC Output Voltage
32	GND	Negative Main Supply

Note : Pins 6, 7, 8, 9, 10, 19, 22, 25, 26, 28, 30 are not present

ABSOLUTE MAXIMUM RATINGS at Tc = 25°C (Notes 1, 2)

Rating		Symbol	Conditions	Value	Unit
PFC Section					
PFC IGBT	Collector-emitter voltage	V_{CE}	PFCL to HVGND	600	V
	Repetitive peak collector current	ICP	Duty cycle 10%, pulse width 100 μs	24	A
	Collector current	IC		11.3	A
	Power dissipation	PC		39.1	W
PFC Diode	Diode reverse voltage	VRM	VP to PFCL	600	V
	Repetitive peak forward current	IFP1	Duty cycle 10%, pulse width 100 μs	24	A
	Diode forward current	IF1		11.3	A
	Power dissipation	PD1		27.2	W
Maximum AC input voltage		VAC	Single-phase Full-rectified	264	V
Maximum output voltage		Vo	In the Application Circuit (Vac = 200 V, Vout = 380 V, fc = 40 kHz)	424	V
Maximum output power		Wo		1.8	kW
Input AC current (steady state)		Iin		9.5	Arms
Inverter Section					
Supply voltage		VP	VP to HVGND surge < 500 V (Note 3)	450	V
Collector-emitter voltage		V_{CE}	VP to U, V, W or U, V, W to HVGND	600	V
Output current		Io	VP, HVGND, U, V, W terminal current	±8	A
			VP, HVGND, U, V, W terminal current at Tc = 100°C	±3.7	A
Output peak current		Iop	VP, HVGND, U, V, W terminal current for a Pulse width of 1 ms	±16	A
Maximum power dissipation		Pd	IGBT per 1 channel	16.0	W
Gate driver section					
Gate driver supply voltage		VD1,2,3,4	VBU to U, VBV to V, VBW to W, V_{DD} to GND (Note 4)	−0.3 to 20	V
Input signal voltage		VIN	HINx, LINx, PFCIN (x = U, V, W)	−0.3 to V_{DD}	V
FAULT terminal voltage		VFAULT	FAULT terminal	−0.3 to V_{DD}	V
PFCTRIP terminal voltage		VPTRIP	PTRIP terminal	−1.5 to 2.0	V
Intelligent Power Module					
Junction temperature		Tj	IGBT, FRD	150	°C
Storage temperature		Tstg		−40 to +125	°C
Operating Case temperature		Tc	IPM case temperature	−20 to +100	°C
Tightening torque		MT	Case mounting screws	0.9	Nm
Isolation voltage		Vis	50 Hz sine wave AC 1 minute (Note 5)	2000	VRMS

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This surge voltage developed by the switching operation due to the wiring inductance between VP and HVGND terminals.
4. VBS = VBU to U, VBV to V, VBW to W
5. Test conditions : AC 2500 V, 1 s

RECOMMENDED OPERATING RANGES (Note 6)

Rating	Symbol		Min	Typ	Max	Unit
Supply voltage	V_{CC}	VP to HVGND	0		450	V
Gate driver supply voltage	V_{BS}	VBU to U, VBV to V, VBW to W	12.5	15	17.5	V
	V_{DD}	V_{DD} to GND (Note 6)	13.5	15	16.5	
ON-state input voltage	VIN(ON)	HINU, HINV, HINW, LINU, LINV, LINW,PFCIN	3.0		5.0	V
OFF-state input voltage	VIN(OFF)		0		0.3	
PWM frequency	fPWM		1		20	kHz
Dead time	DT	Turn-off to turn-on (external)	1.5			μs
Allowable input pulse width	PWIN	ON and OFF	1			μs
Package mounting torque		'M3' type screw	0.6		0.9	Nm

6. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS at Tc = 25°C, VD1, VD2, VD3, VD4=15V (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PFC Section						
Collector-emitter cut-off current	V_{CE} = 600 V	I_{CE}	-	-	100	μA
Reverse leakage current (PFC Diode)	VR = 600 V	IR	-	-	100	μA
Collector-emitter saturation voltage	Ic = 12 A, Tj = 25°C	V_{CE}(sat)	-	1.8	2.2	V
	Ic = 6 A, Tj = 100°C		-	1.5	-	
Diode forward voltage (PFC Diode)	IF = 12 A, Tj = 25°C	VF1	-	2.5	3.0	V
	IF = 6 A, Tj = 100°C		-	1.9	-	
Junction to case thermal resistance	IGBT(Q1)	θj-c(T)	-	-	3.2	°C/W
	FRD1(D1)	θj-c(D)	-	-	4.6	
Switching characteristics						
Switching time	Ic = 12 A, VP = 300 V, Tj = 25°C	tON	-	0.5	-	μs
		tOFF	-	1.1	-	μs
Diode reverse recovery time		trr	-	180	-	ns
Inverter section						
Collector-emitter leakage current	V_{CE} = 600 V	I_{CE}	-	-	100	μA
Bootstrap diode reverse current	VR(BD) = 600 V	IR(BD)	-	-	100	μA
Collector to emitter saturation voltage	Ic = 8 A, Tj = 25°C	V_{CE}(sat)	-	2.1	2.6	V
	Ic = 4 A, Tj = 100°C		-	1.8	-	V
Diode forward voltage	IF = 8 A, Tj = 25°C	VF	-	2.0	2.5	V
	IF = 4 A, Tj = 100°C		-	1.6	-	V
Junction to case thermal resistance	IGBT	θj-c(T)	-	-	7.8	°C/W
Switching time	Ic = 8 A, VP = 300 V, Tj = 25°C	t_{ON}	-	0.7	-	μs
		t_{OFF}	-	0.9	-	μs
Turn-on switching loss	Ic = 8 A, V_{CC} = 300 V, Tj = 25°C	E_{ON}	-	770	-	μJ
Turn-off switching loss		E_{OFF}	-	200	-	μJ
Total switching loss		E_{TOT}	-	970	-	μJ
Turn-on switching loss	Ic = 4 A, V_{CC} = 300 V, Tj = 100°C	E_{ON}	-	350	-	μJ
Turn-off switching loss		E_{OFF}	-	110	-	μJ
Total switching loss		E_{TOT}	-	460	-	μJ
Diode reverse recovery energy	Ic = 8 A, V_{CC} = 300 V, Tj = 25°C (di/dt set by internal driver)	E_{REC}	-	130	-	μJ
Diode reverse recovery time		trr	-	180	-	ns
Reverse bias safe operating area	Ic = 16 A, V_{CE} = 450 V	RBSOA	Full Square	-		
Short circuit safe operating area	V_{CE} = 400 V	SCSOA	4	-	-	μs

7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS at Tc = 25°C, V_{BS} = 15 V, V_{DD} = 15 V (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Driver Section						
Gate driver consumption current	V_{BS} = 15 V (Note 4), per driver	ID	-	0.08	0.4	mA
	V_{DD} = 15 V, total	ID	-	0.85	2.4	mA
High level Input voltage	HINU, HINV, HINW, LINU, LINV, LINW to GND	Vin H	2.5	-	-	V
Low level Input voltage		Vin L	-	-	0.8	V
Logic 1 input current	VIN = +3.3 V	I_{IN+}	-	100	143	μA
Logic 0 input current	VIN = 0 V	I_{IN-}	-	-	2	μA
Bootstrap diode forward voltage	IF = 0.1 A	VF(DB)	-	0.8	-	V
Bootstrap circuit resistance		RBC	-	2	-	Ω
FAULT/TH terminal sink current	FAULT : ON / VFAULT = 0.1 V	IoSD	-	2	-	mA
FAULT clearance delay time		FLTCLR	1	2	3	ms
Over current protection for inverter stage	VN to HVGND current	OCP	8.7	9.8	10.9	A
ISO terminal Output voltage	Io = 8 A, ISO to GND voltage	VISO	0.38	0.40	0.42	V
PTRIP threshold voltage	PTRIP to GND	VPTRIP	−0.37		−0.26	V
PTRIP to shutdown propagation delay		t_{PTRIP}	(790)	(900)	(1150)	ns
PTRIP blanking time		$t_{PTRIPBL}$	290	350	-	ns
V_{DD} and V_{BS} supply undervoltage positive going input threshold		V_{DDUV+} V_{BSUV+}	10.5	11.1	11.7	V
V_{DD} and V_{BS} supply undervoltage negative going input threshold		V_{DDUV-} V_{BSUV-}	10.3	10.9	11.5	V
V_{DD} and V_{BS} supply undervoltage $I_{lockout}$ hysteresis		V_{DDUVH} V_{BSUVH}	-	0.2	-	V

8. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS PFC SECTION

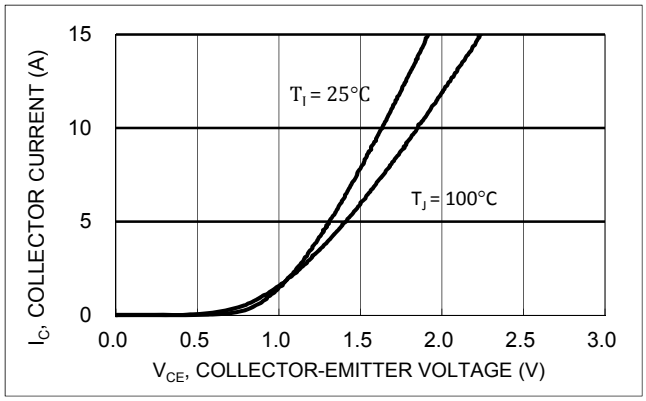


Figure 4 V_{CE} versus ID for different temperatures (V_{DD} = 15 V)

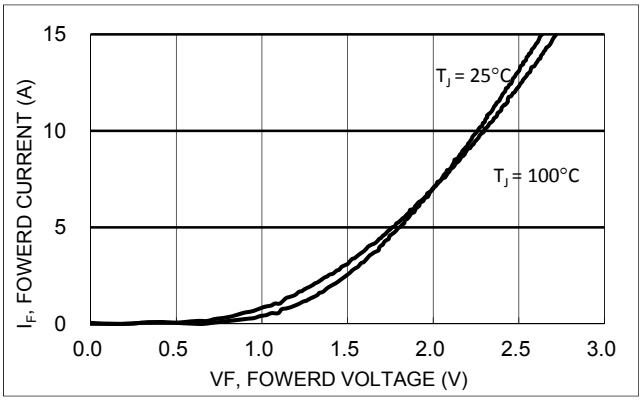


Figure 5 PFC Diode VF versus IF for different temperatures

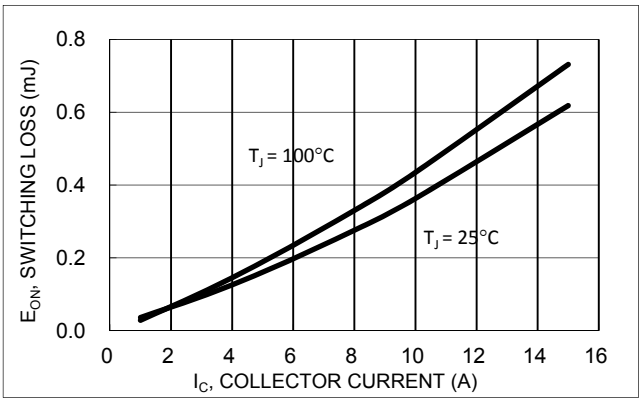


Figure 6 IGBT EON versus ID for different temperatures

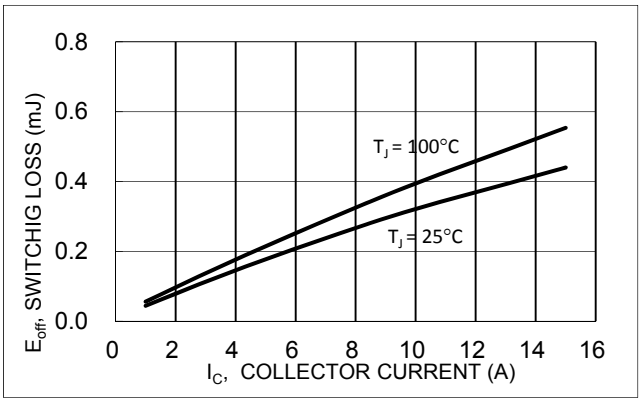


Figure 4 IGBT EOFF versus ID for different temperatures

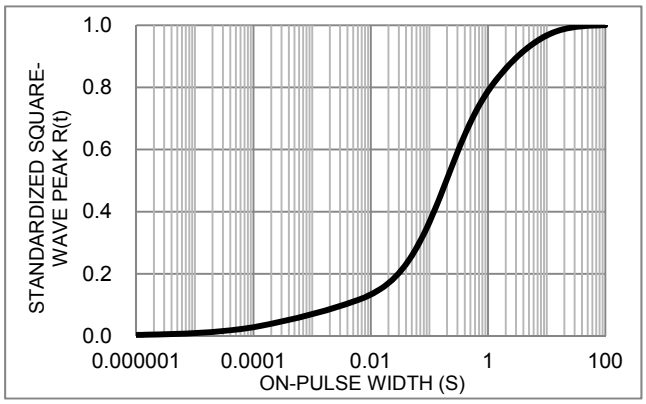


Figure 8 Thermal Impedance Plot

TYPICAL CHARACTERISTICS INVERTER SECTION

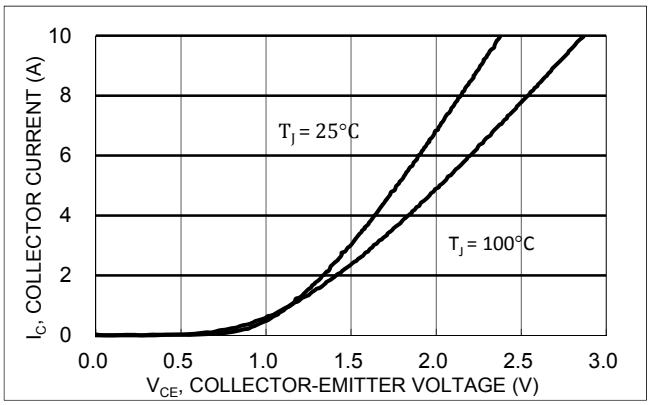


Figure 9 V_{CE} versus ID for different temperatures (V_{DD} = 15 V)

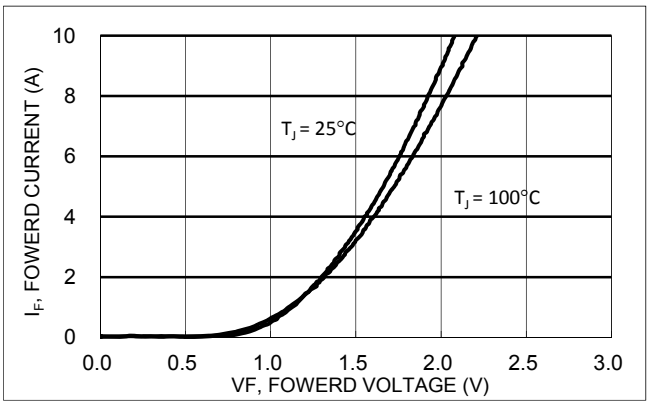


Figure 10 VF versus ID for different temperatures

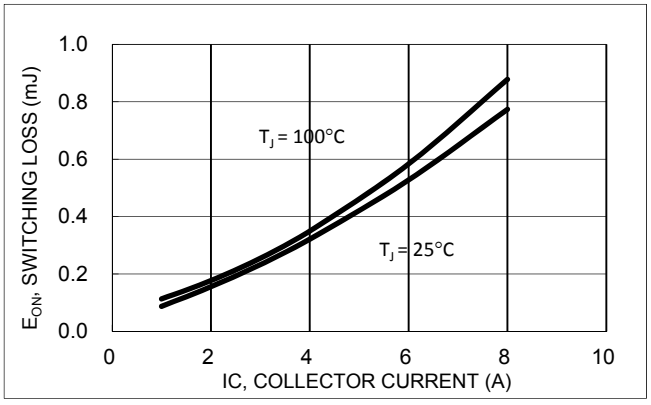


Figure 11 EON versus ID for different temperatures

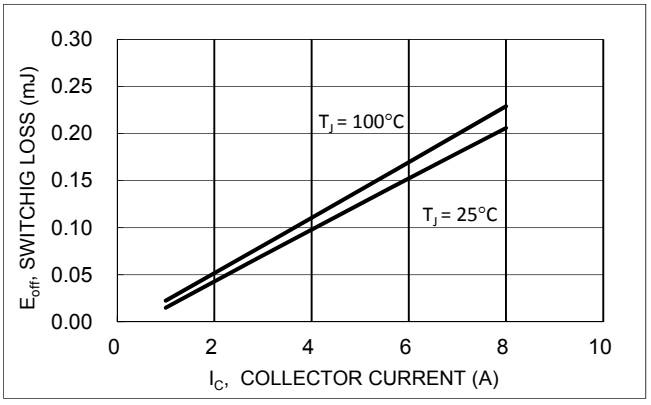


Figure 12 EOFF versus ID for different temperatures

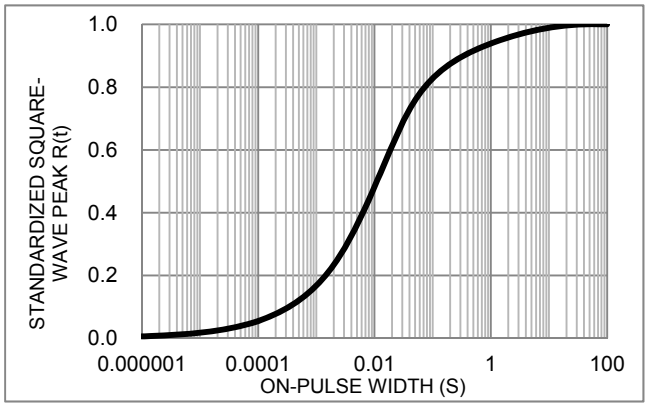


Figure 13 Thermal Impedance Plot

APPLICATIONS INFORMATION

Input / Output Timing Chart

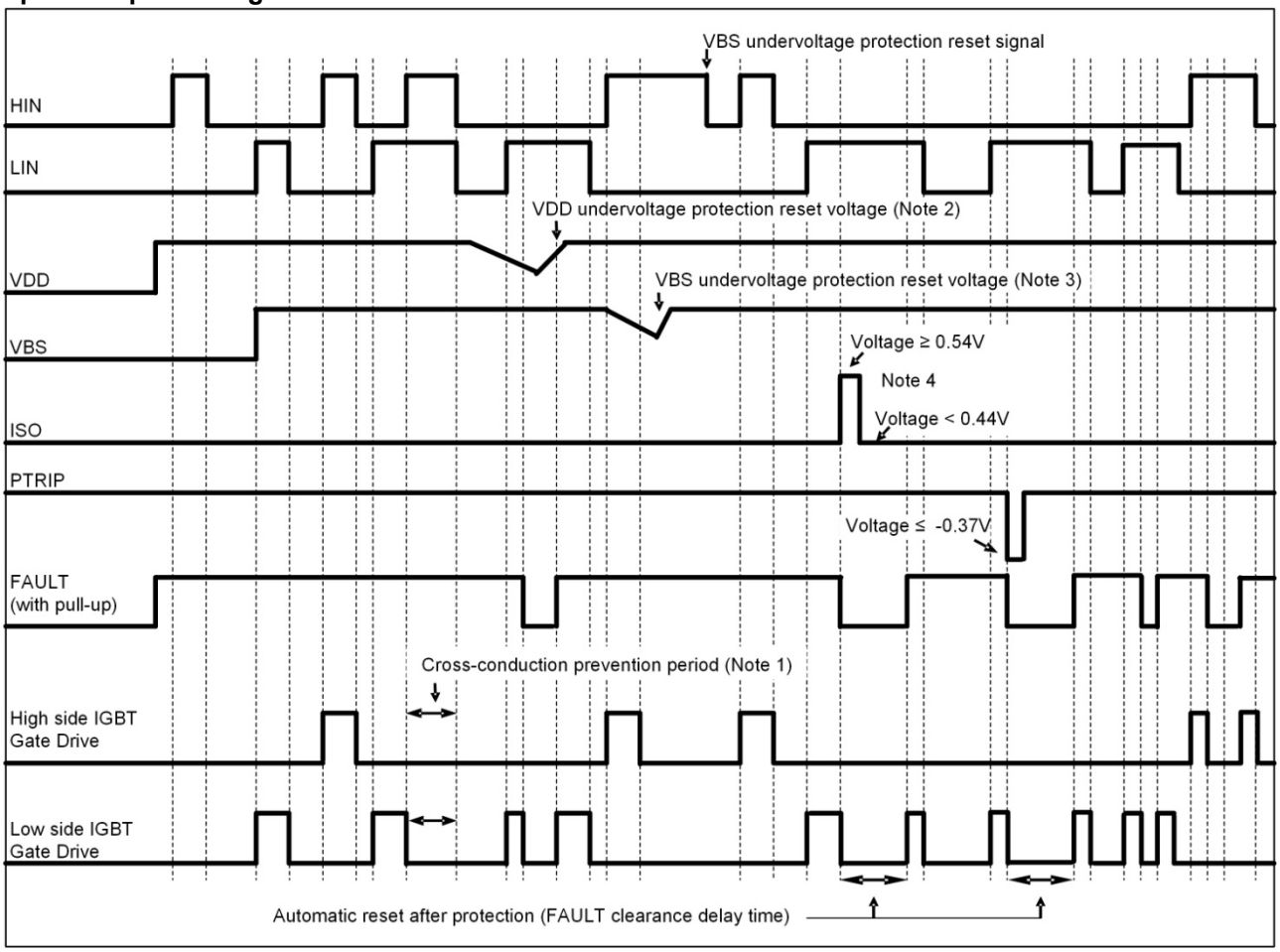


Figure 14. Input/Output Timing Chart

Notes

1. This section of the timing diagram shows the effect of cross-conduction prevention.
2. This section of the timing diagram shows that when the voltage on V_{DD} decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on V_{DD} rises sufficiently, normal operation will resume.
3. This section shows that when the bootstrap voltage V_{BS} drops, the corresponding high side output (U or V or W) is switched off. When V_{BS} rises sufficiently, normal operation will resume.
4. This section shows that when the voltage on ITRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed.

Input / Output Logic Table

INPUT				OUTPUT			
HIN	**LIN**	**Itrip**	**Enable**	**High side IGBT**	**Low side IGBT**	**U,V,W**	**FAULT**
H	L	L	H	ON (Note 5)	OFF	VP	OFF
L	H	L	H	OFF	ON	NU,NV,NW	OFF
L	L	L	H	OFF	OFF	High Impedance	OFF
H	H	L	H	OFF	OFF	High Impedance	OFF
X	X	H	H	OFF	OFF	High Impedance	ON
X	X	X	L	OFF	OFF	High Impedance	OFF

Thermistor characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	99	100	101	kΩ
	R_{100}	Tc = 100°C	5.18	5.38	5.60	kΩ
B-Constant (25 to 50°C)	B		4208	4250	4293	K
Temperature Range			−40		+125	°C

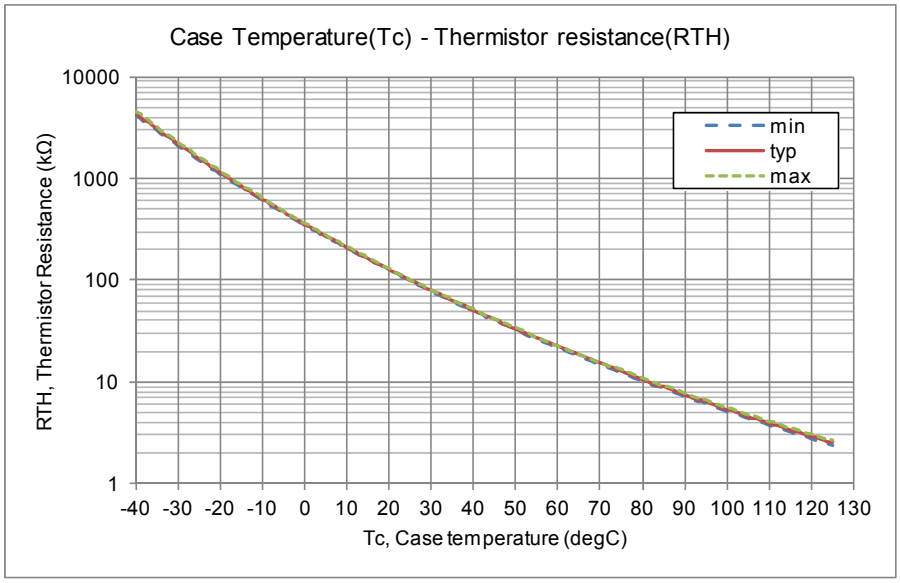


Figure 5 Thermistor Resistance versus Case Temperature

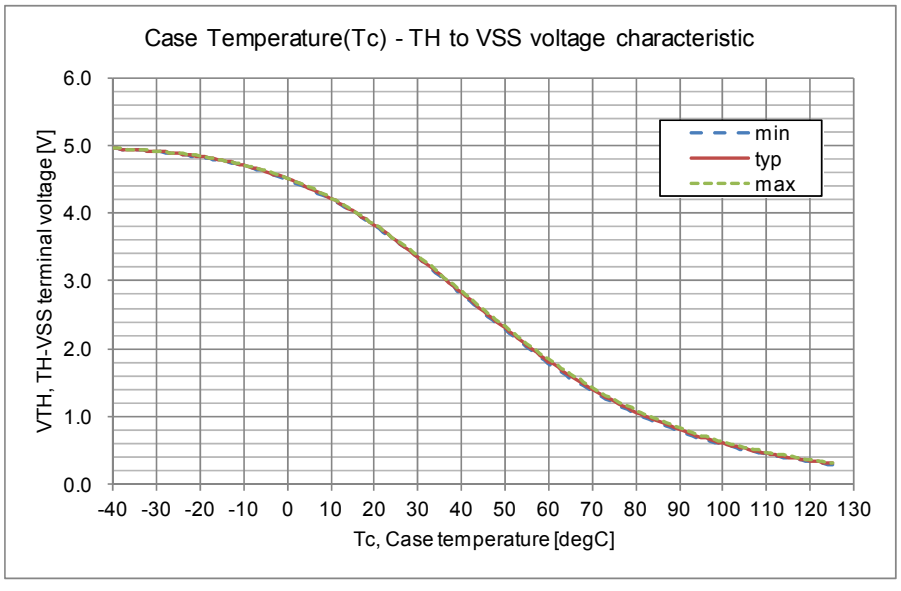


Figure 8 Thermistor Voltage versus Case Temperature
Conditions: RTH = 39 kΩ, pull-up voltage 5.0 V

(see

Figure 2)

Signal inputs
Each signal input has a pull-down resistor. An additional pull-down resistor of between 2.2 kΩ and 3.3 kΩ is recommended on each input to improve noise immunity

FAULT/TH pin
The FAULT/TH pin is connected to an open-drain FAULT output requiring a pull-up resistor. If the pull-up voltage is 5 V, use a pull-up resistor with a value of 6.8 kΩ or higher. If the pull-up voltage is 15 V, use a pull-up resistor with a value of 20 kΩ or higher. The pulled up voltage in normal operation for the FLTEN pin should be above 2.5 V. The FAULT output is triggered if there is a V_{CC} undervoltage or an overcurrent condition on either the PFC or inverter stages.
The terminal has a function of thermistor output, which is connected between GND and this terminal.

Overcurrent protection
An over-current condition is detected if the voltage on the PTRIP pin is larger than the reference voltage. There is a blanking time of typically 350 ns to improve noise immunity. After a shutdown propagation delay of typically 0.55 μs, the FAULT output is switched on.

The over-current protection threshold should be set to be equal or lower to the absolute maximum current.

An additional fuse is recommended to protect against system level or abnormal over-current fault conditions.

Capacitors on High Voltage and V_{DD} supplies
Both the high voltage and V_{DD} supplies require an electrolytic capacitor and an additional high frequency capacitor. The recommended value of the high frequency capacitor is between 100 nF and 10 μF.

Minimum input pulse width
When input pulse width is less than 1μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Input terminal Zener Diode
The inputs are protected with 10 V Zener diodes. If the input voltage exceeds 5 V, a current limiting resistor which limits the input current to less than 0.5 mA must be added to the input. This also helps with improving noise immunity.

Calculation of bootstrap capacitor value
The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS: Bootstrap power supply.
  15 V is recommended.
- QG: Total gate charge of IGBT at VBS = 15 V.
  42nC
- UVLO: Falling threshold for UVLO.
  Specified as 12 V.
- ID_{MAX}: High side drive consumption current.
  Specified as 95 μA
- t_{ONMAX}: Maximum ON pulse width of high side IGBT.

Capacitance calculation formula:

$$CB = (QG + I_{DMAX} * t_{ONMAX}) / (VBS - UVLO)$$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

The internal bootstrap circuit uses a MOSFET. The turn on time of this MOSFET is synchronized with the turn on of the low side IGBT. The bootstrap capacitor is charged by turning on the low side IGBT.

If the low side IGBT is held on for a long period of time (more than one second for example), the bootstrap voltage on the high side MOSFET will slowly discharge.

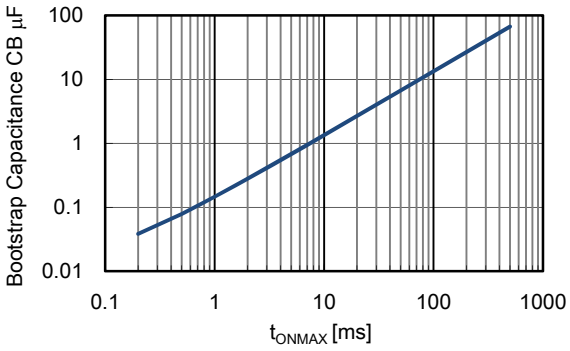


Figure 97: Bootstrap capacitance versus t_{ONMAX}

Mounting Instructions

Item	Recommended Condition
Pitch	41 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter : M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer dimensions (Figure 14) D = 7 mm, d = 3.2 mm and t = 0.5 mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : −50 to 50 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening : 50 to 60% of final tightening on first screw Temporary tightening : 50 to 60% of final tightening on second screw Final tightening : 0.4 to 0.6 Nm on first screw Final tightening : 0.4 to 0.6 Nm on second screw
Grease	Silicone grease. Thickness : 50 to 100 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.

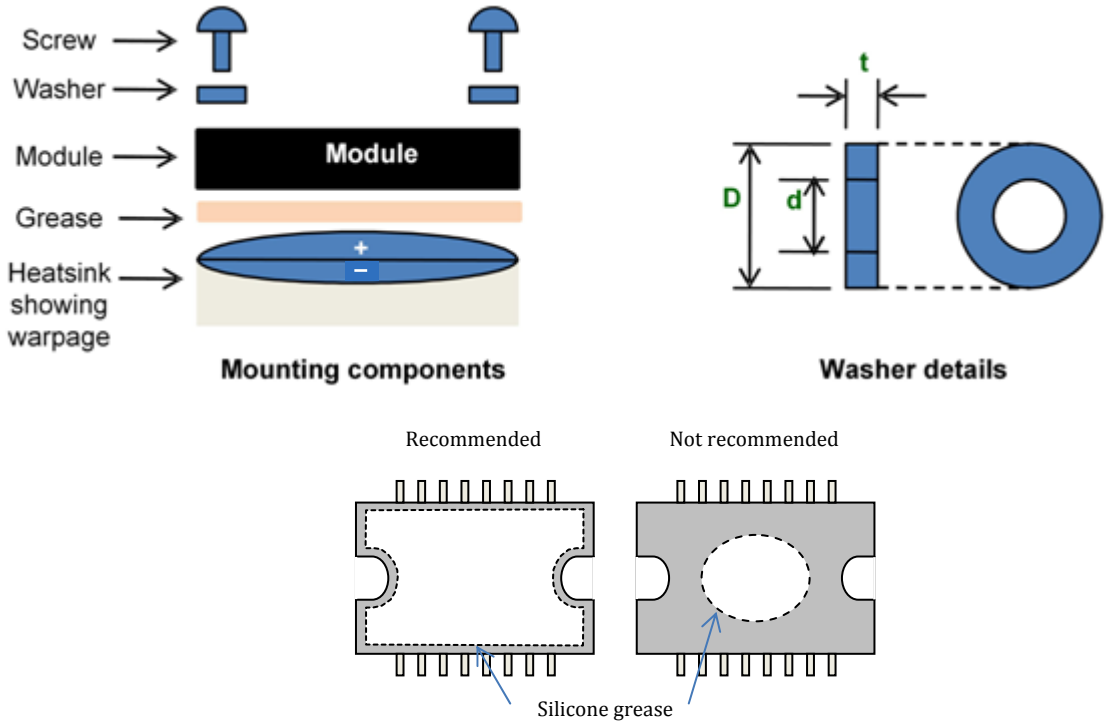
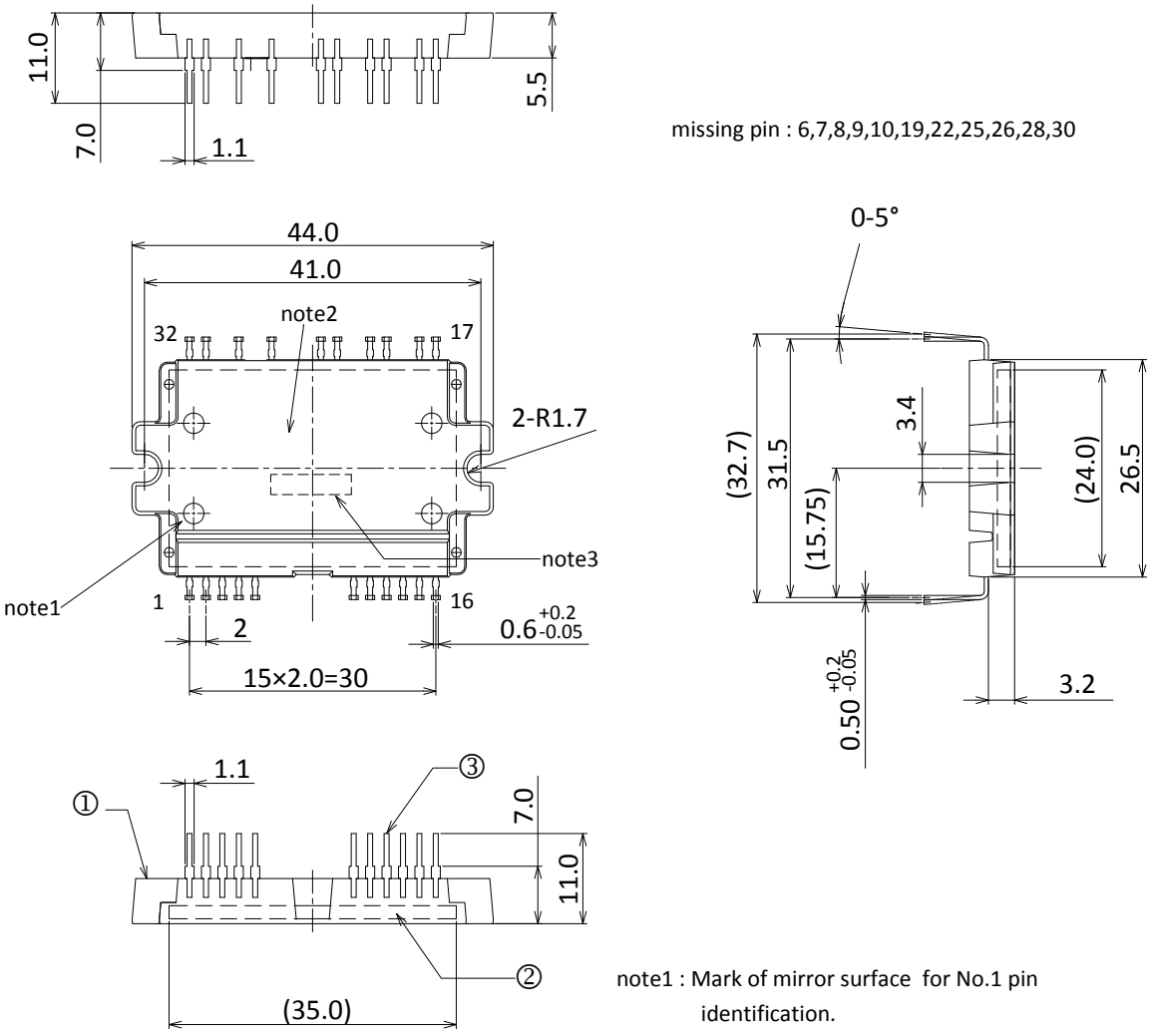


Figure 108: Module Mounting details: components; washer drawing; need for even spreading of thermal grease

Package Dimensions

unit : mm

The tolerances of length are +/− 0.5 mm
unless otherwise specified.



missing pin : 6,7,8,9,10,19,22,25,26,28,30

note1 : Mark of mirror surface for No.1 pin identification.

note2 : The form of a character in this drawing differs from that of IPM.

note3 : This indicates the lot code. The form of a character in this drawing differs from that of IPM.