REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Z. Correct the maximum iccsba value in table I. Update boilerplate in according with MIL-PRF-38535 requirement. - phn	13-02-11	Thomas M. Hess

REV																				
SHEET																				
REV	A	A	A																	
SHEET	15	16	17																	

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

Phu H. Nguyen

APPROVED BY

10-01-12

DRAWING APPROVAL DATE

Thomas M. Hess

REVISION LEVEL

A

MICROCIRCUIT, DIGITAL, ASIC, CMOS GATE ARRAY BASED ON SPACEWIRE REMOTE TERMINAL CONTROLLER, MONOLITHIC SILICON

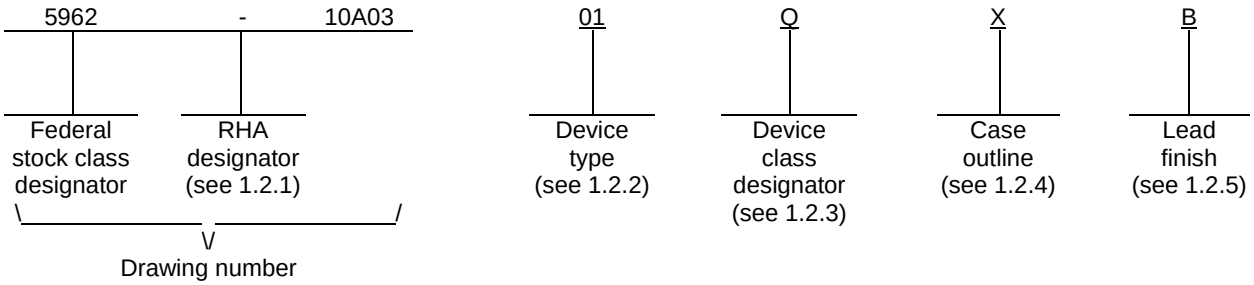
SIZE	CAGE CODE	
A	**67268**	**5962-10A03**

SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AT7913E	SpaceWire Remote Terminal Controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	349	Column Grid Array and interposer SCI
Y	See figure 1	349	Column Grid Array
Z	See figure 1	352	Quad flatpack with non conductive tie bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range for core (V_{CC1})	-0.3 V to 2.0 V dc
Supply voltage range for I/O's (V_{CC2})	-0.3V to 4.0 V dc
Power dissipation (Pd)	2 W
Storage temperature range	-65°C to 150°C
Maximum junction temperature (T_J)	175°C
Thermal resistance junction to case (Rjc):	
Case X	2°C/W
Case Y	1 °C/W
Case Z	2°C/W
Operating free-air temperature range (T_A)	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range for core (V_{CC1})	1.65 V to 1.95 V dc
Supply voltage range for I/O's (V_{CC2})	3.0 V to 3.6 V dc
Ambient operating temperature (T_A)	-55°C to 125°C
Storage temperature	30°C, 20 to 65% RH, dust free, original packing

1.5 Radiation features.

Maximum total dose available (dose rate = 0.1 rads(Si)/s) ..... 100 krads(Si)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage referenced to ground unless otherwise specified

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

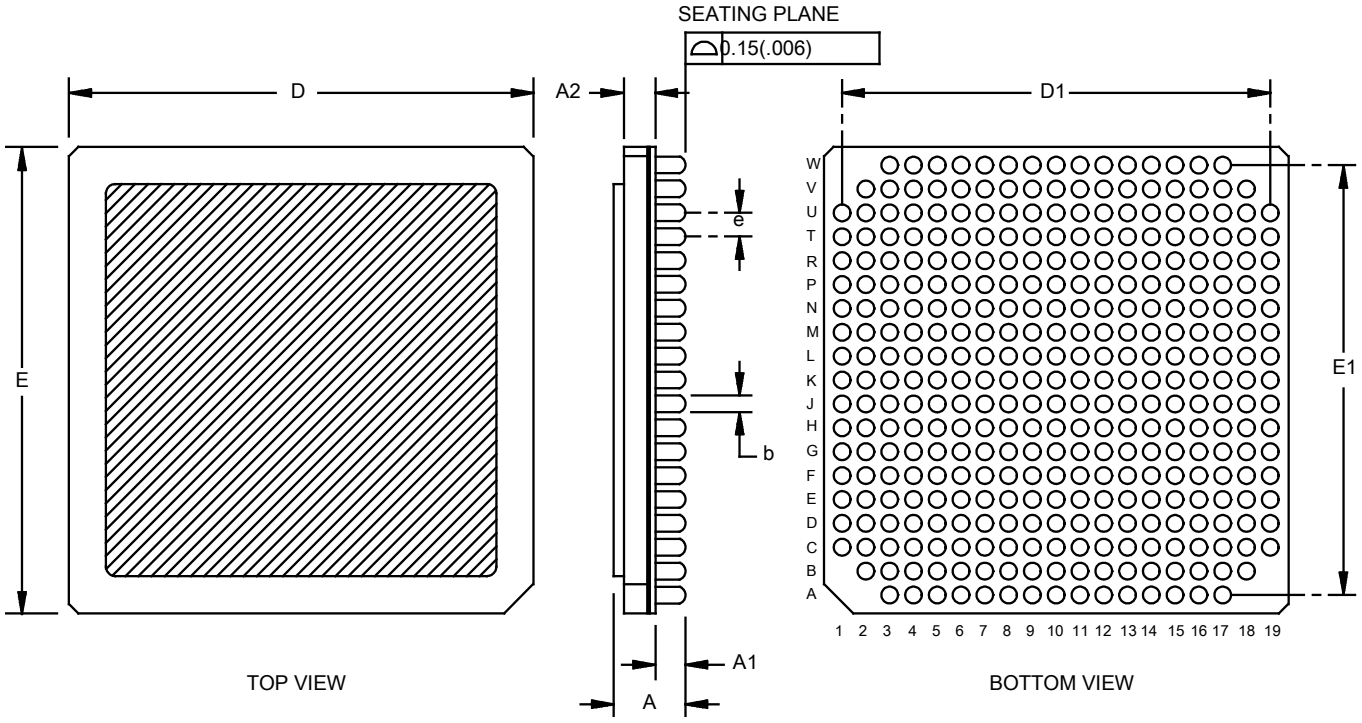
TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $1.65\ V \le V_{CC1} \le 1.95\ V$ $3.0\ V \le V_{CC2} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Low level input voltage	V_{IL}	CMOS	1,2,3		0.8	V
High level input voltage	V_{IH}	CMOS	1,2,3	2.0		V
Low level input current	I_{IL}	V_{IN} = GND, V_{CC2} = 3.3 V	1,2,3	-1		µA
Low level input current Pull-down	I_{ILPD}	V_{IN} = GND, V_{CC2} = 3.3 V	1,2,3	-5		µA
Low level input current Pull-up	I_{ILPU}	V_{IN} = GND, V_{CC2} = 3.3 V	1,2,3	-400		µA
High level input current	I_{IH}	$V_{IN} = V_{CC2}$ = 3.3 V	1,2,3		1	µA
High level input current Pull-up	I_{IHPU}	$V_{IN} = V_{CC2}$ = 3.3 V	1,2,3		5	µA
High level input current Pull-down	I_{IHPD}	$V_{IN} = V_{CC2}$ = 3.3 V	1,2,3		600	µA
Output leakage low current	I_{OZL}	Outputs disabled V_{OUT}=GND	1,2,3	-1		µA
Output leakage high current	I_{OZH}	Outputs disabled V_{OUT}=VCC2	1,2,3		1	µA
Low level output voltage	V_{OL}	V_{CC2} = 3.0 V I_{OL}= 2,4,8,12,16 mA	1,2,3		0.4	V
high level output voltage	V_{OH}	V_{CC2} = 3.0 V I_{OH} = -2,-4,-8,-12,-16 mA	1,2,3	V_{CC2}-0.4		V
Supply current for array when not clocked	I_{CCSBA}	V_{CC2} = 3.6 V V_{CC1} = 1.95 V	1,2,3		5.3	mA
Operating supply current for array	I_{CCOPA}	V_{CC2} = 3.6 V, V_{CC1} = 1.95 V	1,2,3		52	mA
Input/Output capacitance 1/	C_{IO}	V_{CC2} = 0 V	4		7	pF
Propagation delay, SysClk rising to MemCsN_0 falling 2/	t_{P0}	V_{CC2} = 3.0 V	9,10,11		18	ns
Propagation delay, SysClk rising to CanTx_0 rising 2/	t_{P1}	V_{CC2} = 3.0 V	9,10,11		29	ns
Propagation delay, SysClk rising to Gpio_22 rising 2/	t_{P2}	V_{CC2} = 3.0 V	9,10,11		25	ns
Propagation delay, SysClk rising to FifoD_1 rising 2/	t_{P3}	V_{CC2} = 3.0 V	9,10,11		16	ns
Propagation delay, SpwClkSrc rising to SpwDout_P_0 falling 2/	t_{P4}	V_{CC2} = 3.0 V	9,10,11		14	ns
Propagation delay, SpwClkSrc rising to SpwDout_N_0 rising 2/	t_{P5}	V_{CC2} = 3.0 V	9,10,11		14	ns

1/ This parameter is tested initially and after major process changes, otherwise guaranteed.

2/ Unless otherwise specified the capacitance load shall be 50 pF in worst case. Input signals dynamic characteristics: tr, tf < 10 ns Threshold voltages: $V_{OL} = V_{OH} = V_{CC}/2$.

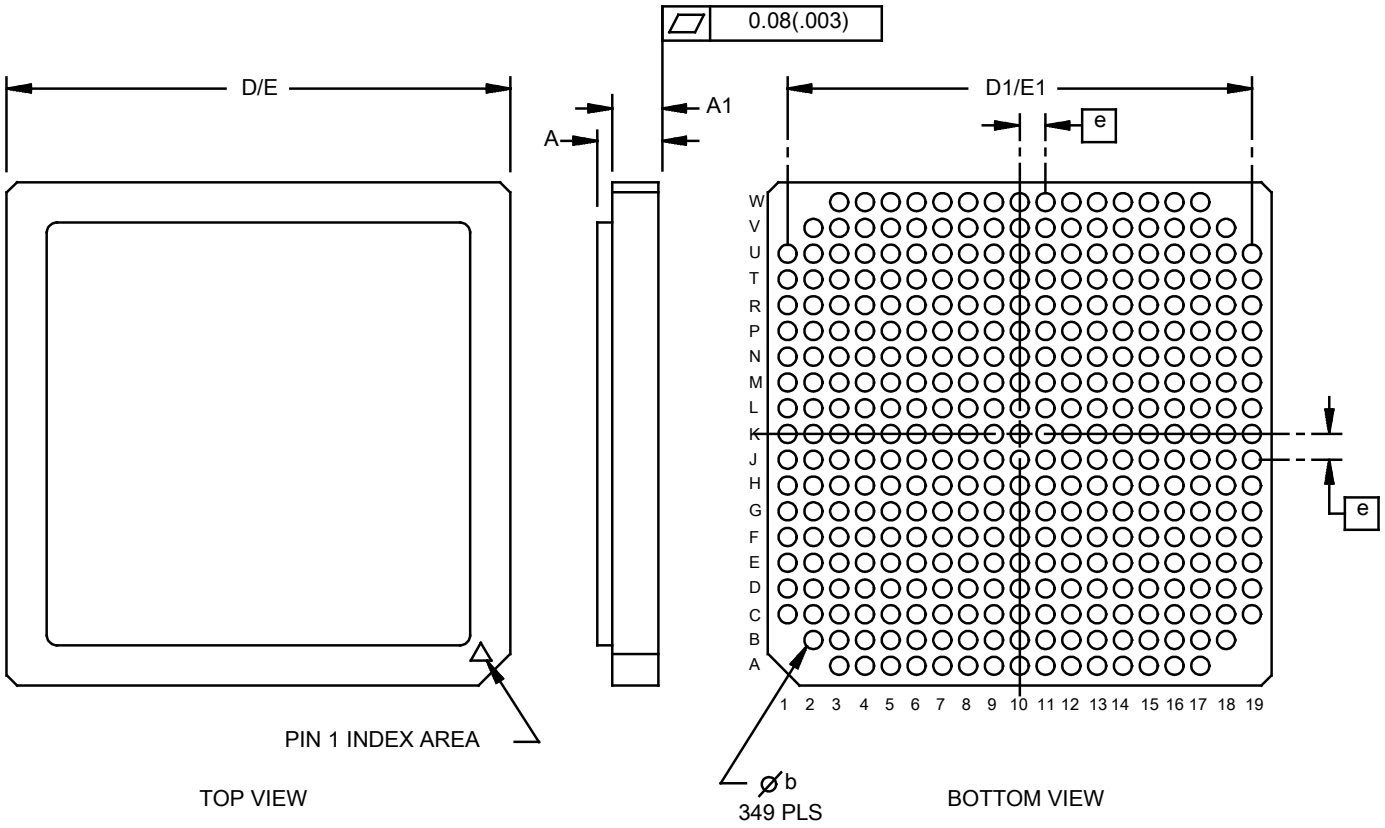
Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	4.30	5.90	.169	.232	D/E	24.80	25.20	.976	.992
A1	1.40	1.85	.055	.073	D1/E1	22.86 REF		.900 REF	
A2	2.40	3.45	.094	.136	e	1.27 REF		.050 REF	
b	0.79	0.99	.031	.040					

FIGURE 1. Case outline.

Case Y

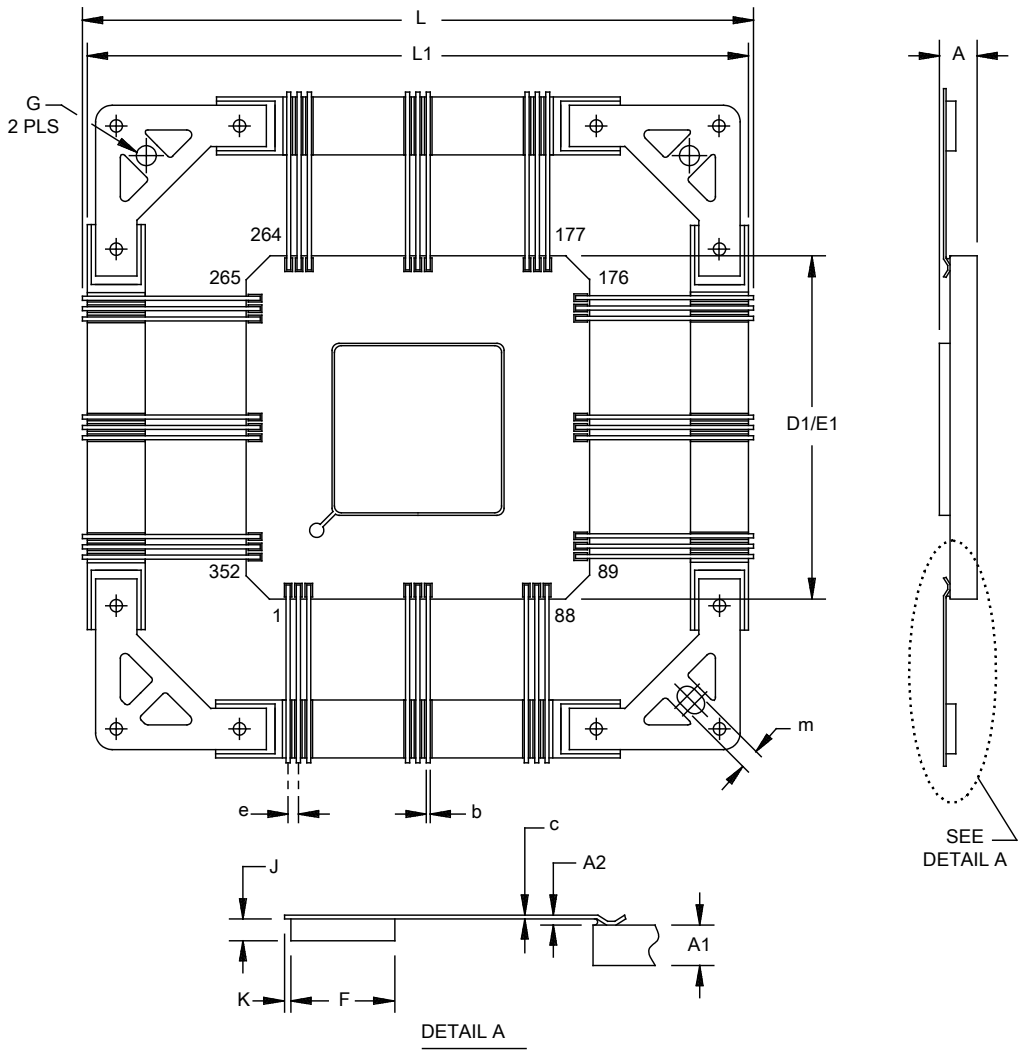


Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		3.40	D1/E1	22.86 REF	
A1	2.27	2.77	e	1.27 REF	
D/E	24.85	25.15			

NOTE: Lid is connected to ground

FIGURE 1. Case outline - Continued.

Case Z



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.75	3.75	.108	.148	G	2.50	2.60	.098	.104
A1	2.35	3.15	.092	.124	J	0.75	1.05	.029	.041
A2	0.05	0.35	.002	.014	K		0.50		.020
b	0.19	0.25	.007	.010	L	74.85	76.40	2.947	3.008
b1	0.18	0.22	.007	.009	L1	74.60	75.40	2.937	2.968
c	0.11	0.20	.004	.008	L2	55.60	57.00	2.189	2.244
D1/E1	47.52	48.48	1.871	1.908	L3	65.85	65.95	2.592	2.596
e	0.50 Basic		.0196 Basic		m	2.50	2.65	.098	.104
F	4.50	5.50	.177	.217					

FIGURE 1. Case outline - Continued.

Case outline X and Y

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
K5	ADAddr_0	F6	Fifop_0	M9	LeonPio_15	K17	MemD_14	A12	SpwSOut_P_0	J15	VDB22
L5	ADAddr_1	F4	Fifop_1	N7	LeonWDN	K15	MemD_15	M19	SpwSOut_P_1	J16	VDB23
K2	ADAddr_2	F2	FifoRdN	D11	LvdsRef	K13	MemD_16	R1	SysClk	G15	VDB24
K7	ADAddr_3	E4	FifoWrN	L16	LvdsRef2	J19	MemD_17	R4	SysResetN	F17	VDB25
L1	ADAddr_4	A9	Gpio_0	P9	MemA_0	H17	MemD_18	E10	Tap Tck	F18	VDB26
M3	ADAddr_5	B9	Gpio_1	R8	MemA_1	J18	MemD_19	G10	Tap Tdi	D17	VDB30
L2	ADAddr_6	C9	Gpio_2	N9	MemA_2	J17	MemD_20	B10	Tap Tdo	V18	VSA0
L3	ADAddr_7	D9	Gpio_3	V9	MemA_3	K11	MemD_21	C10	Tap Tms	V4	VSA1
P2	ADCs	F9	Gpio_4	U9	MemA_4	H15	MemD_22	E9	Tap TrstN	W4	VSA2
K9	ADData_0	J10	Gpio_5	P10	MemA_5	H19	MemD_23	H8	TestMode	B18	VSA3
M5	ADData_1	E8	Gpio_6	M10	MemA_6	J12	MemD_24	H3	TestSE	A4	VSA4
M1	ADData_2	B8	Gpio_7	W10	MemA_7	H18	MemD_25	J5	TimeClk	A16	VSA5
L8	ADData_3	E7	Gpio_8	R9	MemA_8	G17	MemD_26	K4	TimeTrig_1	B2	VSA6
M4	ADData_4	D8	Gpio_9	T10	MemA_9	J13	MemD_27	K3	TimeTrig_2	B16	VSA7
N3	ADData_5	C7	Gpio_10	R11	MemA_10	H14	MemD_28	V17	VDA0	C3	VSA8
L7	ADData_6	G9	Gpio_11	V10	MemA_11	F15	MemD_29	V16	VDA1	C17	VSA9
M6	ADData_7	F8	Gpio_12	N10	MemA_12	G18	MemD_30	W3	VDA2	D1	VSA10
N1	ADData_8	A7	Gpio_13	W11	MemA_13	J11	MemD_31	B17	VDA3	D19	VSA11
P5	ADData_9	E6	Gpio_14	U12	MemA_14	P13	MemOeN_0	A3	VDA4	T1	VSA12
N2	ADData_10	B7	Gpio_15	T11	MemA_15	V14	MemOeN_1	A17	VDA5	T19	VSA13
P3	ADData_11	C6	Gpio_16	P11	MemA_16	U16	MemOeN_2	B3	VDA6	U3	VSA14
N4	ADData_12	D7	Gpio_17	L10	MemA_17	W15	MemOeN_3	B4	VDA7	U17	VSA15
L9	ADData_13	J9	Gpio_18	R12	MemA_18	V13	MemWrN_0	C1	VDA8	V2	VSA16
T2	ADData_14	A6	Gpio_19	W12	MemA_19	U14	MemWrN_1	C2	VDA9	W16	VSA17
P4	ADData_15	F7	Gpio_20	R13	MemA_20	T13	MemWrN_2	C18	VDA10	D12	VSB0
N6	ADRc	D6	Gpio_21	T12	MemA_21	L11	MemWrN_3	C19	VDA11	H10	VSB1
L4	ADRdy	C5	Gpio_22	U13	MemA_22	A14	PVDDPLL	U1	VDA12	H9	VSB2
L6	ADTrig	B6	Gpio_23	D14	MemBExcN	F14	PVSSPLL	U2	VDA13	B5	VSB3
R3	ADWr	D16	IoBrdyN	F19	MemCB_0	N11	RomCsN_0	U18	VDA14	D2	VSB4
E2	CanEn_0	C16	IoCsN	D18	MemCB_1	P12	RomCsN_1	U19	VDA15	H7	VSB5
D4	CanEn_1	B14	IoOeN	F16	MemCB_2	A10	SpwClk10Mbit_0	V3	VDA16	J6	VSB6
D5	CanRx_0	D15	IoRead	E17	MemCB_3	E11	SpwClk10Mbit_1	W17	VDA17	K8	VSB7
G8	CanRx_1	A15	IoWrN	E19	MemCB_4	D10	SpwClk10Mbit_2	G12	VDB0	N5	VSB8
C4	CanTx_0	R7	LeonDsuAct	E16	MemCB_5	D13	SpwClkMult_0	F10	VDB1	T3	VSB9
A5	CanTx_1	V8	LeonDsuBre	H13	MemCB_6	H12	SpwClkMult_1	A8	VDB2	P8	VSB10
G4	FifoD_0	N8	LeonDsuEn	G13	MemCB_7	H11	SpwClkMuxSel	G7	VDB3	U8	VSB11
G2	FifoD_1	U7	LeonDsuRx	T15	MemCsN_0	C14	SpwClkPllCnfg_0	F1	VDB4	R10	VSB12
F3	FifoD_2	T8	LeonDsuTx	N12	MemCsN_1	A13	SpwClkPllCnfg_1	J8	VDB5	U11	VSB13
G1	FifoD_3	M7	LeonErrorN	T16	MemCsN_2	E14	SpwClkPllCnfg_2	H6	VDB6	V12	VSB14
F5	FifoD_4	P7	LeonPio_0	N14	MemCsN_3	B13	SpwClkSrc	K6	VDB7	R14	VSB15
H4	FifoD_5	T4	LeonPio_1	T17	MemD_0	C11	SpwDln_N_0	M2	VDB8	U15	VSB16
G3	FifoD_6	W5	LeonPio_2	R19	MemD_1	L17	SpwDln_N_1	V5	VDB9	R18	VSB17
H2	FifoD_7	T5	LeonPio_3	R16	MemD_2	B11	SpwDln_P_0	W8	VDB10	P14	VSB18
G5	FifoD_8	V6	LeonPio_4	P16	MemD_3	L18	SpwDln_P_1	W9	VDB11	N18	VSB19

FIGURE 2. Terminal connections.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
H1	FifoD_9	U4	LeonPio_5	P19	MemD_4	E13	SpwDOut_N_0	U10	VDB12	M16	VSB20
H5	FifoD_10	T6	LeonPio_6	T18	MemD_5	N15	SpwDOut_N_1	V11	VDB13	K12	VSB21
J7	FifoD_11	W6	LeonPio_7	N16	MemD_6	B12	SpwDOut_P_0	M11	VDB14	K18	VSB22
J2	FifoD_12	P6	LeonPio_8	P17	MemD_7	M18	SpwDOut_P_1	W13	VDB15	J14	VSB23
J3	FifoD_13	T7	LeonPio_9	N19	MemD_8	C12	SpwSln_N_0	T14	VDB16	H16	VSB24
J1	FifoD_14	M8	LeonPio_10	P15	MemD_9	M17	SpwSln_N_1	N13	VDB17	G16	VSB25
K1	FifoD_15	V7	LeonPio_11	L12	MemD_10	A11	SpwSln_P_0	P18	VDB18	G14	VSB26
D3	FifoEmpN	U6	LeonPio_12	K19	MemD_11	L19	SpwSln_P_1	M12	VDB19	F13	VSB30
G6	FifoFullN	W7	LeonPio_13	L15	MemD_12	F12	SpwSOut_N_0	M13	VDB20		
E1	FifoHalfN	R6	LeonPio_14	K16	MemD_13	M14	SpwSOut_N_1	K14	VDB21		

Not connected pins: B15, C8, C13, C15, E3, E5, E12, E15, E18, F11, G11, G19, J4, K10, L13, L14, M15, N17, P1, R2, R5, R15, R17, T9, U5, V15, W14.

NOTE:

VDA* are core power pins, VSA* are core ground pins
VDB* are buffer power pins, VSB* are buffer ground pins

FIGURE 2. Terminal connections - Continued.

Case outline Z

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
3	CanEn_0	47	ADAddr_0	94	LeonPio_1	138	MemA_12	185	MemD_1
4	CanEn_1	48	ADAddr_1	95	VSA8	139	MemA_13	186	MemD_2
5	FifoFullN	49	ADAddr_2	96	VDA8	140	MemA_14	187	VDB18
6	FifoEmpN	50	ADAddr_3	97	LeonPio_2	141	VDB13	188	VSB18
7	VSA4	51	ADAddr_4	98	LeonPio_3	142	VSB13	189	MemD_3
8	VDA4	52	ADAddr_5	99	LeonPio_4	145	MemA_15	191	MemD_4
9	FifoHalfN	53	ADAddr_6	100	LeonPio_5	146	MemA_16	192	MemD_5
10	FifoWrN	54	ADAddr_7	101	LeonPio_6	147	MemA_17	193	MemD_6
11	FifoRdN	57	ADRdy	104	LeonPio_7	148	MemA_18	194	VDB19
12	FifoP_0	58	ADTrig	105	LeonPio_8	149	MemA_19	195	VSB19
13	FifoP_1	59	ADData_0	106	LeonPio_9	150	VDB14	196	MemD_7
16	VDB4	60	ADData_1	107	LeonPio_10	151	VSB14	197	MemD_8
17	VSB4	61	ADData_2	108	LeonPio_11	152	MemA_20	198	MemD_9
18	FifoD_0	62	ADData_3	109	LeonPio_12	153	MemA_21	199	MemD_10
19	TestMode	63	VDB8	110	LeonPio_13	154	MemA_22	200	VDB20
20	FifoD_1	64	VSB8	111	LeonPio_14	155	RomCsN_0	202	VSB20
21	FifoD_2	65	ADData_4	112	LeonPio_15	156	RomCsN_1	203	SpwDOut_P_1
22	FifoD_3	66	ADData_5	113	LeonDsuEn	157	VDB15	205	SpwDOut_N_1
23	FifoD_4	67	ADData_6	114	LeonDsuTx	158	VSB15	206	SpwSOut_P_1
24	VDB5	68	ADData_7	115	LeonDsuRx	159	MemWrN_0	208	SpwSOut_N_1
25	VSB5	69	ADData_8	116	LeonDsuBre	160	MemWrN_1	210	LvdsRef2
26	FifoD_5	70	ADData_9	117	LeonDsuAct	161	MemWrN_2	211	SpwDIn_P_1
27	FifoD_6	71	ADData_10	118	VDB10	162	MemWrN_3	212	SpwDIn_N_1
28	FifoD_7	72	ADData_11	119	VSB10	164	MemOeN_0	213	SpwSIn_P_1
29	FifoD_8	73	ADData_12	120	MemA_0	165	VDB16	214	SpwSIn_N_1
30	FifoD_9	74	ADData_13	121	MemA_1	166	VSB16	215	VDB21
31	VDB6	76	ADData_14	124	MemA_2	167	MemOeN_1	217	VSB21
32	VSB6	77	ADData_15	125	MemA_3	168	MemOeN_2	218	MemD_11
33	FifoD_10	78	ADWr	126	MemA_4	169	VSA10	219	MemD_12
36	FifoD_11	79	ADCs	127	VDB11	170	VDA10	220	MemD_13
37	FifoD_12	80	ADRc	128	VSB11	171	MemOeN_3	221	MemD_14
38	FifoD_13	81	VSA6	129	MemA_5	172	MemCsN_0	222	MemD_15
39	FifoD_14	82	VDA6	130	MemA_6	173	MemCsN_1	223	VDB22
40	TestSE	83	SysClk	131	MemA_7	175	VDB17	224	VSB22
41	VDB7	84	SysResetN	132	MemA_8	179	VSB17	225	MemD_16
42	VSB7	85	LeonErrorN	133	MemA_9	180	MemCsN_2	226	MemD_17
43	FifoD_15	87	LeonWDN	134	VDB12	181	MemCsN_3	227	MemD_18
44	TimeClk	91	VDB9	135	VSB12	182	MemD_0	228	MemD_19
45	TimeTrig_1	92	VSB9	136	MemA_10	183	VSA12	230	MemD_20
46	TimeTrig_2	93	LeonPio_0	137	MemA_11	184	VDA12	231	VDB23

FIGURE 2. Terminal connections - Continued.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
233	VSB23	257	VSA14	283	SpwClkSrc	309	TapTms	333	Gpio_14
234	MemD_21	258	VDA14	284	SpwClkPllCnfg_0	310	TapTck	334	Gpio_15
235	MemD_22	259	VSB26	285	SpwClkPllCnfg_1	311	TapTrstN	335	Gpio_16
236	MemD_23	260	MemCB_4	286	SpwClkPllCnfg_2	312	TapTdo	336	Gpio_17
237	MemD_24	261	MemCB_5	287	SpwClkMuxSel	313	TapTdi	337	Gpio_18
238	MemD_25	262	MemCB_6	288	VDB0	314	Gpio_0	338	Gpio_19
239	VDB24	263	MemCB_7	290	VSB0	317	Gpio_1	339	Gpio_20
240	VSB24	267	VDB30	291	SpwDOut_P_0	318	Gpio_2	340	Gpio_21
241	MemD_26	268	VSB30	293	SpwDOut_N_0	319	Gpio_3	341	Gpio_22
242	MemD_27	269	IoBrdyN	294	SpwSOut_P_0	320	Gpio_4	342	Gpio_23
243	MemD_28	270	IoWrN	296	SpwSOut_N_0	322	Gpio_5	343	CanTx_0
247	MemD_29	271	VSA1	298	LvdsRef	323	Gpio_6	344	CanTx_1
248	MemD_30	272	VDA1	299	SpwDIn_P_0	324	VDB2	345	VSA2
249	VDB25	273	IoRead	300	SpwDIn_N_0	325	VSB2	346	VDA2
250	VSB25	274	IoOeN	301	SpwSIn_P_0	326	Gpio_7	347	CanRx_0
251	MemD_31	275	IoCsN	302	SpwSIn_N_0	327	Gpio_8	348	CanRx_1
252	MemCB_0	276	MemBExcN	303	VDB1	328	Gpio_9	349	VDB3
253	MemCB_1	279	PVDDPLL	305	VSB1	329	Gpio_10	351	VSB3
254	MemCB_2	280	PVSSPLL	306	SpwClk10Mbit_0	330	Gpio_11		
255	MemCB_3	281	SpwClkMult_0	307	SpwClk10Mbit_1	331	Gpio_12		
256	VDB26	282	SpwClkMult_1	308	SpwClk10Mbit_2	332	Gpio_13		

Not connected pins: 1, 2, 14, 15, 34, 35, 55, 56, 75, 86, 88, 89, 90, 102, 103, 122, 123, 143, 144, 163, 174, 176, 177, 178, 190, 201, 204,;207, 209, 216, 229, 232, 244, 245, 246, 264, 265, 266, 277, 278, 289, 292, 295, 297, 304, 315, 316, 321, 350, 352.

NOTES:

VDA* are core power pins,
VSA* are core ground pins.
VDB* are buffer power pins,
VSB* are buffer ground pins.

FIGURE 2. Terminal connections - Continued.

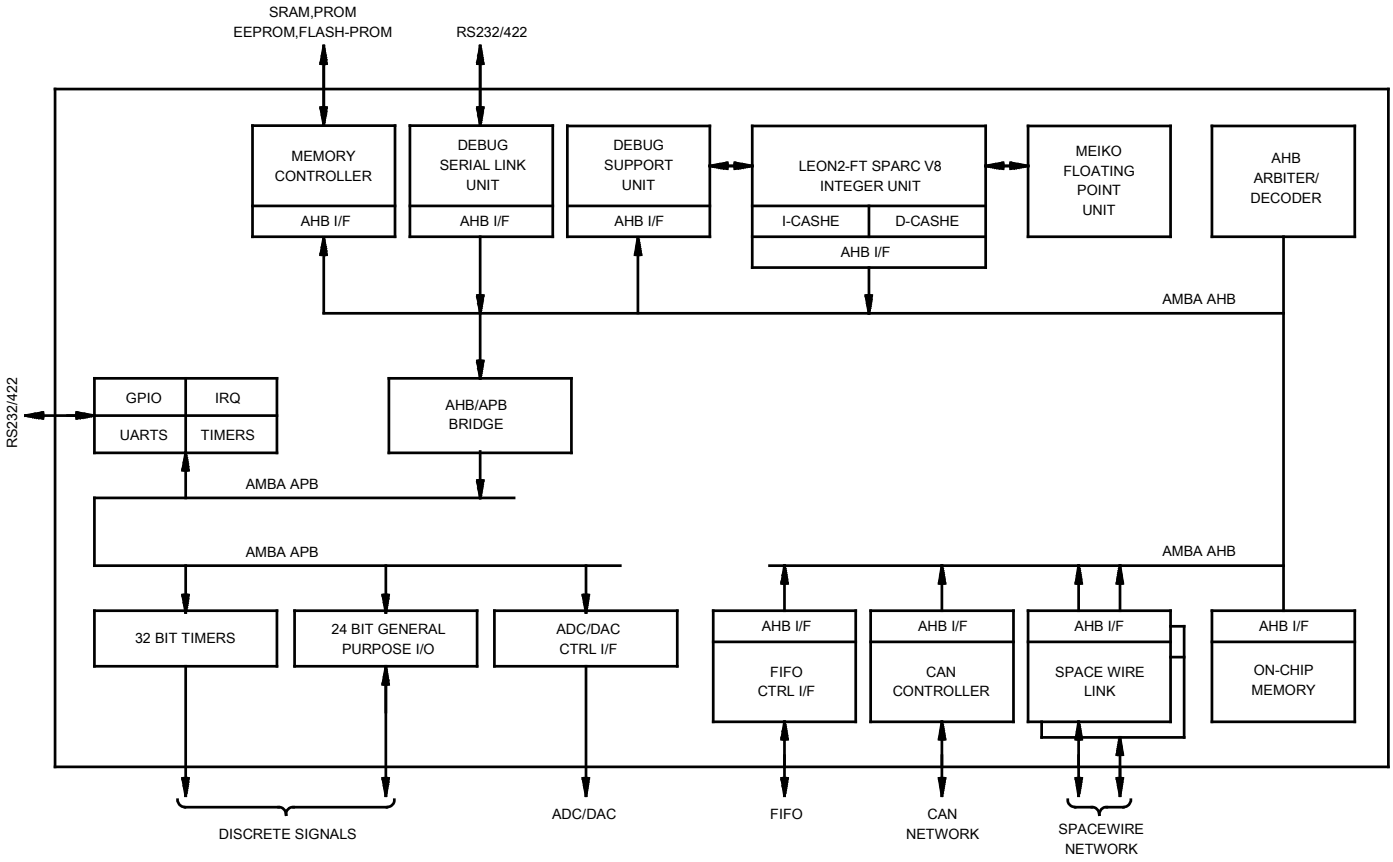


FIGURE 3. Block diagram.

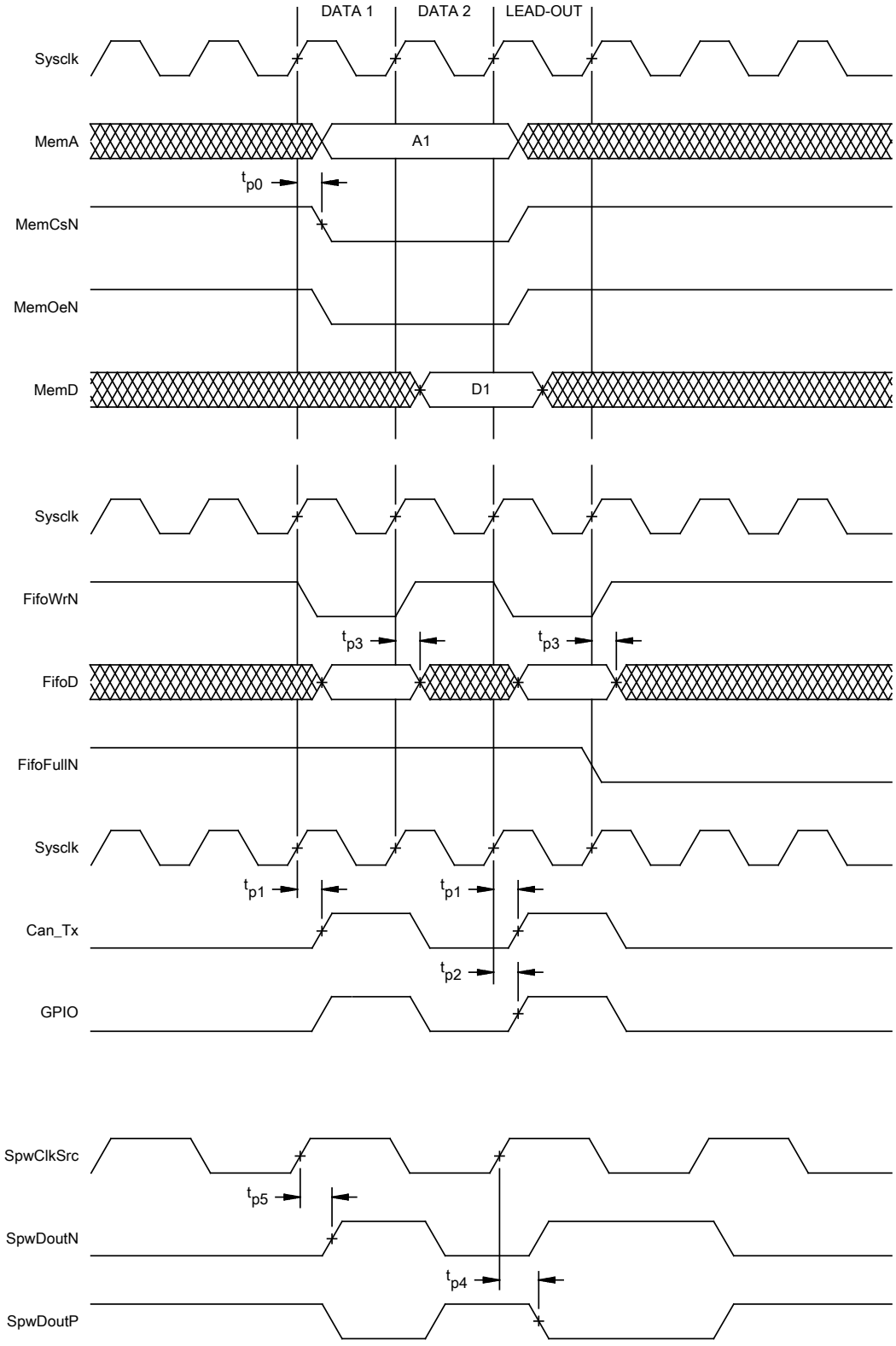


FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection..

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1, 2, 3, 4, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 7, 8, 9, 10, 11, Δ 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9, Δ
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in delta parameters (25°C).

Parameter	Limit	Unit
I_{IL}/I_{IH}	+/- 10% of specificied value in table 1	µA
I_{OZL}/I_{OZH}	+/- 10% of specificied value in table 1	µA
I_{CCSB}	+/- 10% of specificied value in table 1	mA

NOTE: The parameters shall be recorded before and after the required burn-in and lifetest to determine the delta limits.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.
c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5 krads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-02-11

Approved sources of supply for SMD 5962-10A03 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-10A0301QXB	F7400	AT7913E2H-MQ
5962-10A0301VXB	F7400	AT7913E2H-SV
5962R10A0301VXB	F7400	AT7913E2H-SR
5962-10A0301QYC	F7400	AT7913E2U-MQ
5962-10A0301VYC	F7400	AT7913E2U-SV
5962R10A0301VYC	F7400	AT7913E2U-SR
5962-10A0301QZC	F7400	AT7913EYC-MQ
5962-10A0301VZC	F7400	AT7913EYC-SV
5962R10A0301VZC	F7400	AT7913EYC-SR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes La Chantrerie 44306 Nantes Cedex3 France