PL610-01

1.8V to 3.3V, 1 MHz to 130 MHz XO IC

Features

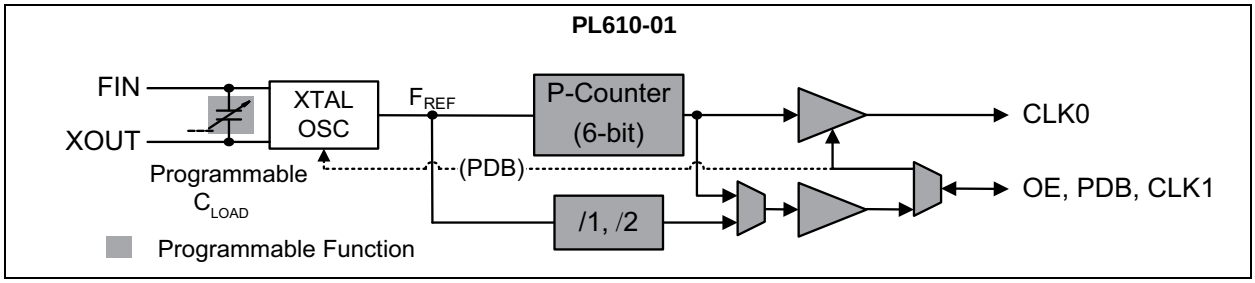
- Wide Frequency Coverage, Programmable, Advanced Oscillator Design
- Programmable “Odd/Even” Divider up to ÷63
- Direct Oscillation Operation with Optional Programmable Features:
  - Output Drive Strength (4 mA, 8 mA, or 16 mA)
  - 6-bit Odd/Even Output Divider
- Input Frequency:
  - Fundamental Crystal: 5 MHz to 130 MHz
  - Reference Clock: 1 MHz to 130 MHz
- Supports CMOS or Sine Wave Input Clock
- Output Frequency: 20 kHz to 130 MHz
- Very Low Jitter and Phase Noise
- Low Current Consumption
- Single 1.8V ~ 3.3V ±10% Power Supply
- Operating Temperature Range from –40°C to +85°C
- Available in 6-pin TDFN or SOT-23 GREEN/RoHS-Compliant Packaging

General Description

The PL610 is a high performance general purpose oscillator IC for outputs up to 130 MHz. Designed to fit in a small 2 mm x 1.3 mm TDFN or 3 mm x 3 mm SOT-23 package, the PL610 offers the best phase noise and jitter performance as well as the lowest power consumption of any comparable IC.

In addition, there is a ‘6’ bit optional programmable Odd/Even divider (default = ÷1), and ‘3’ programmable output drive strengths (4 mA, 8 mA [default], 16 mA) to choose from. The full feature set of the PL610 makes it the most versatile XO for any application.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}) ..... –0.5V to +4.6V
Input Voltage (V_{IN})..... –0.5V to V_{DD} + 0.5V
Output Voltage (V_{OUT})..... –0.5V to V_{DD} + 0.5V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Parts are tested to commercial grade only.

TABLE 1-1: AC ELECTRICAL CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Crystal Input Frequency	—	5	—	130	MHz	Fundamental Crystal
FIN Input Frequency	—	1	—	130	MHz	@ V_{DD} = 3.3V
						@ V_{DD} = 2.5V
						@ V_{DD} = 1.8V
FIN Input Signal Amplitude	—	0.9	—	V_{DD}	V_{PP}	Internally AC-coupled (High Frequency)
		0.1	—	V_{DD}		Internally AC-coupled (Low Frequency) 3.3V <50 MHz, 2.5V <40 MHz, 1.8V <15 MHz
Output Frequency	—	0.02	—	130	MHz	@ V_{DD} = 1.8V-3.3V
V_{DD} Sensitivity	—	–2	—	2	ppm	Frequency vs. V_{DD} ±10%
Output Rise Time (see Figure 5-1)	—	—	1	1.2	ns	15 pF Load, 10/90% V_{DD}, High Drive, 3.3V
Output Fall Time (see Figure 5-1)	—	—	1	1.2	ns	15 pF Load, 10/90% V_{DD}, High Drive, 3.3V
Duty Cycle (Note 1, see Figure 5-1)	—	45	50	55	%	—

Note 1: For 1.8V operation, the 50% ±5% duty cycle is guaranteed for frequencies ≤40 MHz.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current, Dynamic, with Loaded CMOS Output	I_{DD}	—	3.4	—	mA	V_{DD} = 3.3V, 25 MHz, Load = 15 pF
		—	2.1	—		V_{DD} = 2.5V, 25 MHz, Load = 10 pF
		—	0.9	—		V_{DD} = 1.8V, 25 MHz, Load = 5 pF
		—	0.65	—		V_{DD} = 1.8V, 2.0 MHz, Load = 5 pF
Operating Voltage	V_{DD}	1.62	—	3.63	V	—
Output Low Voltage	V_{OL}	—	—	0.1	V	I_{OL} = +4 mA Standard Drive
Output High Voltage	V_{OH}	V_{DD} – 0.4	—	—	V	I_{OH} = –4 mA Standard Drive
Output Current, Low Drive (See Figure 5-2)	I_{OLD}	4	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V
Output Current, Standard Drive (See Figure 5-2)	I_{OSD}	8	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V
Output Current, High Drive (See Figure 5-2)	I_{OHD}	16	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V

TABLE 1-3: CRYSTAL SPECIFICATIONS (5 MHZ TO 60 MHZ)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Fundamental Crystal Resonator Frequency	F_{XIN}	5	—	60	MHz	—
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L(XTAL)}$	8	—	12	pF	—
Maximum Sustainable Drive Level	—	—	—	100	µW	—
Operating Drive Level	—	—	25	—	µW	—
Crystal Shunt Capacitance	C0	—	—	3	pF	—
Effective Series Resistance, Fundamental, (See Figure 5-4)	ESR	—	—	50	Ω	—

TABLE 1-4: CRYSTAL SPECIFICATIONS (60 MHZ TO 130 MHZ)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Fundamental Crystal Resonator Frequency	F_{XIN}	60	—	130	MHz	—
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L(XTAL)}$	5	—	8	pF	—
Maximum Sustainable Drive Level	—	—	—	100	µW	—
Operating Drive Level	—	—	25	—	µW	—
Crystal Shunt Capacitance	C0	—	—	2.5	pF	—
Effective Series Resistance, Fundamental, (See Figure 5-4)	ESR	—	—	30	Ω	—

TABLE 1-5: KEY PROGRAMMING PARAMETERS (OPTIONAL)

CLK[0:1] Output Frequency	Output Drive Strength	Programmable Input/Output
$F_{OUT} = F_{REF} \div P$* (*: P is an Odd/Even Divider) Where P = 6 bit CLK0 = F_{REF}, $F_{REF}/2$ or F_{REF}/P CLK1 = F_{REF}, $F_{REF}/2$ or CLK0	Three optional drive strengths to choose from: • Low: 4 mA • Std: 8 mA (default) • High: 16 mA	One output pin can be configured as: • OE - input • PDB - input • CLK1 – output

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Ambient Operating Temperature	T_A	–40	—	+85	°C	—

Note 1: Exposure of the device under conditions beyond the limits specified by the maximum ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

Pin Configurations

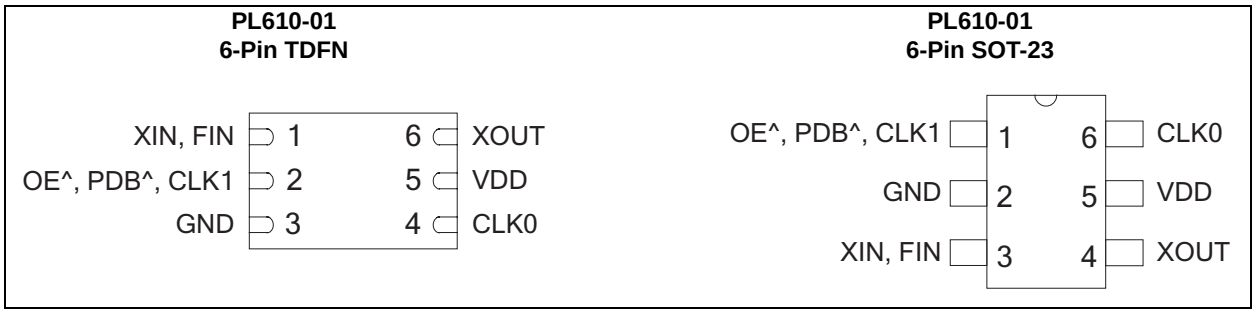


TABLE 2-1: PIN FUNCTION TABLE

6-Pin TDFN Pin Number	6-Pin SOT-23 Pin Number	Name	Type	Description
1	3	XIN, FIN	I	Crystal or Reference Clock input pin
2	1	OE, PDB, CLK1	I/O	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down input (PDB) input or CLK1 clock output. This pin has an internal 60 kΩ pull-up resistor for OE and 10 MΩ pull up resistor for PDB.
				State / **OE** / **PDB**
				0 / Tri-State CLK / Power Down Mode
				1 (default) / Normal Mode / Normal Mode
3	2	GND	P	GND connection
4	6	CLK0	O	Programmable Clock Output
5	5	VDD	P	V_{DD} connection
6	4	XOUT	O	Crystal Output pin. Do Not Connect (DNC) when FIN is present.

3.0 FUNCTIONAL DESCRIPTION

PL610-01 is a highly featured, very flexible, advanced XO design for high performance, low-power, small form-factor applications. The PL610-01 accepts a fundamental input crystal of 5 MHz to 130 MHz or a reference clock input of 1 MHz to 130 MHz and is capable of producing two outputs up to 130 MHz. This flexible design allows the PL610-01 to deliver any frequency, F_{REF} (Crystal or Ref Clk) frequency, $F_{REF}/2$ or F_{REF}/P to CLK0 and/or CLK1. Some of the design features of the PL610-01 are mentioned below.

3.1 Clock Output (CLK0)

CLK0 is the main clock output. The output from CLK0 can be F_{REF} (Crystal or Ref Clk), $F_{REF}/2$ or F_{REF}/P output. The output drive level can be programmed to Low Drive (4 mA), Standard Drive (8 mA), or High Drive (16 mA).

3.2 Programmable I/O (OE/PDB/CLK1)

The PL610-01 provides one programmable I/O pin which can be configured as one of the following functions:

3.2.1 OUTPUT ENABLE (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 60 kΩ pull-up resistor giving a default condition of logic “1”.

3.2.2 POWER DOWN CONTROL (PDB)

The Power Down (PDB) feature allows the user to put the PL610-01 into “Sleep Mode.” When activated (logic ‘0’), PDB disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10 µA of power. The PDB pin incorporates a 10 MΩ pull-up resistor giving a default condition of logic “1”.

3.2.3 CLOCK OUTPUT (CLK1)

The CLK1 feature allows the PL610-01 to have an additional clock output programmed to one of the following:

- F_{REF} - Reference (Crystal or Ref Clk) Frequency
- $F_{REF}/2$
- CLK0

4.0 LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance-optimized PCB design.

4.1 Signal Integrity and Termination Considerations

- Keep traces short.
- Trace = Inductor. With a capacitive load this creates ringing.
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

4.2 Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply.
- Multiple V_{DD} pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with V_{DD} can help prevent noise from other board sources.
- Value of decoupling capacitor is frequency dependent. Typical values to use are 0.1 µF for designs using crystals <50 MHz and 0.01 µF for designs using crystals >50 MHz.

4.3 Typical CMOS Termination

Place series resistor as close as possible to the CMOS output.

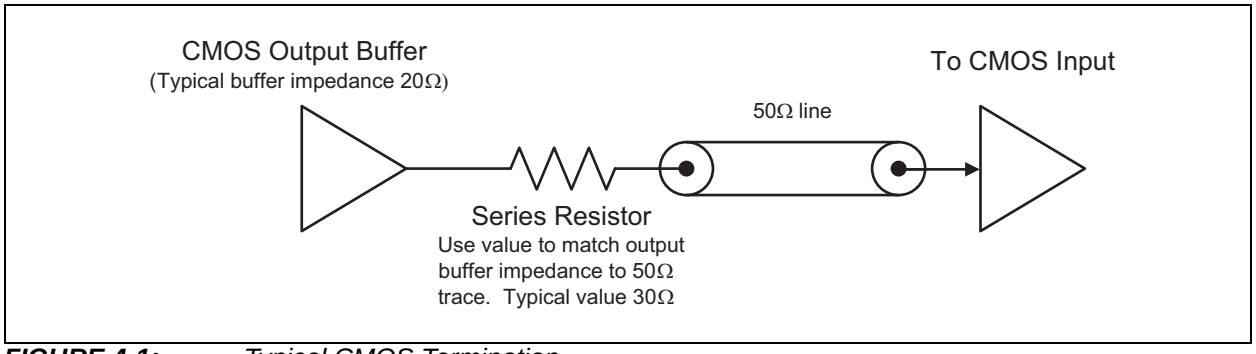
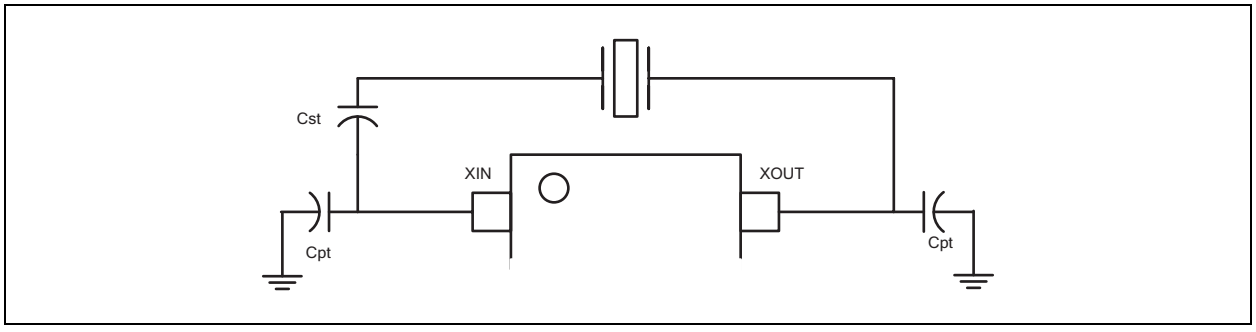


FIGURE 4-1: *Typical CMOS Termination.*

4.4 Crystal Tuning Circuit

Series and parallel capacitors are used to fine tune the crystal load to the circuit load.



CST: Series capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a C_{LOAD} of equal or greater value than the oscillator.

CPT: Parallel capacitors, used to raise the circuit load to match the crystal load. Lowers frequency offset.

5.0 MEASUREMENT TEST CIRCUITS (MTC)

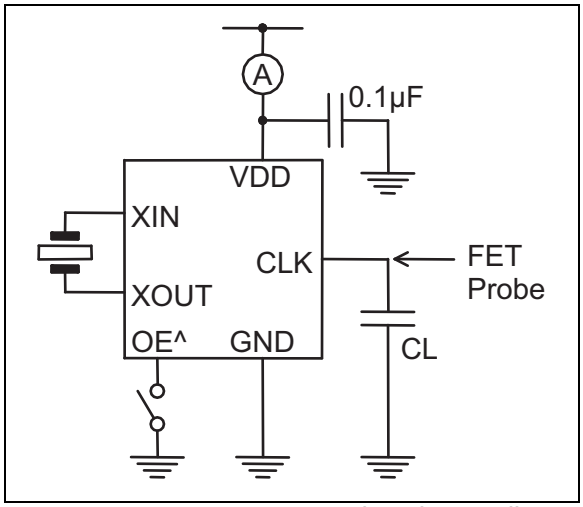


FIGURE 5-1: *MTC-1: Rise Time, Fall Time, Duty Cycle, V_{OL}, V_{OH}, I_{DD}, Power Down Current, Output Enable/Disable.*

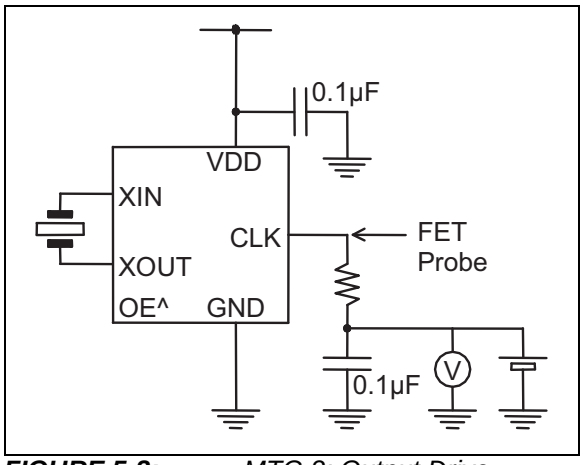


FIGURE 5-2: *MTC-2: Output Drive Current and Output Impedance.*

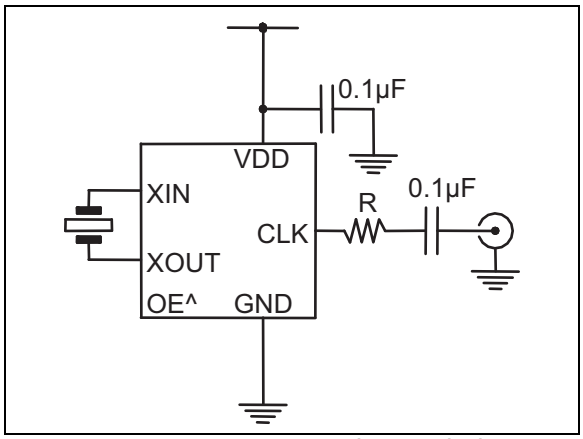


FIGURE 5-3: *MTC-3: Jitter and Phase Noise.*

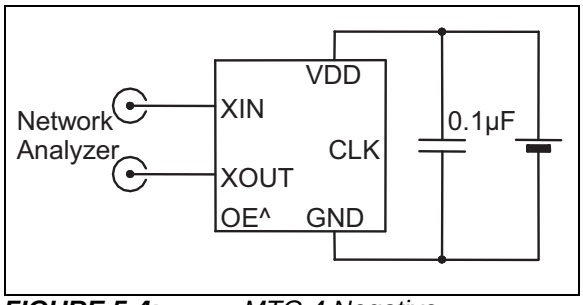


FIGURE 5-4: *MTC-4 Negative Resistance.*

6.0 WAVEFORM SWITCHING CHARACTERISTICS

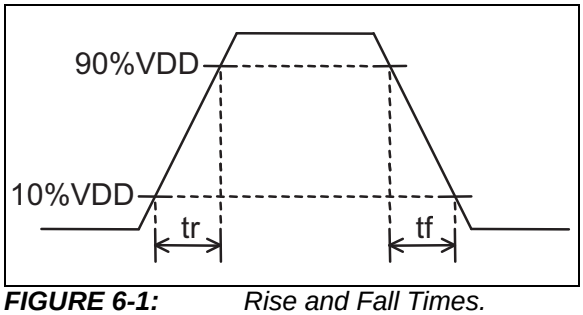


FIGURE 6-1: *Rise and Fall Times.*

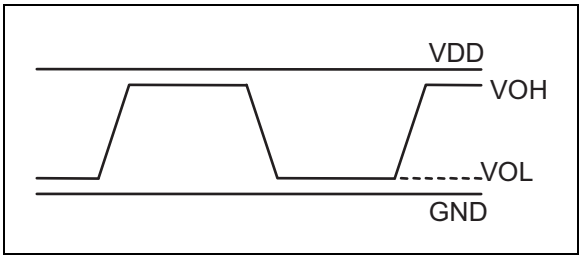


FIGURE 6-2: V_{OH}, V_{OL}.

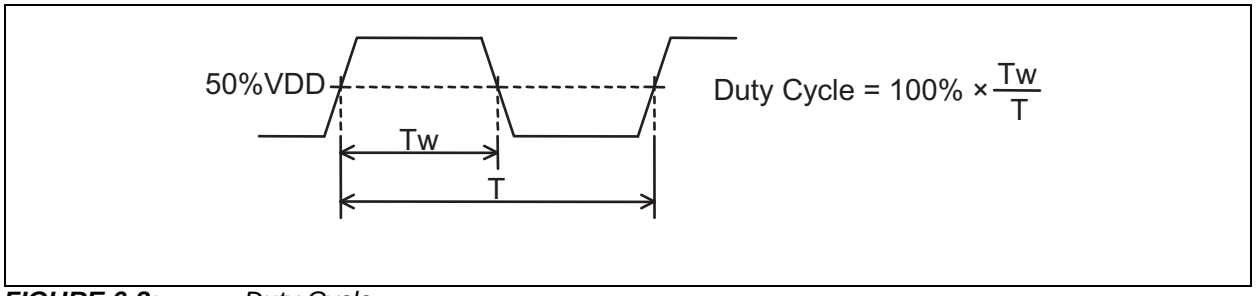


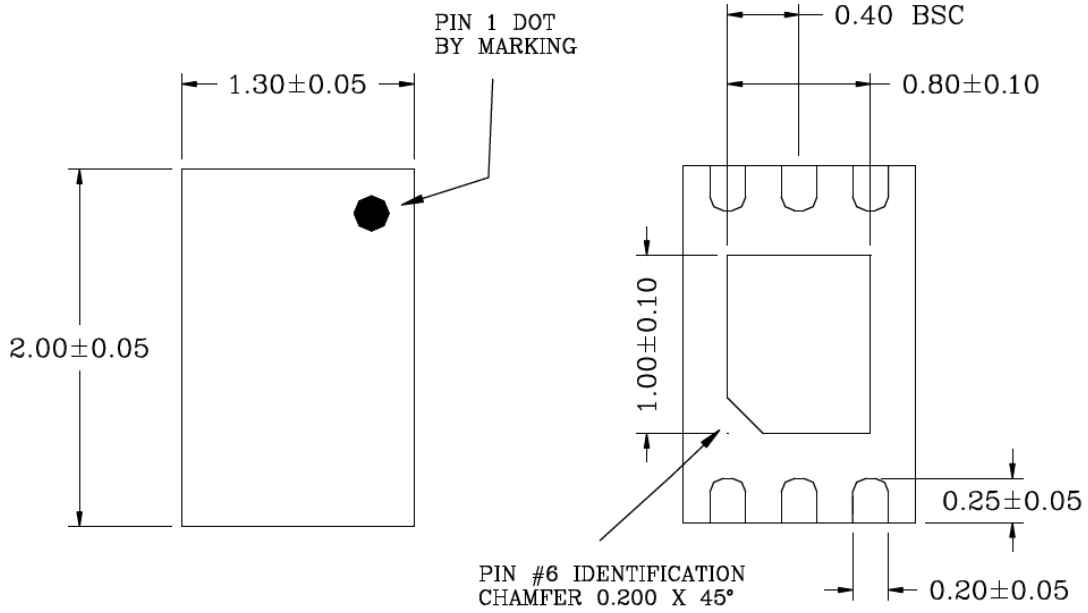
FIGURE 6-3: *Duty Cycle.*

7.0 PACKAGING INFORMATION

6-Pin TDFN 2.0 mm x 1.3 mm Package Outline and Recommended Land Pattern

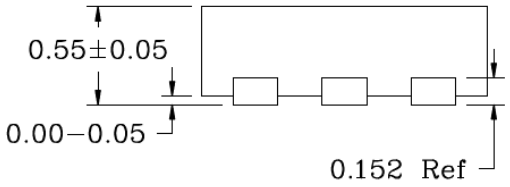
TITLE
6 LEAD TDFN 2.0x1.3 mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TDFN2013-6LD-PL-1	**UNIT**	MM
Lead Frame	NiPdAu	**Lead Finish**	NiPdAu



TOP VIEW
NOTE: 1, 2

BOTTOM VIEW
NOTE: 1, 2



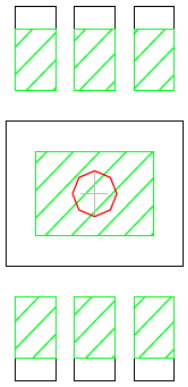
SIDE VIEW
NOTE: 1, 2

NOTES
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mmm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. UNIT IN mm.
5. SHADED AREA IS SOLDER STENCIL OPENING.
6. RECOMMENDED VIA SIZE IS 0.30-0.35mm.

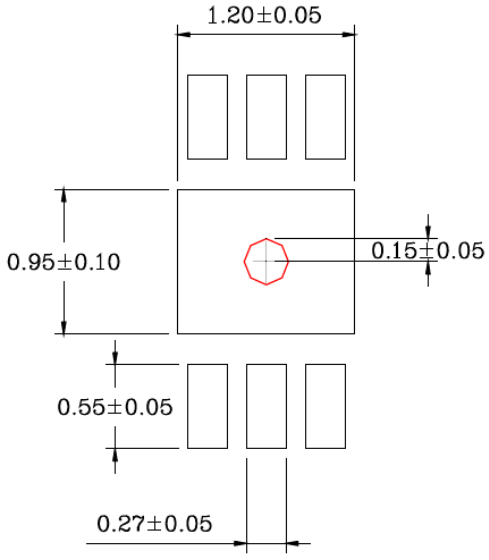
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern TDFN2013-6LD-PL-1

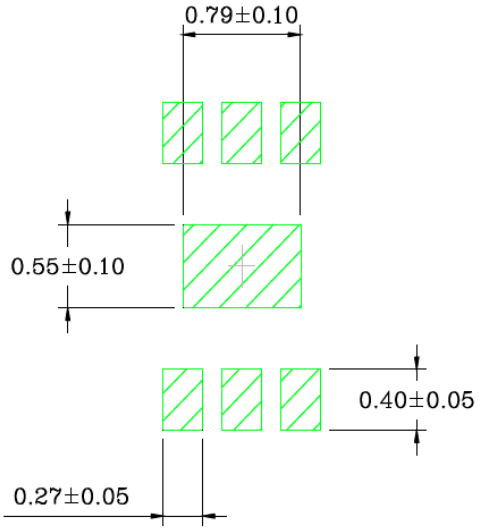
RECOMMENDED LAND PATTERN



STACKED-UP
NOTE: 4, 5, 6



EXPOSED METAL TRACE
NOTE: 4, 6



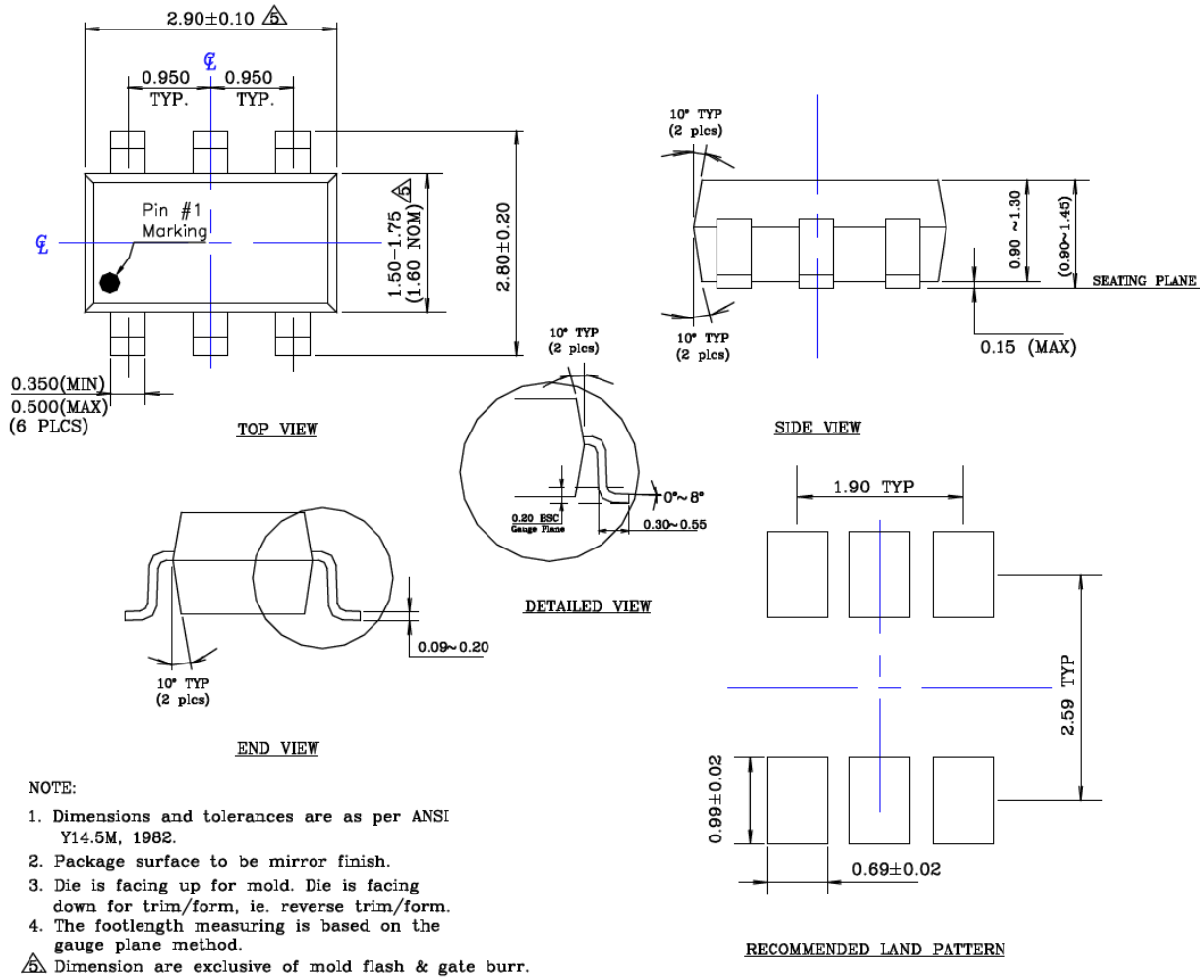
SOLDER STENCIL OPENING
NOTE: 4, 5

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

6-Pin SOT-23 Package Outline and Recommended Land Pattern

TITLE
6 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT23-6LD-PL-1	UNIT	MM



NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the gauge plane method.
5. Dimension are exclusive of mold flash & gate burr.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2016)

- Converted Micrel document PL610-01 to Microchip data sheet DS20005615A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	—	XXX	X	X	—	XX
Device		ID Code	Package	Temperature		Media Type

Device:	PL610-01:	1.8V to 3.3V, 1 MHz to 130 MHz XO IC
ID Code:	XXX =	3 Digit ID Code will be assigned at time of programming
Package:	T =	6-Pin SOT-23
	G =	6-Pin TDFN
Temperature:	C =	0°C to +70°C (Commercial)
	I =	–40°C to +85°C (Industrial)
Media Type:	none =	Bag
	TR =	Tape & Reel

Part Marking (Note 1)

TDFN Marking	SOT-23 Marking
XXX LLL	E1XXX LLL

Note 1: "XXX" designates a marking identifier that could be independent of the part number.

Examples:

a) PL610-01-XXXTC: 1.8V to 3.3V, 1 MHz to 130 MHz XO IC, ID Code, 6-Pin SOT-23, Commercial Temperature Range, Bag

b) PL610-01-XXXTC-TR: 1.8V to 3.3V, 1 MHz to 130 MHz XO IC, ID Code, 6-Pin SOT-23, Commercial Temperature Range, Tape & Reel

c) PL610-01-XXXTI: 1.8V to 3.3V, 1 MHz to 130 MHz XO IC, ID Code, 6-Pin SOT-23, Industrial Temperature Range, Bag

d) PL610-01-XXXTI-TR: 1.8V to 3.3V, 1 MHz to 130 MHz XO IC, ID Code, 6-Pin SOT-23, Industrial Temperature Range, Tape & Reel

e) PL610-01-XXXGC: 1.8V to 3.3V, 1 MHz to 130 MHz XO IC, ID Code, 6-Pin TDFN, Commercial Temperature Range, Bag

f) PL610-01-XXXGC-TR: 1.8V to 3.3V, 1 MHz to 130 MHz XO IC, ID Code, 6-Pin TDFN, Commercial Temperature Range, Tape & Reel

g) PL610-01-XXXGI: 1.8V to 3.3V, 1 MHz to 130 MHz XO IC, ID Code, 6-Pin TDFN, Industrial Temperature Range, Bag

h) PL610-01-XXXGI-TR: 1.8V to 3.3V, 1 MHz to 130 MHz XO IC, ID Code, 6-Pin TDFN, Industrial Temperature Range, Tape & Reel

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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China - Nanjing
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China - Xian
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China - Zhuhai
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India - Bangalore
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Fax: 91-80-3090-4123

India - New Delhi
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India - Pune
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Japan - Osaka
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Japan - Tokyo
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Fax: 81-3-6880-3771

Korea - Daegu
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Fax: 82-53-744-4302

Korea - Seoul
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Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
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Fax: 60-3-6201-9859

Malaysia - Penang
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Philippines - Manila
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Singapore
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Taiwan - Hsin Chu
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Taiwan - Kaohsiung
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Taiwan - Taipei
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