PL610-01/-02/-03

1.8V to 3.3V Single IC XO with Frequency Tuning (10 MHz to 130 MHz)

Features

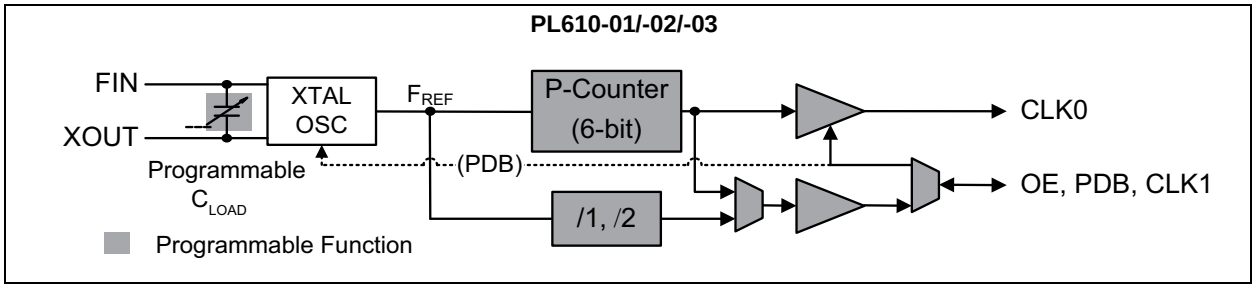
- Single Die, Wide Frequency Coverage, Programmable Advanced Oscillator Design
- Single IC to Cover up to 130 MHz Output Frequency.
- Direct Oscillation Operation with Optional Programmable Features:
  - ±50 ppm Frequency Tuning
  - Output Drive Setting (4 mA, 8 mA, or 16 mA)
  - 6-Bit Odd/Even Output Divider (≤ ÷63)
- Fundamental Crystal Input Frequency:
  - 10 MHz to 60 MHz (Default)
  - 60 MHz to 130 MHz (Programming Option)
- Output Frequency: LVCMOS
  - 80 kHz to 130 MHz
- Wire Bond and Flip Chip Options to Choose from
- Very Low Jitter and Phase Noise
- Low Current Consumption
- Single 1.8V, 2.5V, or 3.3V ±10% Power Supply
- Operating Temperature Range from –40°C to +85°C

General Description

The PL610 is a high performance general purpose clock that uses a single die to cover outputs up to 130 MHz, eliminating the need for multiple ICs to cover a wide frequency range. Designed to fit in a small 2.0 mm x 1.6 mm, or larger substrates, the PL610 offers the best phase noise and jitter performance, smallest die size, and lowest power consumption of any comparable IC.

The optional 'frequency fine tuning' feature of PL610 allows for frequency adjustment after encapsulation of the module, up to ±50 ppm. In addition, there is a '6' bit optional programmable Odd/Even divider (default = ÷1), and three programmable output drive strengths (4 mA, 8 mA (default), 16 mA) to choose from. The full feature set of PL610 makes it the most versatile XO for any application.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}) ..... –0.5V to +7.0V
Input Voltage (V_{IN})..... –0.5V to V_{DD} + 0.5V
Output Voltage (V_{OUT})..... –0.5V to V_{DD} + 0.5V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Parts are tested to commercial grade only.

TABLE 1-1: AC ELECTRICAL CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Crystal Input Frequency (XIN)	—	10	—	60	MHz	Fundamental Crystal, Low Frequency
		60	—	130		Fundamental Crystal, High Frequency
Output Frequency	—	.080	—	130	MHz	@ V_{DD} = 1.8V to 3.3V, ±10%
V_{DD} Sensitivity	—	–2	—	+2	ppm	Frequency vs. V_{DD}±10%
Output Rise Time (see Figure 3-1)	—	—	1	1.2	ns	15 pF Load, 10/90% V_{DD}, High Drive, 3.3V
Output Fall Time (see Figure 3-1)	—	—	1	1.2	ns	15 pF Load, 10/90% V_{DD}, High Drive, 3.3V
Duty Cycle (Note 1, see Figure 3-1)	—	45	50	55	%	—

Note 1: For 1.8V operation, the 50% ±5% duty cycle is guaranteed for frequencies ≤40 MHz.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current, Dynamic, with Loaded LVCMOS Output	I_{DD}	—	3.7	—	mA	V_{DD} = 3.3V, 40 MHz, Load = 15 pF
		—	2.75	—		V_{DD} = 2.5V, 40 MHz, Load = 15 pF
		—	2.0	—		V_{DD} = 1.8V, 40 MHz, Load = 15 pF
		—	2.5	—		V_{DD} = 3.3V, 26 MHz, Load = 15 pF
		—	1.8	—		V_{DD} = 2.5V, 26 MHz, Load = 15 pF
		—	1.3	—		V_{DD} = 1.8V, 26 MHz, Load = 15 pF
Supply Current, Dynamic, with Unloaded LVCMOS Output	—	—	1.65	—	mA	V_{DD} = 3.3V, 40 MHz, No Load
		—	1.2	—		V_{DD} = 2.5V, 40 MHz, No Load
		—	0.9	—		V_{DD} = 1.8V, 40 MHz, No Load
		—	1.2	—		V_{DD} = 3.3V, 26 MHz, No Load
		—	0.8	—		V_{DD} = 2.5V, 26 MHz, No Load
		—	0.58	—		V_{DD} = 1.8V, 26 MHz, No Load
Operating Voltage	V_{DD}	1.62	—	3.63	V	—
Power Supply Ramp	t_{PU}	0.001	—	100	ms	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.
Output Low Voltage	V_{OL}	—	—	0.1	V	I_{OL} = +4 mA Standard Drive
Output High Voltage	V_{OH}	V_{DD} – 0.4	—	—	V	I_{OH} = –4 mA Standard Drive

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Current, Low Drive (See Figure 3-2)	I_{OLD}	±4	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V
Output Current, Standard Drive (See Figure 3-2)	I_{OSD}	±8	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V
Output Current, High Drive (See Figure 3-2)	I_{OHD}	±16	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V

TABLE 1-3: CRYSTAL SPECIFICATIONS (10 MHZ TO 60 MHZ)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Fundamental Crystal Resonator Frequency	F_{XIN}	10	—	60	MHz	—
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L(XTAL)}$	8	—	12	pF	—
Maximum Sustainable Drive Level	—	—	—	100	µW	—
Operating Drive Level	—	—	25	—	µW	—
Crystal Shunt Capacitance	C0	—	—	3	pF	—
Effective Series Resistance, Fundamental, (See Figure 3-4)	ESR	—	—	50	Ω	—

TABLE 1-4: CRYSTAL SPECIFICATIONS (60 MHZ TO 130 MHZ)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Fundamental Crystal Resonator Frequency	F_{XIN}	60	—	130	MHz	—
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_{L(XTAL)}$	5	—	8	pF	—
Maximum Sustainable Drive Level	—	—	—	100	µW	—
Operating Drive Level	—	—	25	—	µW	—
Crystal Shunt Capacitance	C0	—	—	2.5	pF	—
Effective Series Resistance, Fundamental, (See Figure 3-4)	ESR	—	—	30	Ω	—

TABLE 1-5: PHASE NOISE SPECIFICATIONS (SEE MTC-3)

Parameters	Freq.	@1 Hz	@10 Hz	@100 Hz	@1 kHz	@10 kHz	@100 kHz	@1 MHz	Units
Phase noise relative to carrier (typ.)	40 MHz	–67	–98	–127	–142	–151	–155	–155	dBc/Hz
	26 MHz	–65	–96	–124	–145	–150	–155	–155	

TABLE 1-6: KEY PROGRAMMING PARAMETERS (OPTIONAL)

CLK[0:1] Output Frequency	Crystal Load	Output Drive Strength	Output Dividers
CLK0 = F_{REF}, F_{REF}/2 or F_{REF}/P Where P = 6-bit Optional: CLK1 = F_{REF}, F_{REF}/2 or CLK0	Optional 'Frequency Tuning' after encapsulation, up to: ±50 ppm Tuning Range Single-bit C_L adjustment for high/low frequency input	Three optional drive strengths to choose from: • Low: 4 mA • Std: 8 mA (default) • High: 16 mA	Optional 6-bit odd/even output divider: • ÷1 (default) to ÷63

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Ambient Operating Temperature	T_A	–40	—	+85	°C	—

Note 1: Exposure of the device under conditions beyond the limits specified by the maximum ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2.0 PAD DESCRIPTIONS

The descriptions of the pads are listed in Table 2-2.

Pad Configurations

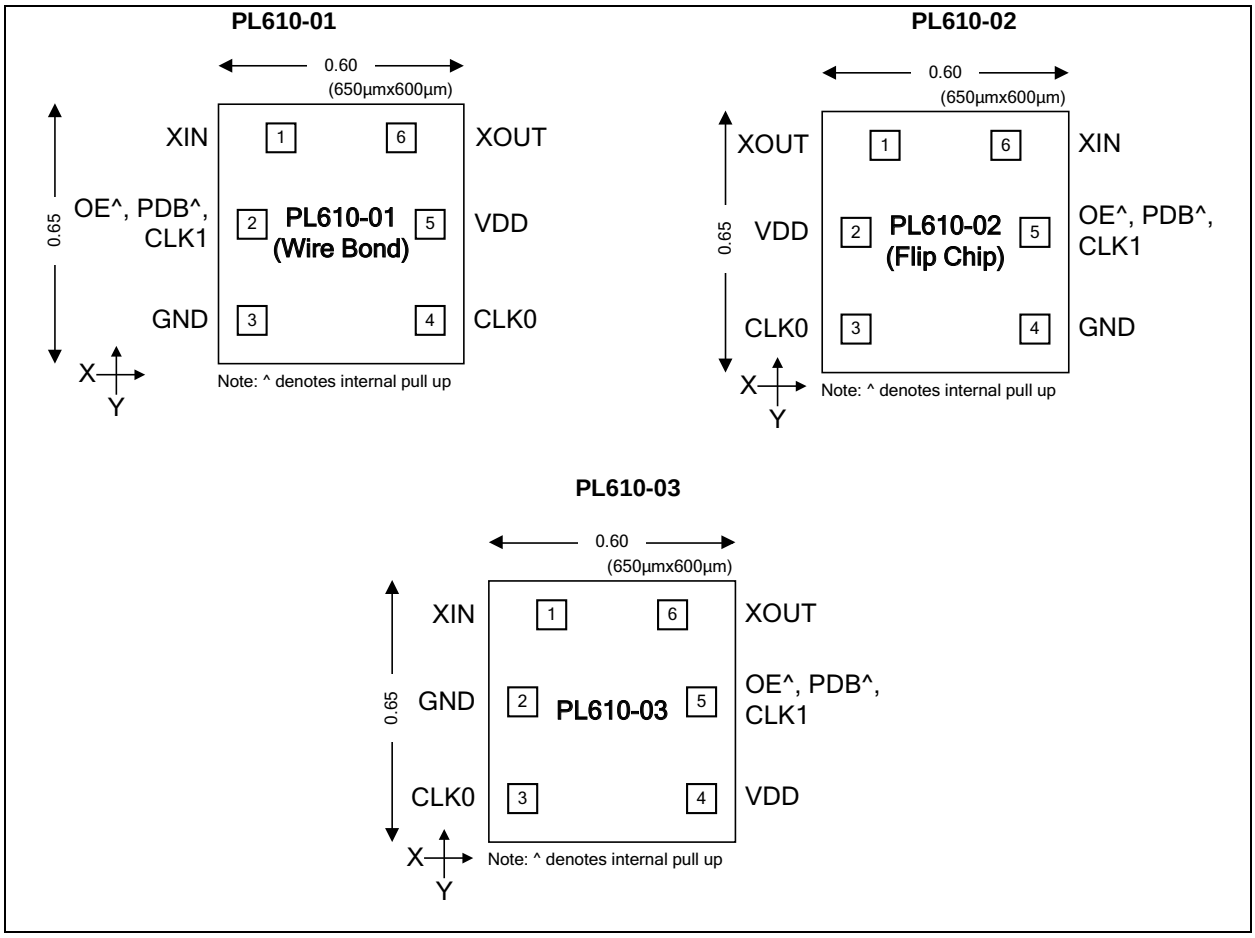


TABLE 2-1: DIE SPECIFICATION

Chip Size	Chip Thickness	Pad Size	Chip Base
0.65 mm x 0.60 mm	Optional	90 µm	GND Level

TABLE 2-2: PAD FUNCTION TABLE

Pad Number	Pad Center		Pad Name PL610-01	Pad Name PL610-02	Pad Name PL610-03
	X	Y			
1	–177	231	XIN	XOUT	XIN
2	–215	41	OE, PDB, CLK1	VDD	GND
3	–215	–186	GND	CLK0	CLK0
4	215	–186	CLK0	GND	VDD
5	215	41	VDD	OE, PDB, CLK1	OE, PDB, CLK1
6	177	213	XOUT	XIN	XOUT

TABLE 2-3: PAD FUNCTION DESCRIPTIONS

Pad Name	Description
CLK0	Programmable clock output
GND	GND connection
OE^, PDB^, CLK1	Programmable as: Output Enable (OE) – Enables/Disables CLK0 output buffer Power Down (PDB) – Enables/Disables CLK0 output buffer and crystal oscillator circuitry CLK1 – Second clock output
V_{DD}	V_{DD} connection
XIN	Crystal input pad
XOUT	Crystal output pad

3.0 MEASUREMENT TEST CIRCUITS (MTC)

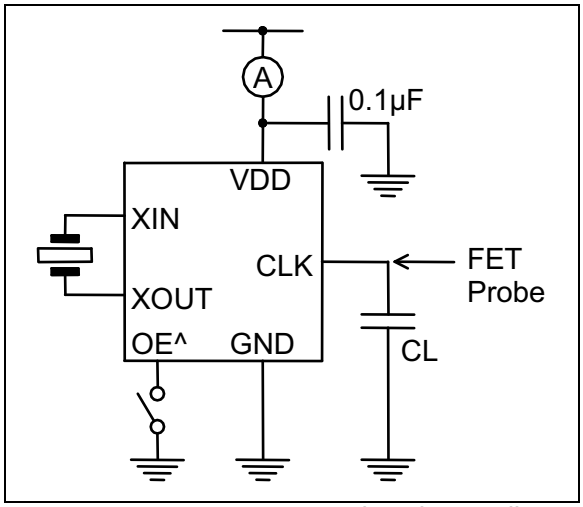


FIGURE 3-1: *MTC-1: Rise Time, Fall Time, Duty Cycle, V_{OL}, V_{OH}, I_{DD}, Power Down Current, Output Enable/Disable.*

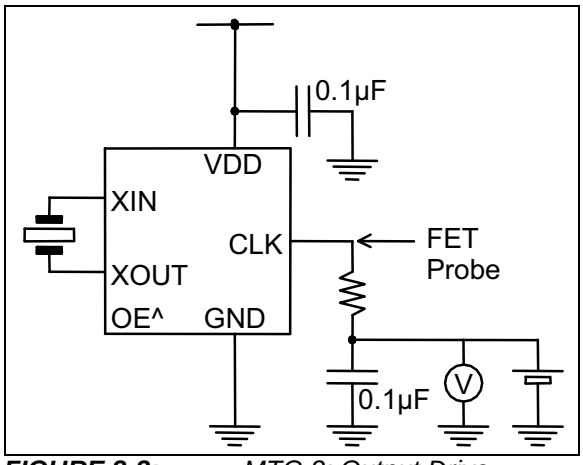


FIGURE 3-2: *MTC-2: Output Drive Current and Output Impedance.*

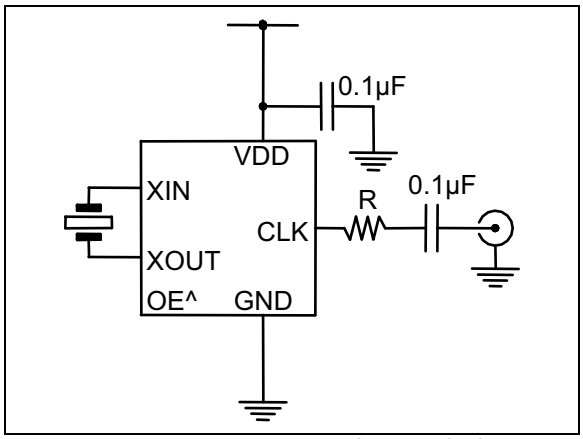


FIGURE 3-3: *MTC-3: Jitter and Phase Noise.*

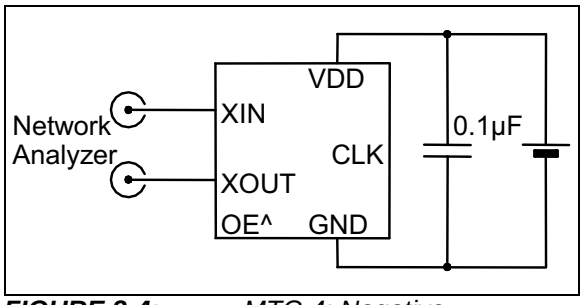


FIGURE 3-4: *MTC-4: Negative Resistance.*

4.0 WAVEFORM SWITCHING CHARACTERISTICS

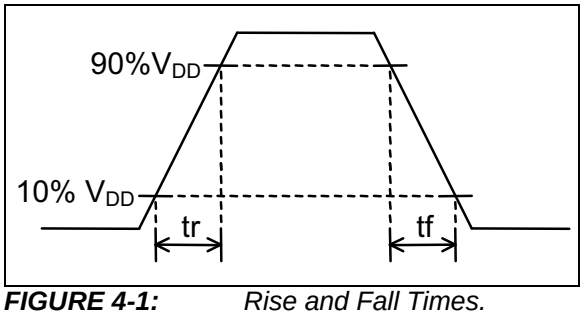


FIGURE 4-1: *Rise and Fall Times.*

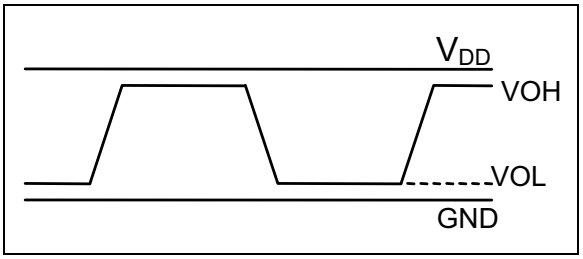


FIGURE 4-2: *V_{OH}, V_{OL}.*

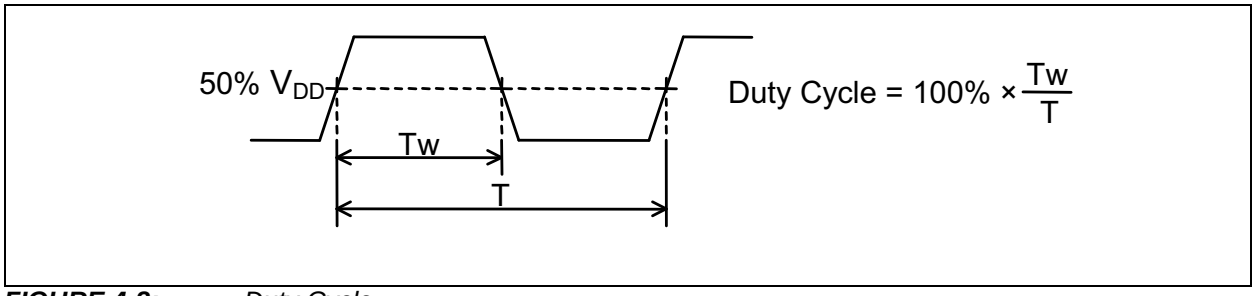


FIGURE 4-3: *Duty Cycle.*

APPENDIX A: REVISION HISTORY

Revision A (August 2016)

- Converted Micrel document PL610-01/-02/-03 to Microchip data sheet DS20005616A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X
Device	Package	Thickness	Temperature	Media Type

Device:	PL610-01:	1.8V to 3.3V Single IC XO with Frequency Tuning (10 MHz to 130 MHz)
	PL610-02:	1.8V to 3.3V Single IC XO with Frequency Tuning (10 MHz to 130 MHz)
	PL610-03:	1.8V to 3.3V Single IC XO with Frequency Tuning (10 MHz to 130 MHz)
Package:	D =	Die
	E =	Die (with non-conductive backcoating)
	V =	Wafer (with non-conductive backcoating)
	W =	Wafer
Thickness:	6 =	6 mm (Die Only)
	8 =	8 mm
	A =	10 mm
	none =	12 mm
Temperature:	C =	0°C to +70°C (Commercial)
Media Type:	none =	Tray

Examples:

a) PL610-01D6C: 1.8V to 3.3V Single IC XO with Frequency Tuning, Die, 6 mm Thickness, Commercial Temp. Range, Tray

b) PL610-02E8C: 1.8V to 3.3V Single IC XO with Frequency Tuning, Die (non-conductive back), 8 mm Thickness, Commercial Temp. Range, Tray

c) PL610-03VAC: 1.8V to 3.3V Single IC XO with Frequency Tuning, Wafer (non-conductive back), 10 mm Thickness, Commercial Temp. Range, Tray

d) PL610-01WC: 1.8V to 3.3V Single IC XO with Frequency Tuning, Wafer, 12 mm Thickness, Commercial Temp. Range, Tray

e) PL610-02W8C: 1.8V to 3.3V Single IC XO with Frequency Tuning, Wafer, 8 mm Thickness, Commercial Temp. Range, Tray

f) PL610-03DAC: 1.8V to 3.3V Single IC XO with Frequency Tuning, Die, 10 mm Thickness, Commercial Temp. Range, Tray

g) PL610-02E6C: 1.8V to 3.3V Single IC XO with Frequency Tuning, Die (non-conductive back), 6 mm Thickness, Commercial Temp. Range, Tray

h) PL610-01VC: 1.8V to 3.3V Single IC XO with Frequency Tuning, Wafer (non-conductive back), 12 mm Thickness, Commercial Temp. Range, Tray

NOTES:

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