Obsolete Device

37LV36/65/128

36K, 64K, and 128K Serial EPROM Family

FEATURES

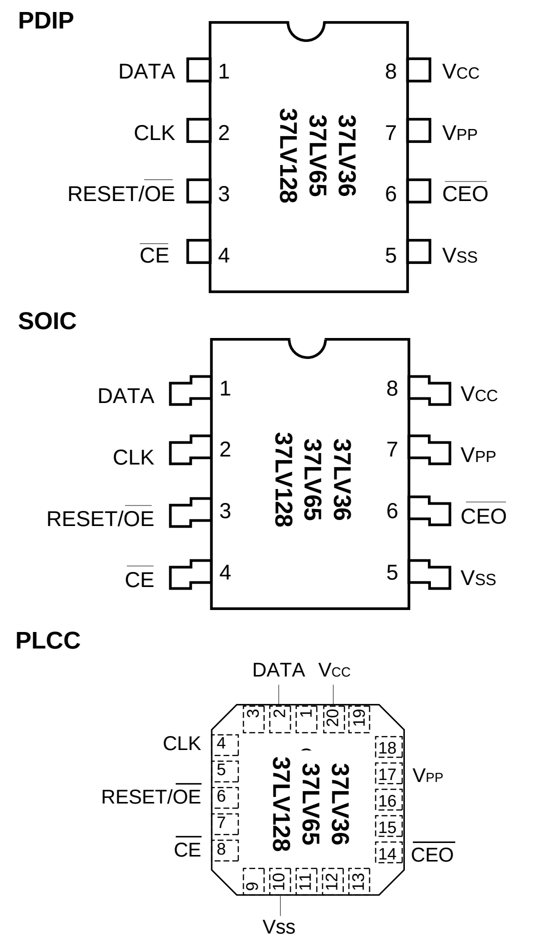
- Operationally equivalent to Xilinx® XC1700 family
- Wide voltage range 3.0 V to 6.0 V
- Maximum read current 10 mA at 5.0 V
- Standby current 100 µA typical
- Industry standard Synchronous Serial Interface/ 1 bit per rising edge of clock
- Full Static Operation
- Sequential Read/Program
- Cascadable Output Enable
- 10 MHz Maximum Clock Rate @ 5.0 Vdc
- Programmable Polarity on Hardware Reset
- Programming with industry standard EPROM programmers
- Electrostatic discharge protection > 4,000 volts
- 8-pin PDIP/SOIC and 20-pin PLCC packages
- Data Retention > 200 years
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

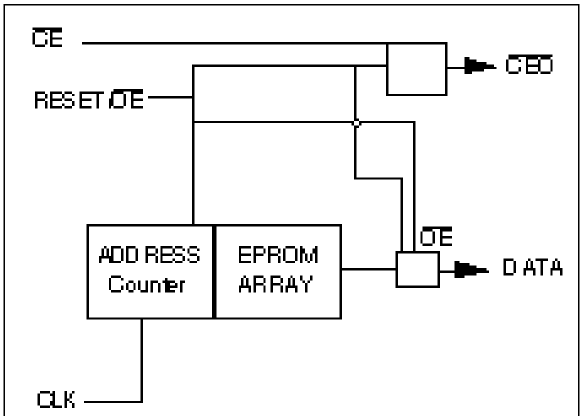
The Microchip Technology Inc. 37LV36/65/128 is a family of Serial OTP EPROM devices organized internally in a x32 configuration. The family also features a cascadable option for increased memory storage where needed. The 37LV36/65/128 is suitable for many applications in which look-up table information storage is desirable and provides full static operation in the 3.0V to 6.0V VCC range. The devices also support the industry standard serial interface to the popular RAM-based Field Programmable Gate Arrays (FPGA). Advanced CMOS technology makes this an ideal bootstrap solution for today's high speed SRAM-based FPGAs. The 37LV36/65/128 family is available in the standard 8-pin plastic DIP, 8-pin SOIC and 20-pin PLCC packages.

Device	Bits	Programming Word
37LV36	36,288	1134 x 32
37LV65	65,536	2048 x 32
37LV128	131,072	4096 x 32

PACKAGE TYPES



BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS .... -0.6V to +0.6V

VPP voltage w.r.t. VSS during programming .... -0.6V to +14.0V

Output voltage w.r.t. VSS ....-0.6V to VCC +0.6V

Storage temperature ....-65°C to +150°C

Ambient temp. with power applied .....-65°C to +125°C

Soldering temperature of leads (10 sec.) .... +300°C

ESD protection on all pins .... ≥ 4 kV

*Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function	8	20
DATA	Data I/O	1	2
CLK	Clock Input	2	4
RESET/$\overline{\text{OE}}$	Reset Input and Output Enable	3	6
$\overline{\text{CE}}$	Chip Enable Input	4	8
VSS	Ground	5	10
$\overline{\text{CEO}}$	Chip Enable Output	6	14
VPP	Programming Voltage Supply	7	17
VCC	+3.0V to 6.0V Power Supply	8	20
Not Labeled	Not utilized, not connected		

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +3.0 to 6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
DATA, $\overline{\text{CE}}$, $\overline{\text{CEO}}$ and Reset pins:					
High level input voltage	VIH	2.0	VCC	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH1	3.86		V	IOH = -4 mA VCC ≥ 4.5V
	VOH2	2.4			IOH = -4 mA VCC ≥ 3.0V
Low level output voltage	VOL	—	.32	V	IOL = 4.0 mA
Input Leakage	ILI	-10	10	µA	VIN = .1V to VCC
Output Leakage	ILO	-10	10	µA	VOUT = .1V to VCC
Input Capacitance (all inputs/outputs)	CINT	—	10	pF	Tamb = 25°C; FCLK = 1 MHz (Note 1)
Operating Current	ICC Read	— —	10 2	mA mA	VCC = 6.0V, CLK = 10 MHz VCC = 3.6V, CLK = 2.5 MHz Outputs open
Standby Current	ICCS	—	100 50	µA µA	VCC = 6.0V, CE = 5.8V VCC = 3.6V, CE = 3.4V

Note 1: This parameter is initially characterized and not 100% tested.

2.0 DATA

2.1 Data I/O

Three-state DATA output for reading and input during programming.

3.0 CLK

3.1 Clock Input

Used to increment the internal address and bit counters for reading and programming.

4.0 RESET/$\overline{\text{OE}}$

4.1 Reset Input and Output Enable

A LOW level on both the $\overline{\text{CE}}$ and RESET/$\overline{\text{OE}}$ inputs enables the data output driver. A HIGH level on RESET/$\overline{\text{OE}}$ resets both the address and bit counters. In the 37LVXXX, the logic polarity of this input is programmable as either RESET/$\overline{\text{OE}}$ or OE/$\overline{\text{RESET}}$. This document describes the pin as RESET/$\overline{\text{OE}}$ although the opposite polarity is also possible. This option is defined and set at device program time.

5.0 $\overline{\text{CE}}$

5.1 Chip Enable Input

$\overline{\text{CE}}$ is used for device selection. A LOW level on both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ enables the data output driver. A HIGH level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low power mode.

6.0 $\overline{\text{CEO}}$

6.1 Chip Enable Output

This signal is asserted LOW on the clock cycle following the last bit read from the memory. It will stay LOW as long as $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are both LOW. It will then follow $\overline{\text{CE}}$ until $\overline{\text{OE}}$ goes HIGH. Thereafter, $\overline{\text{CEO}}$ will stay HIGH until the entire EPROM is read again. This pin also used to sense the status of RESET polarity when Programming Mode is entered.

7.0 VPP

7.1 Programming Voltage Supply

Used to enter programming mode (+13 volts) and to program the memory (+13 volts). Must be connected directly to Vcc for normal Read operation. No overshoot above +14 volts is permitted.

8.0 CASCADING SERIAL EPROMS

Cascading Serial EPROMs provide additional memory for multiple FPGAs configured as a daisy-chain, or for future applications requiring larger configuration memories.

When the last bit from the first Serial EPROM is read, the next clock signal to the Serial EPROM asserts its $\overline{\text{CEO}}$ output LOW and disables its DATA line. The second Serial EPROM recognizes the LOW level on its $\overline{\text{CE}}$ input and enables its DATA output.

When configuration is complete, the address counters of all cascaded Serial EPROMs are reset if RESET goes LOW forcing the RESET/$\overline{\text{OE}}$ on each Serial EPROM to go HIGH. If the address counters are not to be reset upon completion, then the RESET/$\overline{\text{OE}}$ inputs can be tied to ground.

Additional logic may be required if cascaded memories are so large that the rippled chip enable is not fast enough to activate successive Serial EPROMs.

9.0 STANDBY MODE

The 37LVXXX enters a low-power Standby Mode whenever $\overline{\text{CE}}$ is HIGH. In Standby Mode, the Serial EPROM consumes less than 100 μA of current. The output will remain in a high-impedance state regardless of the state of the $\overline{\text{OE}}$ input.

10.0 PROGRAMMING MODE

Programming Mode is entered by holding V_{PP} HIGH (+13 volts) for two clock edges and then holding $V_{PP} = V_{DD}$ for one clock edge. Programming mode is exited by driving a LOW on both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ and then removing power from the device. Figures 4 through 7 show the programming algorithm.

11.0 37LVXXX RESET POLARITY

The 37LVXXX lets the user choose the reset polarity as either RESET/$\overline{\text{OE}}$ or $\overline{\text{OE}}$/RESET. Any third-party commercial programmer should prompt the user for the desired reset polarity.

The programming of the overflow word should be handled transparently by the EPROM programmer; it is mentioned here as supplemental information only.

The polarity is programmed into the first overflow word location, maximum address+1. 00000000 in these locations makes the reset active LOW, FFFFFFFF in these locations makes the reset active HIGH. The default condition is RESET active HIGH.

FIGURE 11-1: READ CHARACTERISTICS TIMING

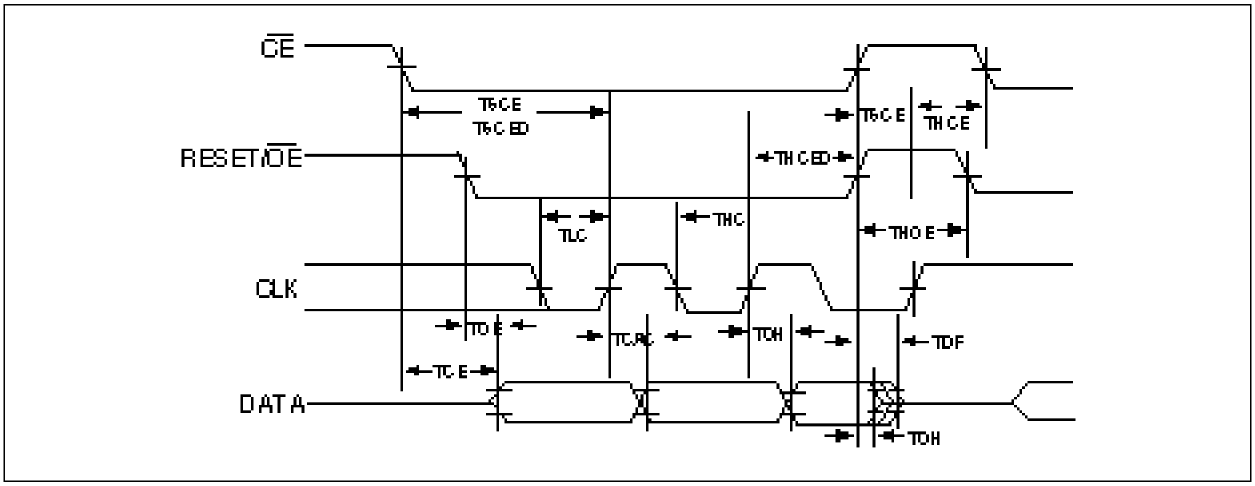


TABLE 11-1: READ CHARACTERISTICS

AC Testing Waveform: VIL = 0.2V; VIH = 3.0V
AC Test Load: 50 pF
VOL = VOL_MAX; VOH = VOH_MIN

Symbol	Parameter	Limits 3.0V ≤ Vcc ≤ 6.0V		Limits 4.5V ≤ Vcc ≤ 6.0V		Units	Conditions
		Min.	Max.	Min.	Max.		
TOE	$\overline{\text{OE}}$ to Data Delay	—	45	—	45	ns	
TCE	$\overline{\text{CE}}$ to Data Delay	—	60	—	50	ns	
TCAC	CLK to Data Delay	—	200	—	60	ns	
TOH	Data Hold from $\overline{\text{CE}}$, $\overline{\text{OE}}$ or CLK	0	—	0	—	ns	
TDF	$\overline{\text{CE}}$ or $\overline{\text{OE}}$ to Data Float Delay	—	50	—	50	ns	Notes 1, 2
TLC	CLK Low Time	100	—	25	—	ns	
THC	CLK High Time	100	—	25	—	ns	
TSCE	$\overline{\text{CE}}$ Set up Time to CLK (to guarantee proper counting)	40	—	25	—	ns	Note 1
TSCED	$\overline{\text{CE}}$ setup time to CLK (to guarantee proper DATA read)	100	—	80	—	ns	
THCE	$\overline{\text{CE}}$ Hold Time to CLK (to guarantee proper counting)	0	—	0	—	ns	Note 1
THCED	$\overline{\text{CE}}$ hold time to CLK (to guarantee proper DATA read)	50	—	0	—	ns	
THOE	$\overline{\text{OE}}$ High Time (Guarantees counters are Reset)	100		20	—	ns	
CLK max	Clock Frequency	—	2.5	—	10	MHz	

Note 1: This parameter is periodically sampled and not 100% tested.
2: Float delays are measured with output pulled through 1kΩ to VLOAD = VCC/2.

FIGURE 11-2: READ CHARACTERISTICS AT END OF ARRAY TIMING

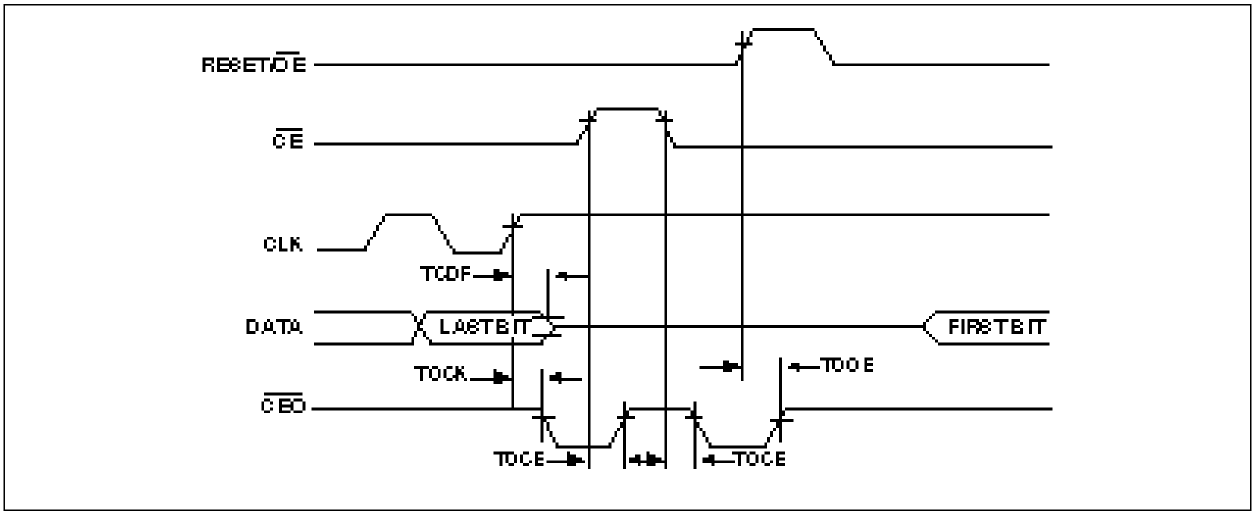


TABLE 11-2: READ CHARACTERISTICS AT END OF ARRAY

AC Testing Waveform: V_{IL} = 0.2V; V_{IH} = 3.0V
AC Test Load: 50 pF
$V_{OL} = V_{OL\_MAX}$; $V_{OH} = V_{OH\_MIN}$

Symbol	Parameter	Limits 3.0V ≤ Vcc ≤ 6.0V		Limits 4.5V ≤ Vcc ≤ 6.0V		Units	Conditions
		Min.	Max.	Min.	Max.		
T_{CDF}	CLK to Data Float Delay	—	50	—	50	ns	Notes 1, 2
T_{OCK}	CLK to $\overline{CEO}$ Delay	—	65	—	40	ns	
T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ Delay	—	45	—	40	ns	
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay	—	45	—	40	ns	

Note 1: This parameter is periodically sampled and not 100% tested.
2: Float delays are measured with output pulled through 1kΩ to $V_{LOAD} = V_{CC}/2$.

TABLE 11-3: PIN ASSIGNMENTS IN THE PROGRAMMING MODE

DIP/SOIC Pin	PLCC Pin	Name	I/O	Description
1	2	DATA	I/O	The rising edge of the clock shifts a data word in or out of the EPROM one bit at a time.
2	4	CLK	I	Clock Input. Used to increment the internal address/word counter for reading and programming operation.
3	6	RESET/$\overline{OE}$	I	The rising edge of CLK shifts a data word into the EPROM when $\overline{CE}$ and $\overline{OE}$ are HIGH; it shifts a data word out of the EPROM when $\overline{CE}$ is LOW and $\overline{OE}$ is HIGH. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held HIGH and $\overline{OE}$ is held LOW. Note 1: Any modified polarity of the RESET/$\overline{OE}$ pin is ignored in the programming mode.
4	8	$\overline{CE}$	I	The rising edge of CLK shifts a data word into the EPROM when $\overline{CE}$ and $\overline{OE}$ are HIGH; it shifts a data word out of the EPROM when $\overline{CE}$ is LOW and $\overline{OE}$ is HIGH. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held HIGH and $\overline{OE}$ is held LOW.
5	10	V_{SS}		Ground pin.
6	14	$\overline{CEO}$	O	The polarity of the RESET/$\overline{OE}$ pin can be read by sensing the $\overline{CEO}$ pin. Note 1: The polarity of the RESET/$\overline{OE}$ pin is ignored while in the Programming Mode. In final verification, this pin must be monitored to go LOW one clock cycle after the last data bit has been read.
7	17	V_{PP}		Programming Voltage Supply. Programming Mode is entered by holding $\overline{CE}$ and $\overline{OE}$ HIGH and V_{PP} at $V_{PP}1$ for two rising clock edges and then lowering V_{PP} to $V_{PP}2$ for one more rising clock edge. A word is programmed by strobing the device with V_{PP} for the duration TPGM. V_{PP} must be tied to V_{CC} for normal read operation.
8	20	V_{CC}		+5 V power supply input.

TABLE 11-4: DC PROGRAMMING SPECIFICATIONS

Symbol	Parameter Ambient Temperature: Tamb = 25°C ±5°C	Limits		Units
		Min.	Max.	
V_{CCP}	Supply voltage during programming	5.0	6.0	V
V_{IL}	Low-level input voltage	0.0	0.5	V
V_{IH}	High-level input voltage	2.4	V_{CC}	V
V_{OL}	Low-level output voltage	—	0.4	V
V_{OH}	High-level output voltage	3.7	—	V
$V_{PP}1$	Programming voltage*	12.5	13.5	V
$V_{PP}2$	Programming Mode access voltage	V_{CCP}	V_{CCP}+1	V
I_{PPP}	Supply current in Programming Mode	—	100	mA
I_L	Input or output leakage current	-10	10	µA
V_{CCL}	First pass Low-level supply voltage for final verification	2.8	3.0	V
V_{CCH}	Second pass High-level supply voltage for final verification	6.4	6.6	V

* No overshoot is permitted on this signal. VPP must not be allowed to exceed 14 volts.

TABLE 11-5: AC PROGRAMMING SPECIFICATIONS (SEE NOTE 2)

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
T_{RPP}	10% to 90% Rise Time of V_{PP}	1		µs	Note 1
T_{FPP}	90% to 10% Fall Time of V_{PP}	1		µs	Note 1
T_{PGM}	V_{PP} Programming Pulse Width	.50	1.05	ms	
T_{SVC}	V_{PP} Setup to CLK for Entering Programming Mode	100		ns	Note 1
T_{SVCE}	$\overline{CE}$ Setup to CLK for Entering Programming Mode	100		ns	Note 1
T_{SVOE}	$\overline{OE}$ Setup to CLK for Entering Programming Mode	100		ns	Note 1
T_{HVC}	V_{PP} Hold from CLK for Entering Programming Mode	300		ns	Note 1
T_{SDP}	Data Setup to CLK for Programming	50		ns	
T_{HDP}	Data Hold from CLK for Programming	0		ns	
T_{LCE}	$\overline{CE}$ Low time to clear data latches	100		ns	
T_{SCC}	$\overline{CE}$ Setup to CLK for Programming/Verifying	100		ns	
T_{SIC}	$\overline{OE}$ Setup to CLK for Incrementing Address Counter	100		ns	
T_{HIC}	$\overline{OE}$ Hold from CLK for Incrementing Address Counter	0		ns	
T_{HOV}	$\overline{OE}$ Hold from V_{PP}	200		ns	Note 1
T_{PCAC}	CLK to Data Valid		400	ns	
T_{POH}	Data Hold from CLK	0		ns	
T_{PCE}	$\overline{CE}$ Low to Data Valid		250	ns	

Note 1: This parameter is periodically sampled and not 100% tested.

Note 2: While in Programming Mode, $\overline{CE}$ should only be changed while $\overline{OE}$ is HIGH and has been HIGH for 200 ns, and $\overline{OE}$ should only be changed while $\overline{CE}$ is HIGH and has been HIGH for 200 ns.

FIGURE 11-3: ENTER AND EXIT PROGRAMMING MODES

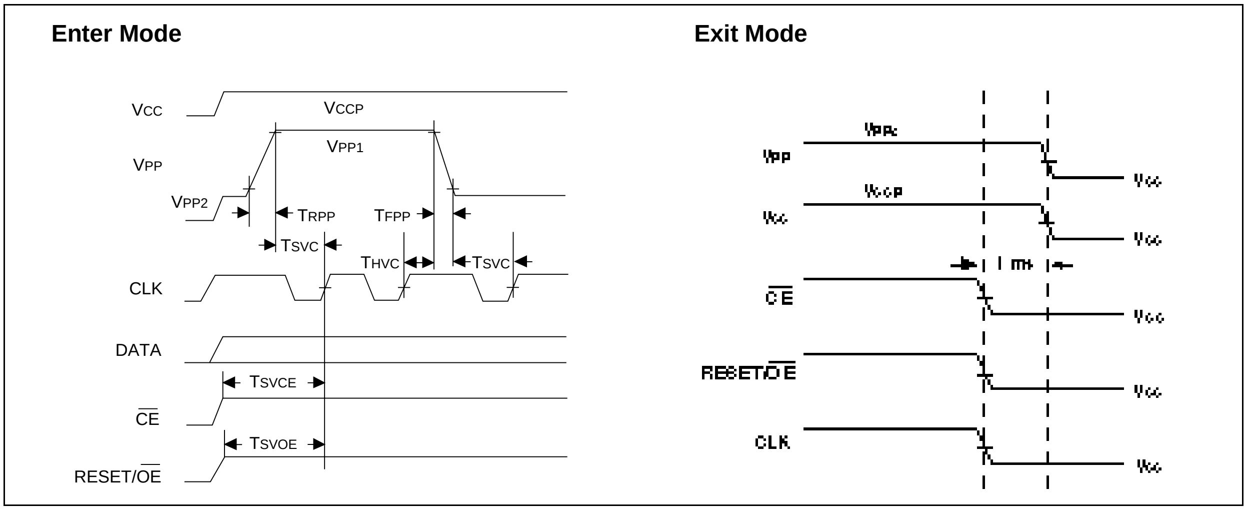


FIGURE 11-4: PROGRAMMING CYCLE OVERVIEW (NO VERIFY UNTIL ENTIRE ARRAY IS PROGRAMMED)

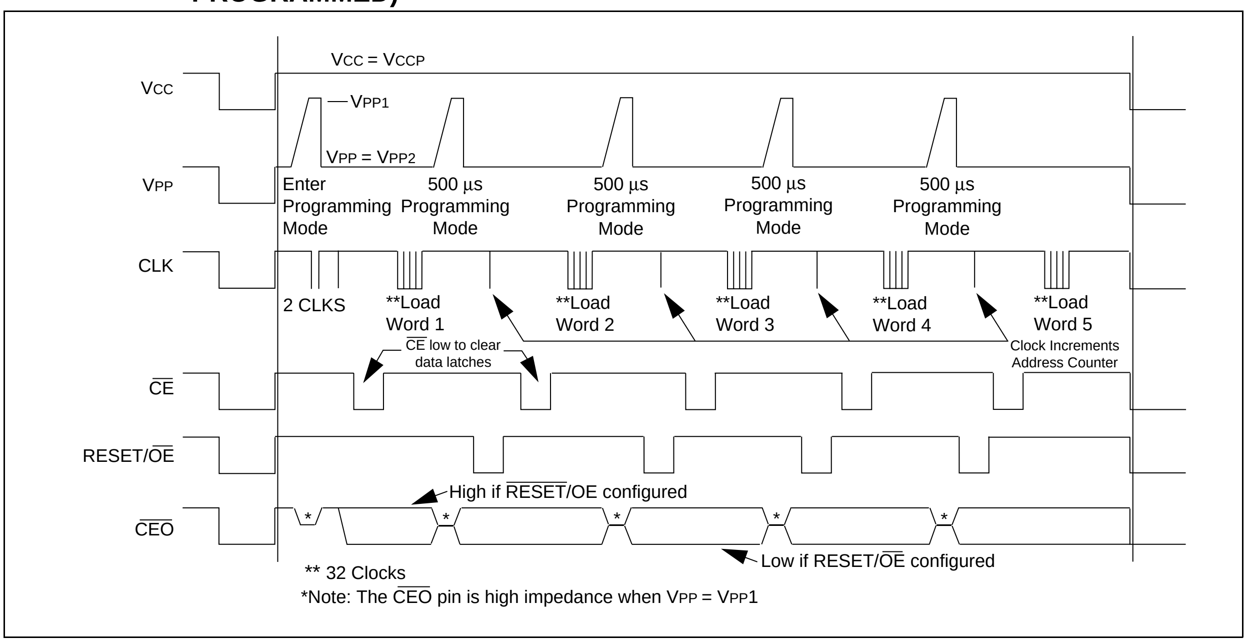


FIGURE 11-5: DETAILS OF PROGRAM CYCLE

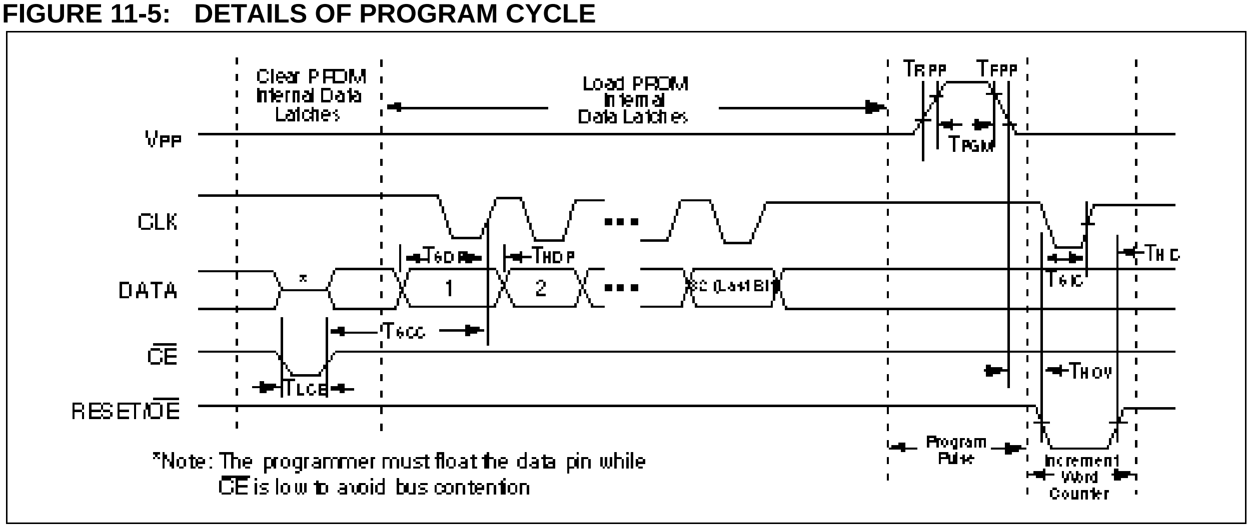


FIGURE 11-6: READ MANUFACTURER AND DEVICE ID OVERVIEW

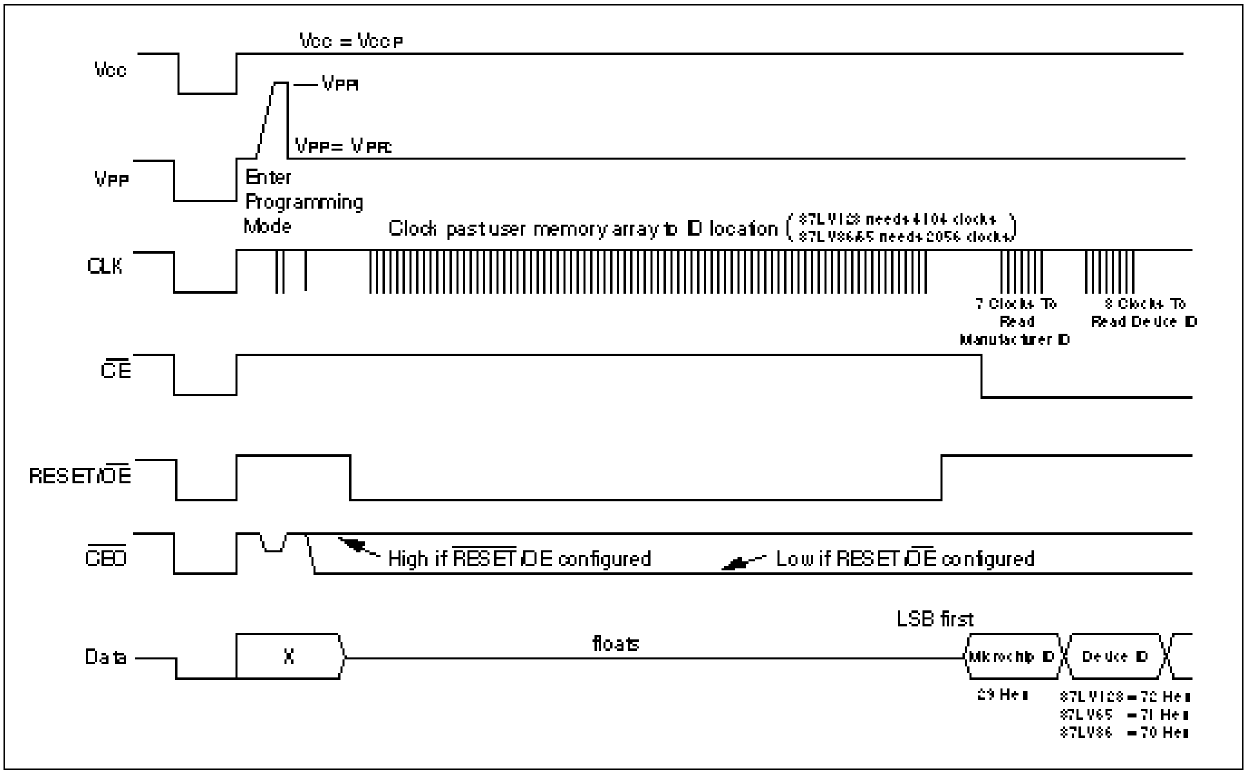


FIGURE 11-7: DETAILS OF READ MANUFACTURER AND DEVICE ID

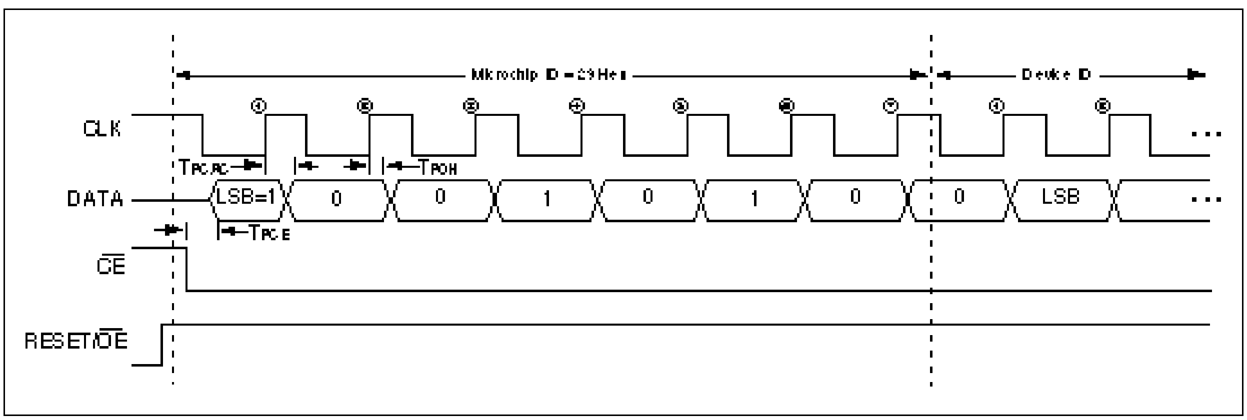
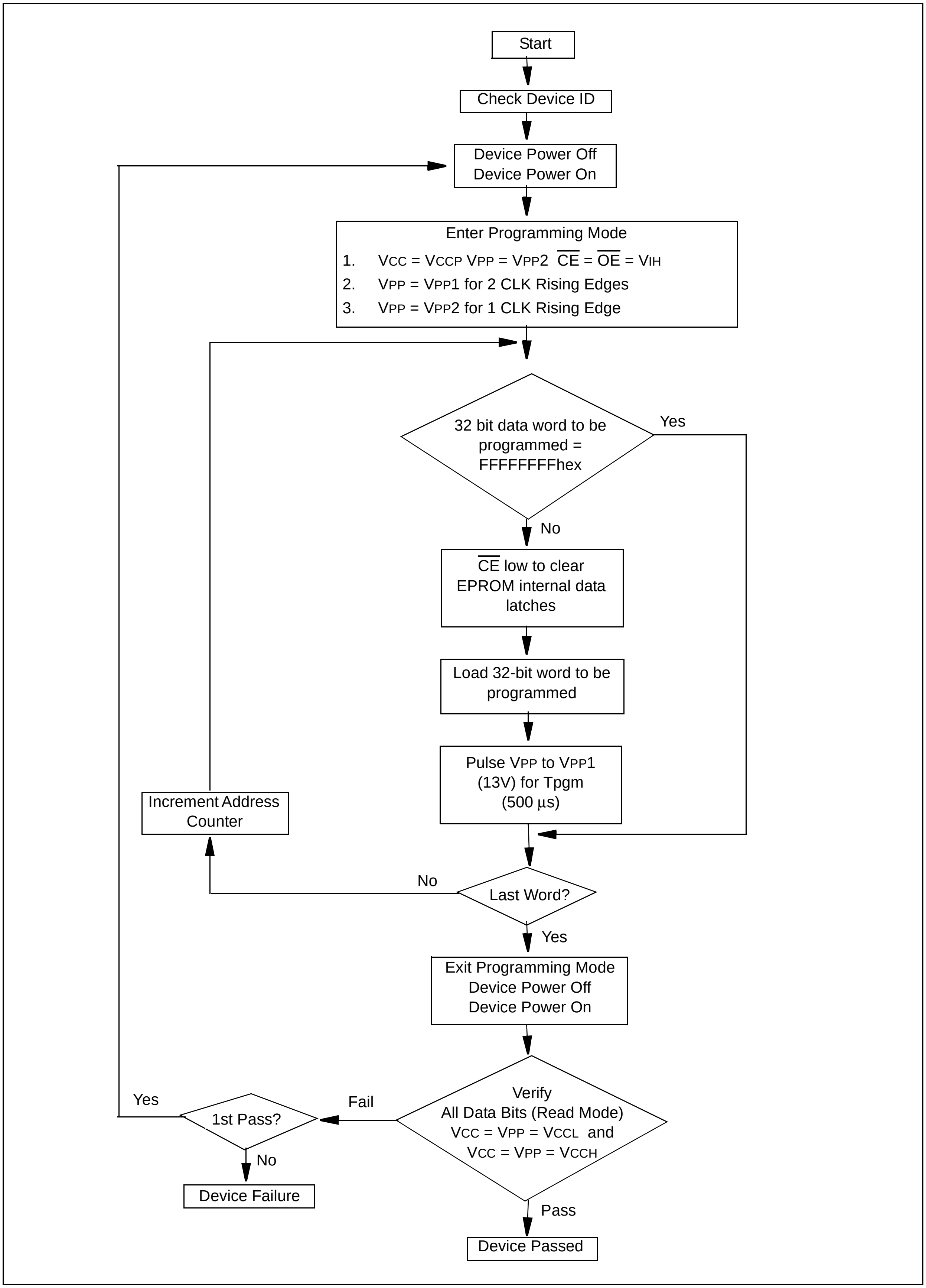


FIGURE 11-8: 37LVXXX PROGRAMMING SPECIFICATIONS



37LV36/65/128 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

37LV36/65/128 – I T /P

Package:	P =	Plastic DIP, 8 lead
	SN =	Plastic SOIC (150 mil Body), 8 lead
	L =	Plastic Leaded Chip Carrier (PLCC), 20 lead
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Shipping:	Blank =	Tube
	T =	Tape and Reel
Device:	37LV128	128K Serial EPROM
	37LV65	64K Serial EPROM
	37LV36	36K Serial EPROM

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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ISO/TS 16949:2002

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