Obsolete Device

24LC09

8K 2.5V ACR Serial EEPROM

Features

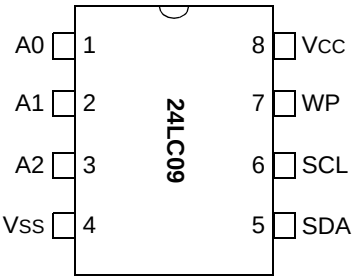
- Supports ACR riser card specification
  - 2-wire ACR serial bus interface
  - Address: 1011
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 500 nA standby current typical at 5V
- Organized as four blocks of 256 bytes (4 x 256 x 8)
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 400 kHz Capability (2.5 to 5.5 Volts)
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP, 8-lead SOIC packages
- Available temperature ranges:
  - Industrial (I): -40°C to +85°C

Description

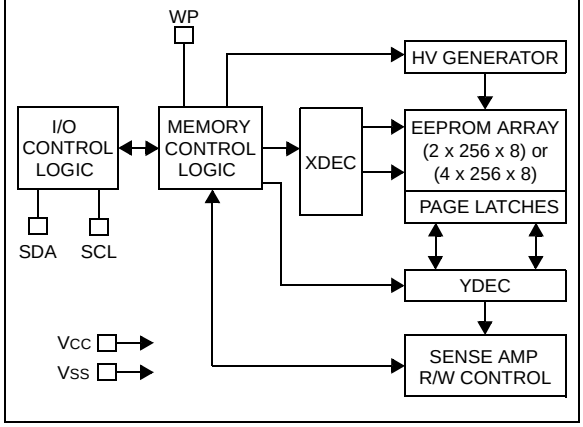
The Microchip Technology Inc. 24LC09 is an 8 Kbit Electrically Erasable PROM (EEPROM) designed to meet the Advanced Communication Riser Special Interest Group (ACR-SIG). The device is organized as four blocks of 256 x 8-bit memory that supports the 2-wire serial interface with a special address: 1011. Low voltage design permits operation down to 2.5 volts with typical standby and active currents of only 5 µA and 1 mA, respectively. The 24LC09 also has a page-write capability for up to 16 bytes of data. The 24LC09 is available in the standard 8-pin DIP, 8-lead surface mount SOIC packages.

Package Types

PDIP/SOIC



Block Diagram



I^2C is a registered trademark of Philips Corporation.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

VCC.....7.0V

All inputs and outputs, w.r.t. VSS ..... -0.3V to VCC + 1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-65°C to +125°C

Soldering temperature of leads (10 seconds) .....+300°C

ESD protection on all pins .....≥ 4 kV

†Notice: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 DC Characteristics

DS Characteristics			Industrial (I): TAMB = -40°C to +85°C			
Param. No.	**Sym**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D1	VIH	High level input voltage	.7 VCC	—	V	
D2	VIL	Low level input voltage	—	.3 VCC	V	
D3	VHYS	Hysteresis of Schmitt trigger Inputs	.05 VCC	—	V	(**Note**)
D4	VOL	Low level output voltage	—	.40	V	IOL = 3.0 mA, VCC = 2.5V
D5	ILI	Input leakage current	-10	10	µA	VIN = 0.1V to VCC
D6	ILO	Output leakage current	-10	10	µA	VOUT = 0.1V to VCC
D7	CIN, COUT	Pin capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V, TAMB = 25°C, FCLK = 1 MHz (**Note**)
D8	ICC WRITE	Operating current	—	3	mA	VCC = 5.5V,
D9	ICC READ		—	1	mA	SCL = 400 kHz
D10	ICCS	Standby current	— —	1 1	µA µA	VCC = 3.0V, SDA = SCL = VCC VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

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1.2 AC Characteristics

AC Characteristics			Industrial (I): T_{AMB} = -40°C to +85°C			
Param. No.	**Sym**	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
1	F_{CLK}	Clock frequency	— —	400 100	kHz	4.5V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V
2	T_{HIGH}	Clock high time	600	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
3	T_{LOW}	Clock low time	1300	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
4	T_R	SDA and SCL rise time	—	300	ns	2.5V ≤ V_{CC} ≤ 5.5V (**Note 1**)
5	T_F	SDA and SCL fall time	—	300	ns	(**Note 1**)
6	$T_{HD:STA}$	START condition hold time	600	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
7	$T_{SU:STA}$	START condition setup time	600	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
8	$T_{HD:DAT}$	Data input hold time	0	—	ns	(**Note 2**)
9	$T_{SU:DAT}$	Data input setup time	100	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
10	$T_{SU:STO}$	STOP condition setup time	600	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
11	T_{AA}	Output valid from clock (Note 2)	—	900	ns	2.5V ≤ V_{CC} ≤ 5.5V
12	T_{BUF}	Bus free time: Time the bus must be free before a new transmission can start	1300	—	ns	2.5V ≤ V_{CC} ≤ 5.5V
13	T_{OF}	Output fall time from V_{IH} minimum to V_{IL} maximum	20+0.1C_B	250	ns	2.5V ≤ V_{CC} ≤ 5.5V (**Note 1**)
14	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	50	ns	(**Notes 1 and 3**)
15	T_{WC}	Write cycle time (byte or page)	—	5	ms	
16		Endurance	1M	—	cycles	25°C, V_{CC} = 5.0V, Block Mode (**Note 4**)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website.

FIGURE 1-1: BUS TIMING START/STOP

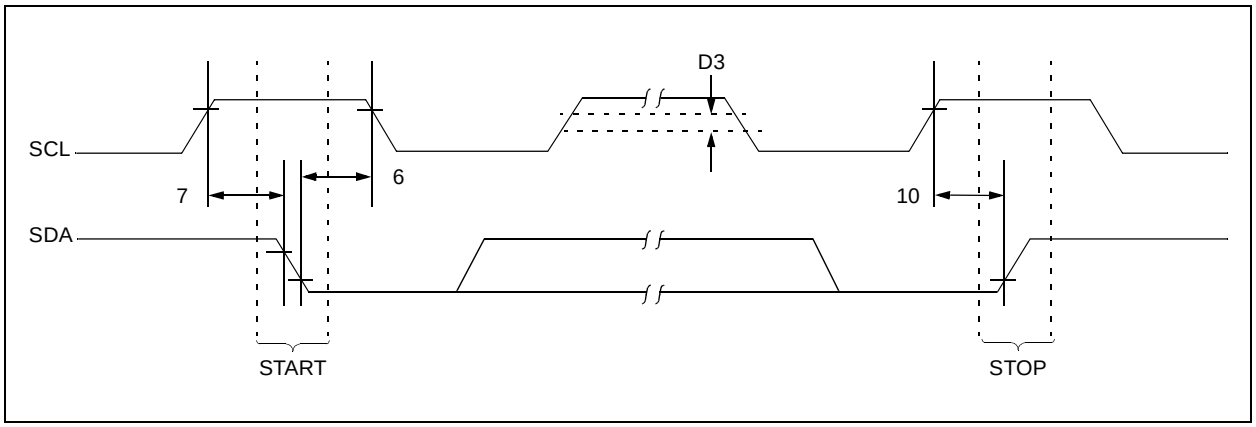
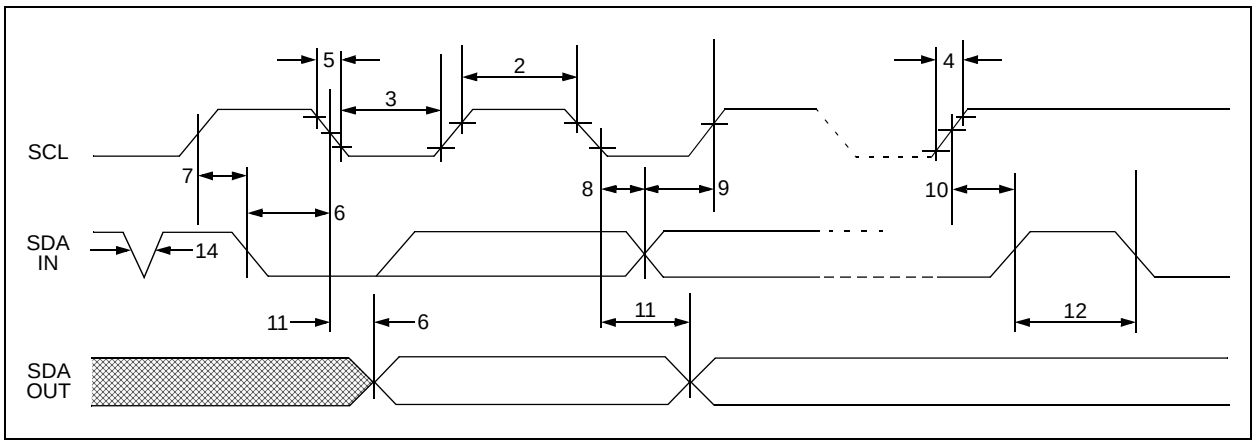


FIGURE 1-2: BUS TIMING DATA



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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	No Internal Connection

2.1 Serial Address/Data Input/Output (SDA)

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

2.3 Write Protect (WP)

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC09 as a serial ROM when WP is enabled (tied to VCC).

2.4 A0, A1, A2

These pins are not used by the 24LC09. They may be left floating or tied to either VSS or VCC.

3.0 FUNCTIONAL DESCRIPTION

The 24LC09 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the Start and Stop conditions, while the 24LC09 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a start or stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

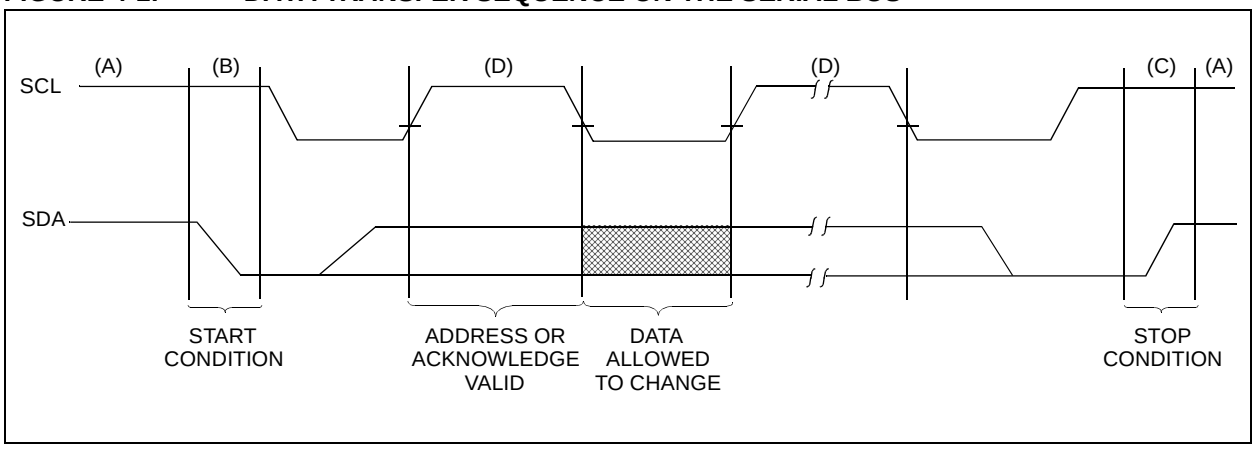
4.1 Bus not Busy (A)

Both data and clock lines remain High.

4.2 Start Data Transfer (B)

A High to Low transition of the SDA line while the clock (SCL) is high determines a start condition. All commands must be preceded by a start condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.3 Stop Data Transfer (C)

A low to high transition of the SDA line while the clock (SCL) is high determines a stop condition. All operations must be ended with a stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of the data bytes transferred between the start and stop conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC09 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the stop condition.

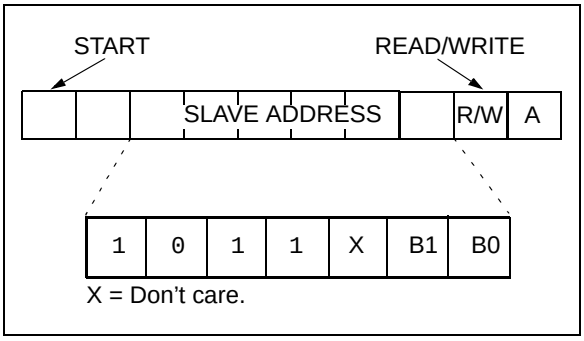
4.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code, for the 24LC09 this is set as 1011 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). B2 is a don't care for the 24LC09. They are used by the master device to select which of the four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC09 monitors the SDA bus checking the device type identifier being transmitted, upon a 1011 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC09 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1011	Block Address	1
Write	1011	Block Address	0

FIGURE 4-2: CONTROL BYTE ALLOCATION



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5.0 WRITE OPERATION

5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC09. After receiving another acknowledge signal from the 24LC09 the master device will transmit the data word to be written into the addressed memory location. The 24LC09 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC09 will not generate acknowledge signals (Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC09 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24LC09 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 5-2).

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 5-1: BYTE WRITE

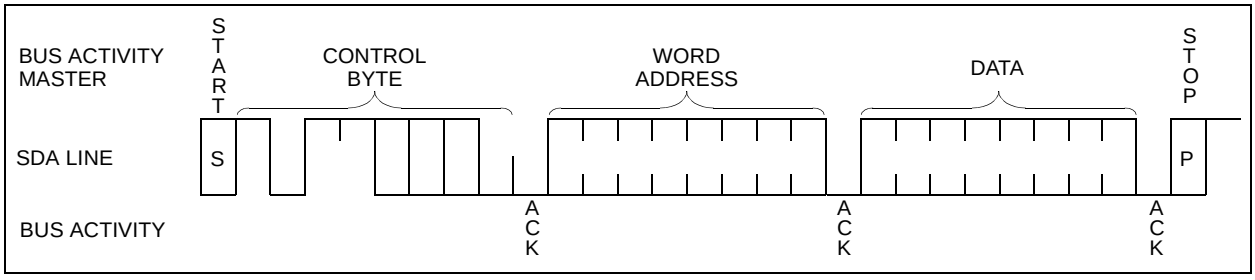
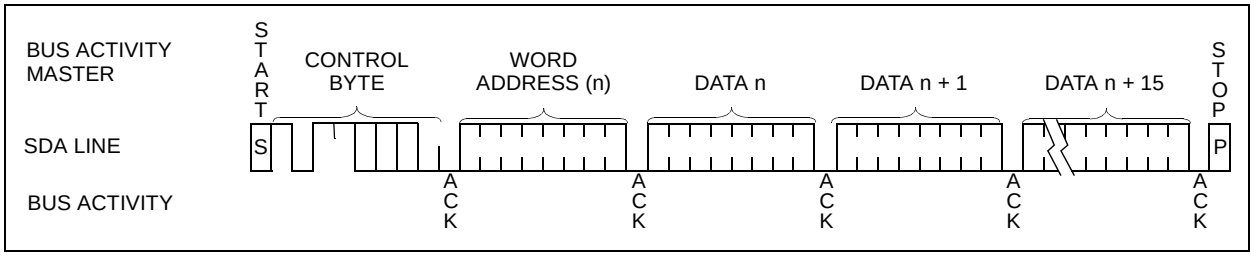


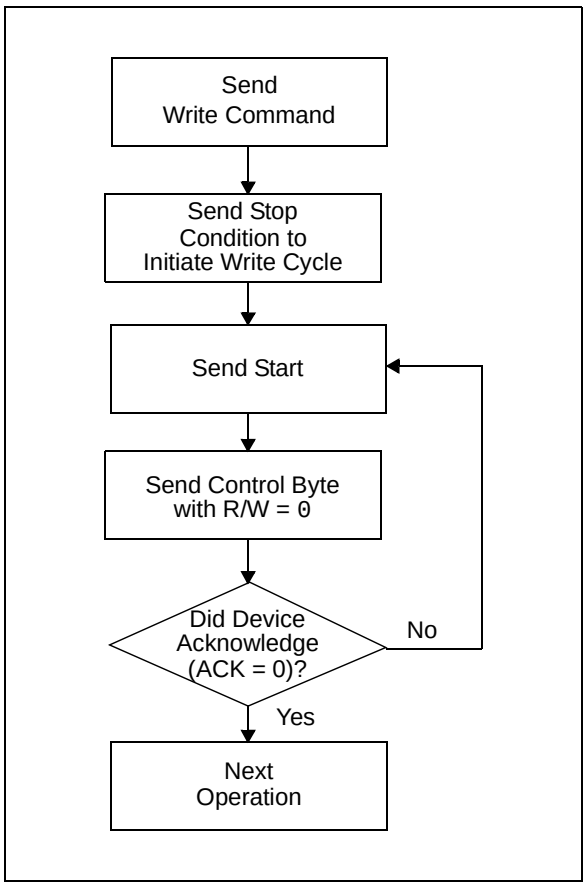
FIGURE 5-2: PAGE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24LC09 can be used as a serial ROM when the WP pin is connected to VCC. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24LC09 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC09 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC09 discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC09 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC09 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC09 discontinues transmission (Figure 8-2).

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC09 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC09 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24LC09 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24LC09 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

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FIGURE 8-1: CURRENT ADDRESS READ

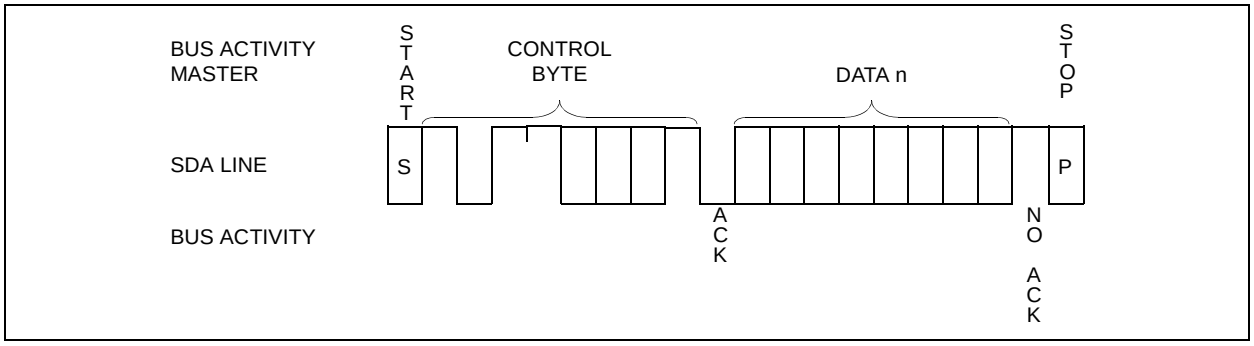


FIGURE 8-2: RANDOM READ

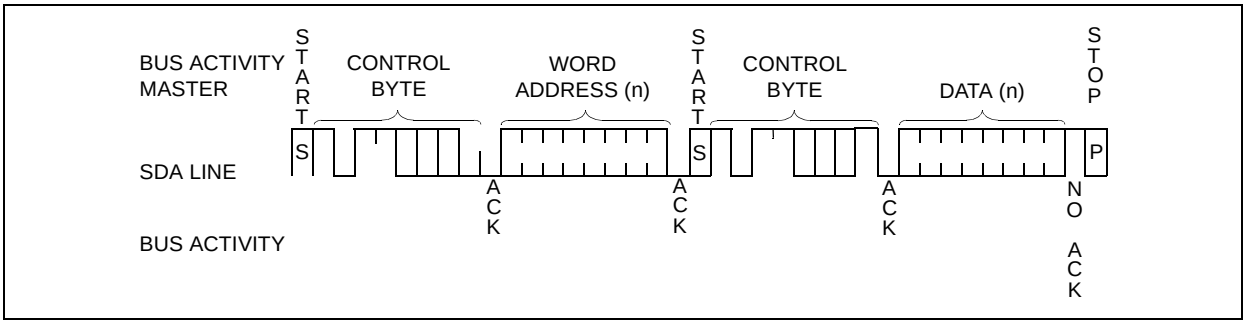
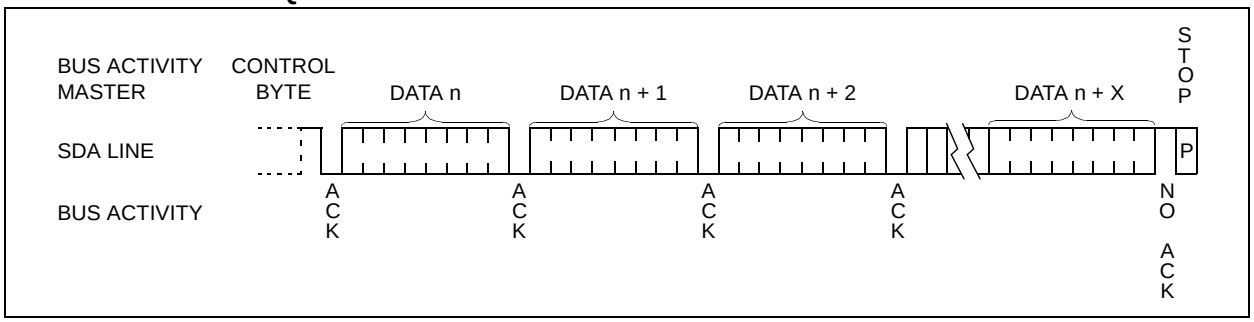


FIGURE 8-3: SEQUENTIAL READ

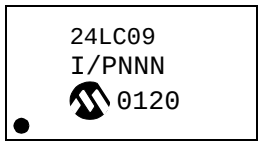


9.0 PACKAGING INFORMATION

9.1 Package Marking Information

8-Lead PDIP (300 mil)

Example



8-Lead SOIC (150 mil)

Example

Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code).

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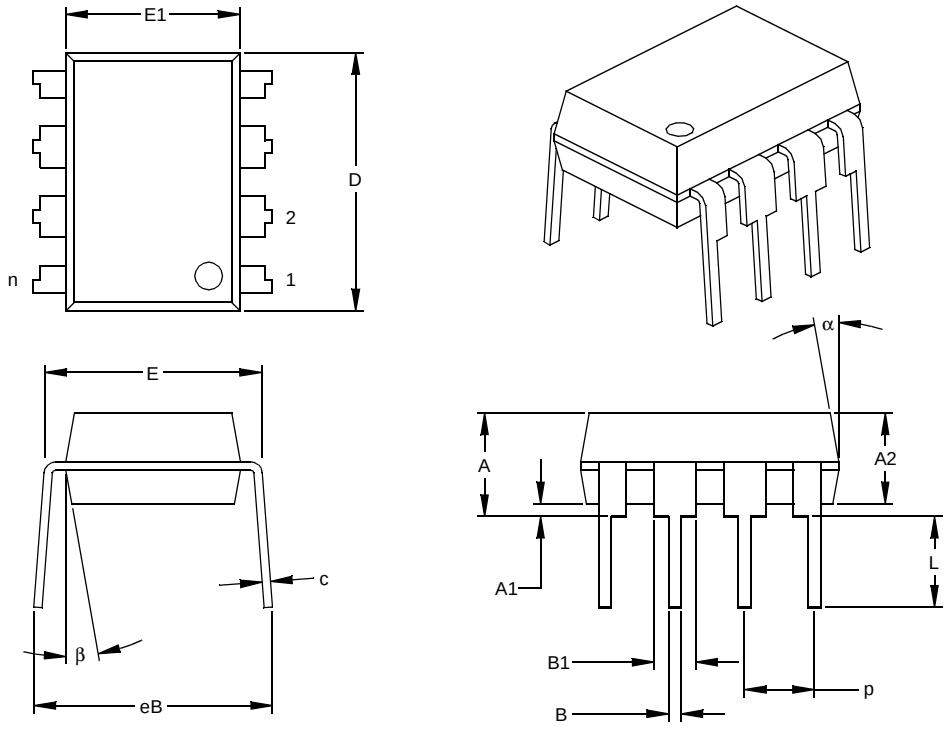
8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

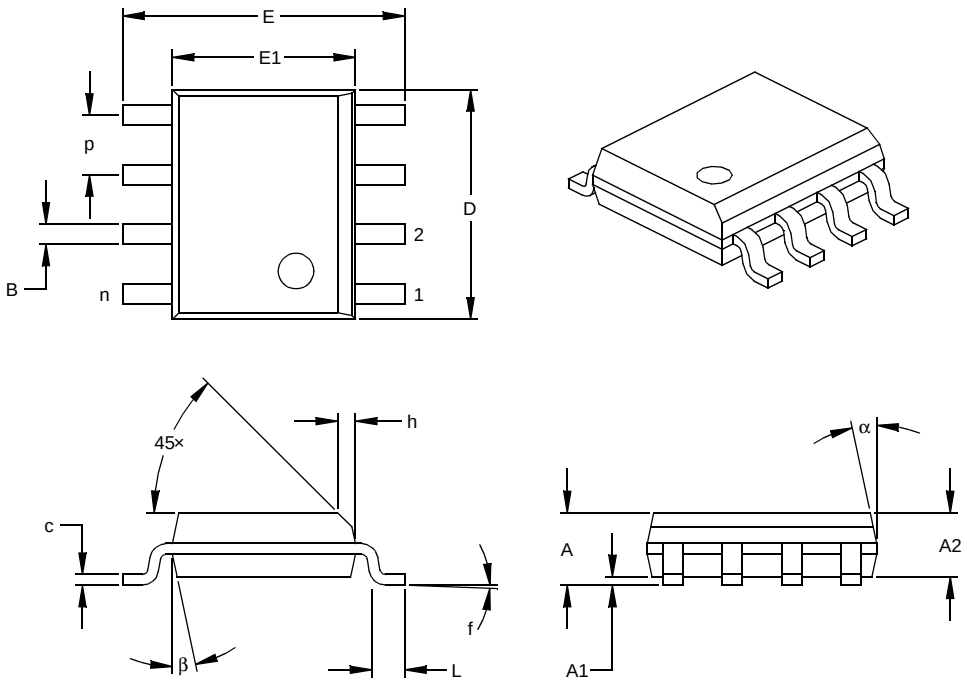


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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013001

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Device: **24LC09** Literature Number: **DS21675B**

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	24LC09:	8K I^2C Serial EEPROM
	24LC09T:	8K I^2C Serial EEPROM (Tape and Reel)
Temperature Range:	I =	-40°C to +85°C
Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead

Examples:

a) 24LC09-I/P: Industrial Temperature, PDIP package, normal V_{DD} limits

b) 24LC09-I/SN: Indistrial Temperature, SOIC package, normal V_{DD} limits.

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