EQCO850SC.3-HS
EQCO875SC.3-HS

EQCO850SC.3-HS/EQCO875SC.3-HS Single-Coax Transceiver for LVDS and Gigabit Ethernet Applications

Features

- Combined Transmitter and Receiver with an Integrated Equalizer to Form a Full-Duplex Bidirectional Connection over a Single 50Ω Coax Cable (EQCO850SC-HS) or 75Ω Coax Cable (EQCO875SC-HS)
- Internal LVDS Termination Resistors for Low External Discrete Count
- Allows Power and Data Signal Distribution Over Coax
- Single 3.3 V Supply
- 16-Pin, 0.65 mm Pin Pitch, 4 mm QFN Package
- Pb-Free and RoHS Compliant

Applications

This solution is useful and economical for many markets and applications, including the following:

- Camera Networks
  - Home Security, Surveillance, Industrial/ Inspection, Medical Cameras
- Coax Cable Distribution Infrastructure

Introduction

The EQCO850SC-HS single-coax transceiver is designed to simultaneously transmit and receive signals on a single 50Ω coax cable. A sister product, the EQCO875SC-HS, can achieve similar performance when used in 75Ω coaxial systems.

The EQCO850SC.3-HS works for 50Ω coax applications and the EQCO875SC.3-HS works for 75Ω coax applications. Everything is the same between both parts except the part number, the coax resistance and the characteristic impedance of transmission lines and connectors between the chip and the edge of the boards. Refer to Section 5.0 “Application Information” for information about the typical application circuit.

TYPICAL EQUALIZATION PERFORMANCE FOR EQCO850SC.3-HS

Bit Rate	EQCO850SC.3-HS range using		
	RG174 (Ø 2.8 mm)	RTK (Ø 2.8 mm)	RG58 (Ø5 mm)
1 Gbps	15m	25m	30m

Note: For other cable types, the length that can be reached in full-duplex may have a maximum of -12 dB insertion loss at 625 MHz, for a bit rate of 1.25 Gbps. Equalizer performance works up to much higher levels in half-duplex.

TYPICAL EQUALIZATION PERFORMANCE FOR EQCO875SC.3-HS

Bit Rate	EQCO875SC.3-HS range using		
	RG179	RG59	RG6
1.25 Gbps	20m	40m	80m

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Conventions

The following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
SIGNAL	Signal Name
msb, lsb	Most significant bit, least significant bit
MSB, LSB	Most significant byte, least significant byte
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
code	Instruction code, or API function or parameter
Multi Word Name	Used for multiple words that are considered a single unit, such as: *Resource Allocate* message, or *Connection Label*, or *Decrement Stack Pointer* instruction.
Section Name	Emphasis, Reference, Section or Document name.
$\overline{\text{VAL}}$	Over-bar indicates active low pin or register bit
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times.
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

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1.0 DEVICE OVERVIEW

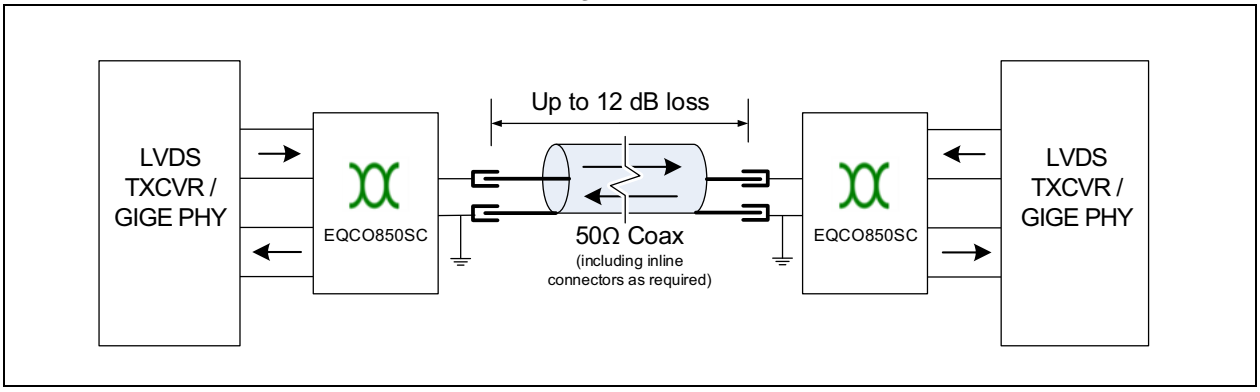
The EQCO850SC-HS (EQCO875SC-HS) is ideally suited for simplex and duplex LVDS connections over 50Ω (75Ω) coax cables at 1.25 Gbps. For correct operation, the signals must be NRZ (Non-Return-to-Zero) 8B10B encoded. Excellent EMI/RFI coax cable shielding allows for good EMI properties.

The EQCO850SC-HS operates with a variety of 50Ω coax cables, including the cost-effective 2.8 mm diameter RTK cable (e.g., Leoni Dakar 302) commonly used for radio and navigation antennas in automotive applications. This cable fits well with the standardized (DIN and USCAR), high-performance, cost-effective RF connectors: SAE/USCAR-18 "FAKRA/SMB RF Connector".

The EQCO875SC-HS is typically useful in situations where legacy 75Ω cables are present.

Figure 1-1 illustrates a typical LVDS coaxial connection. It can be used for Gigabit Ethernet connections over a single coax cable.

FIGURE 1-1: TYPICAL LVDS LINK USING EQCO850SC-HS



2.0 EQCO875SC.3-HS PINOUT

FIGURE 2-1: EQCO850SC.3-HS PIN DIAGRAM (VIEWED FROM TOP)

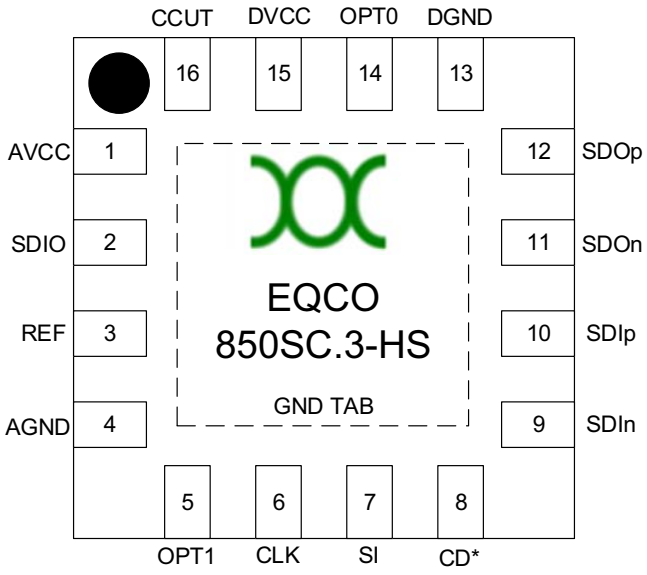


TABLE 2-1: EQCO850SC.3-HS PIN DESCRIPTIONS

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Connect to ground of power supply.
15	DVCC	Power	Connect to +3.3V of power supply.
13	DGND	Power	Connect to ground of power supply.
1	AVCC	Power	Analog VCC. Connect to +3.3V of power supply via RF choke and capacitor to cable outer screen.
4	AGND	Power	Analog GND. Connect to cable outer screen.
2	SDIO	Bidirectional	Serial Input/Output. Connect to center conductor of 50Ω coax cable.
3	REF	Bidirectional	Reference. Connect through 50Ω resistor (or impedance matched to cable) to cable outer screen.
8	CD	Output (open drain)	Leave unconnected. Use of this pin is not advised in practice.
10, 9	SDIp/SDIn	Input	Positive/negative differential serial input. Connect to the LVDS output.
12, 11	SDOp/SDOn	Output	Positive/negative differential serial input. Connect to the LVDS input.
14, 5	OPT0, OPT1	Input	Connect Opt0 and Opt1 both to DVCC (3.3V).
6, 7	CLK, SI	Input	Used for Production test. Connect to DGND.
16	CCUT	Analog	Not used in LVDS applications. Connect to Pin 15 DVCC.

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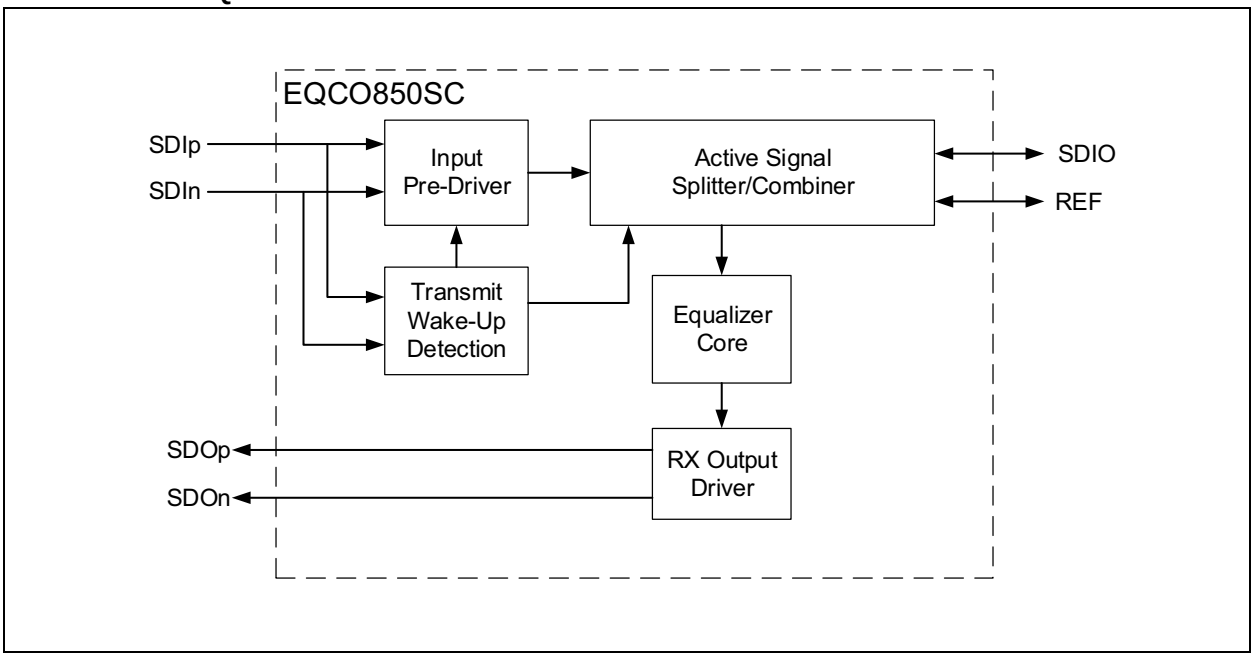
FIGURE 2-2: EQCO850SC-HS BLOCK DIAGRAM SHOWING ELECTRICAL CONNECTIONS



2.1 SDIp/SDIn

SDIp/SDIn together form a differential input pair. The serial data received on these pins will be transmitted on SDIO. The Input pre-driver automatically corrects for variations in signal levels and different edge slew rates at these inputs before they go into the Active Splitter/Combiner for transmission over the coax.

SDIp and SDIn inputs are differentially terminated by 100Ω on-chip. The center of the 100Ω is connected to DGND with a 10 kΩ resistor for DC biasing. The inputs also have protection diodes to ground for ESD purposes. Always AC-couple these inputs to the outputs of the LVDS driver.

A Transmit Wake-Up detection circuit puts both the Input pre-driver and the Active Signal Splitter/Combiner into a low-power mode when no signal is detected on the SDIp/SDIn signal pair.

2.2 SDIO/REF

The signal on the SDIO pin is the sum of the incoming signal (i.e. the signal transmitted by the EQCO850SC-HS on the far-end side of the coax) and the outgoing signal (i.e. the signal based on SDIp/SDIn). The far-end signal is extracted by subtraction of the near-end signal, and it is this voltage that the equalizer analyzes and adaptively equalizes for level and frequency response based on the knowledge that the originating signal is DC-balanced and run-length encoded before transmission.

The REF signal carries a precise anti-phase current to the transmit current on SDIO. REF must be connected directly to AGND at the connector (see Figure 5-1) via a resistor precisely matched to the impedance of the coaxial cable used.

2.3 SDOp/SDOn

SDOp/SDOn together form a differential pair outputting the reconstructed far-end transmit signal. The EQCO850SC-HS uses LVDS drivers with source matching for a 100Ω transmission line. This LVDS signal can normally be connected (subject to input common-mode requirements) directly to the RX signal pair of a standard LVDS receiver.

2.4 CLK, SI

These pins are used for production test and/or reserved for future options. For normal operation, connect them to DGND as indicated in Table 2-1.

3.0 CIRCUIT OPERATION

3.1 Pre-Driver

The pre-driver removes any dependency on the LVDS transmitter for the amplitude and rise time of the outgoing signal on SDIO.

3.2 Active Signal Splitter/Combiner

The active splitter/combiner controls the amplitude and rise time of the outgoing coax signal and transmits it via a precise 50Ω output termination resistor. The output resistor when balanced with the coax characteristic impedance also forms part of a hybrid splitter circuit which subtracts the TX output from the signal on the SDIO output to give yield the far end TX signal. The return loss of the coax termination is a key factor in the performance of the line hybrid.

3.3 Equalizer Core

The EQCO4850SC-HS has an embedded high-speed equalizer in the receive path with unique characteristics:

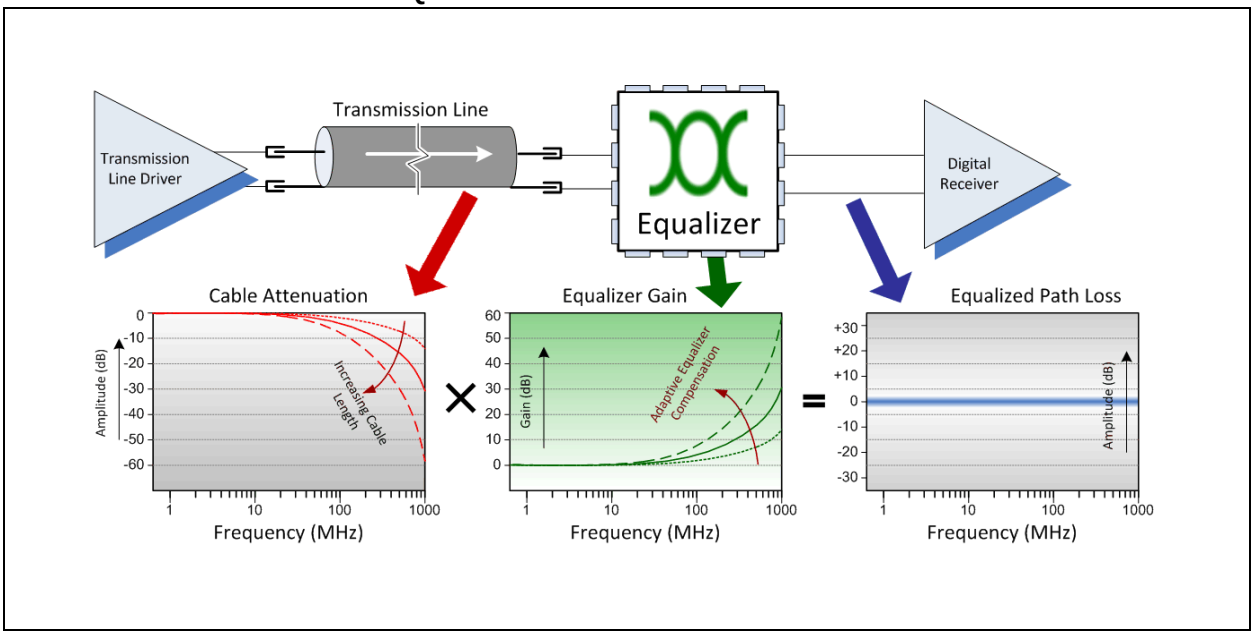
- Auto-adaptive

The equalizer controls a multiple-pole analog filter which compensates for attenuation of the cable, as illustrated in Figure 3-1. The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable gain

EQCO850SC-HSs are used in pairs; one at each end of the coax. The EQCO850SC-HS can be used with any LVDS driver with a differential transmit amplitude in the range of 300 mV to 800 mV; the transmit amplitude on the coax is regulated by the input pre-driver. The receiver equalizer has variable gain to compensate for attenuation through the coax. Example equalizer performance measurements can be found in Section Appendix A: “Typical Operating Characteristics”.

FIGURE 3-1: PRINCIPLE OF EQUALIZER OPERATION



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4.0 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 4-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Typ.	Max.	Units	Conditions
Storage Temperature	-65	—	+150	°C	
Ambient Temperature	-55	—	+125	°C	Power Applied
Operating Temperature	-40	—	+85	°C	Normal Operation (VCC = 3.3V ±5%)
Supply Voltage to Ground	-0.5	—	+4.0	V	
DC Input Voltage	-0.5	—	+4.0	V	
DC Voltage to Outputs	-0.5	—	+4.0	V	
Current into Outputs	—	—	90	mA	Outputs Low

TABLE 4-2: ELECTRICAL CHARACTERISTICS (OVER THE OPERATING VCC AND -40 TO +85°C RANGE)

Parameter	Min.	Typ.	Max.	Unit	Description
Power Supply					
V_{CC}	3.2	3.3	3.4	V	Supply voltage.
I_s	47.5	62.5	75.5	mA	Supply current, both transmitting and receiving.
I_{sr}	25	35	43	mA	Supply current when only receiving.
SDIp/SDIn Input (LVDS-like)					
ΔV_i	250	—	800	mV	Input amplitude $V_{SDIp,n}$.
V_{turnon}	80	140	200	mV	Minimal ΔV_i to turn on transmit function.
V_{cmin}	Note 4	0	Note 4	V	Common-mode input voltage (terminated to DGND via 10 kΩ and with protection diodes).
R_{input}	93	104	117	Ω	Differential input termination.
SDIO Connection to Coax					
Z_{coax}	48 (72)	50 (75)	52 (78)	Ω	Coax cable characteristic impedance.
R_{SDIO}	46 (69)	51 (76)	55 (82)	Ω	Input impedance between SDIO and AGND.
R_{loss}	15	—	—	dB	Coax return-loss as seen on SDIO pin. Frequency range = 10 MHz-625 MHz.
ΔV_{TX}	270	325	380	mV	Transmit amplitude.
t_{rise_tx}	350	450	550	ps	Rise/fall time 20% to 80% of ΔV_{TX}.
Att_{max}	—	12	—	dB	Cable attenuation budget @ 625 MHz.
ΔV_{RXmin}	—	40	—	mV	Minimum input for fully reconstructed output.

TABLE 4-2: ELECTRICAL CHARACTERISTICS (OVER THE OPERATING VCC AND -40 TO +85°C RANGE) (CONTINUED)

SDOp/SDOn Outputs (LVDS-compatible)					
ΔV_o	300	350	400	mV	Output amplitude $V_{SDOp,n.}$
V_{cmout}	1.1	1.2	1.3	V	Common-mode output voltage.
ΔV_{o_off}	-20	0	20	mV	Output amplitude $V_{SDOp,n}$ with equalizer off.
R_{output}	92	102	115	Ω	Differential termination between SDOp and SDOn.
t_{rise_o}	150	240	350	ps	Rise/fall time 20% to 80% of $V_{SDOp,n}$.

TABLE 4-3: JITTER PERFORMANCE

Parameter	Min.	Typ.	Max.	Units	Conditions
Jitter peak-to-peak on SDO	—	170	500	ps	12dB cable attenuation, over full V_{CC}, ΔV_{TX} range, temp range, full duplex 8B10B encoded pattern

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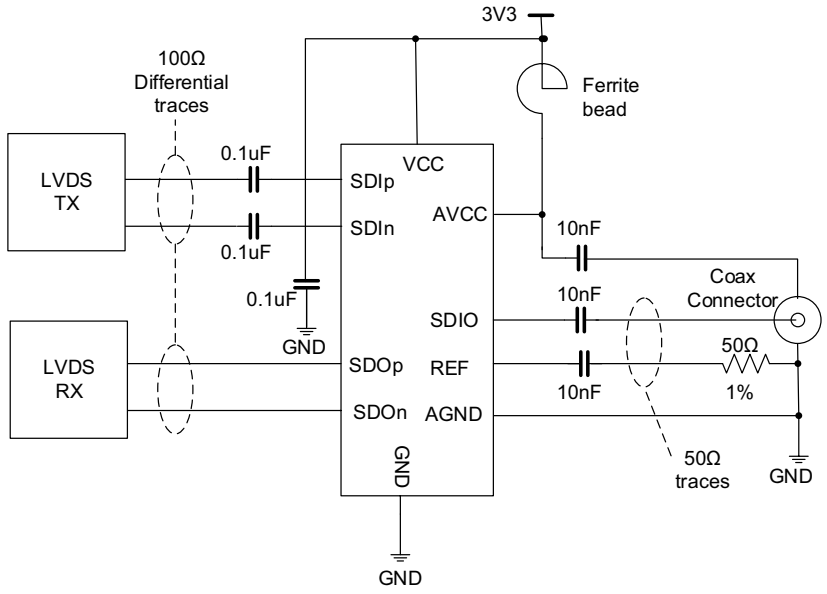
5.0 APPLICATION INFORMATION

5.1 Typical LVDS Application Circuit

Figure 5-1 illustrates a typical schematic implementation.

FIGURE 5-1: EQCO850SC.3-HS TYPICAL APPLICATION CIRCUIT



Note: For EQCO875SC.3-HS, replace the two 50Ω references with two 75Ω references.

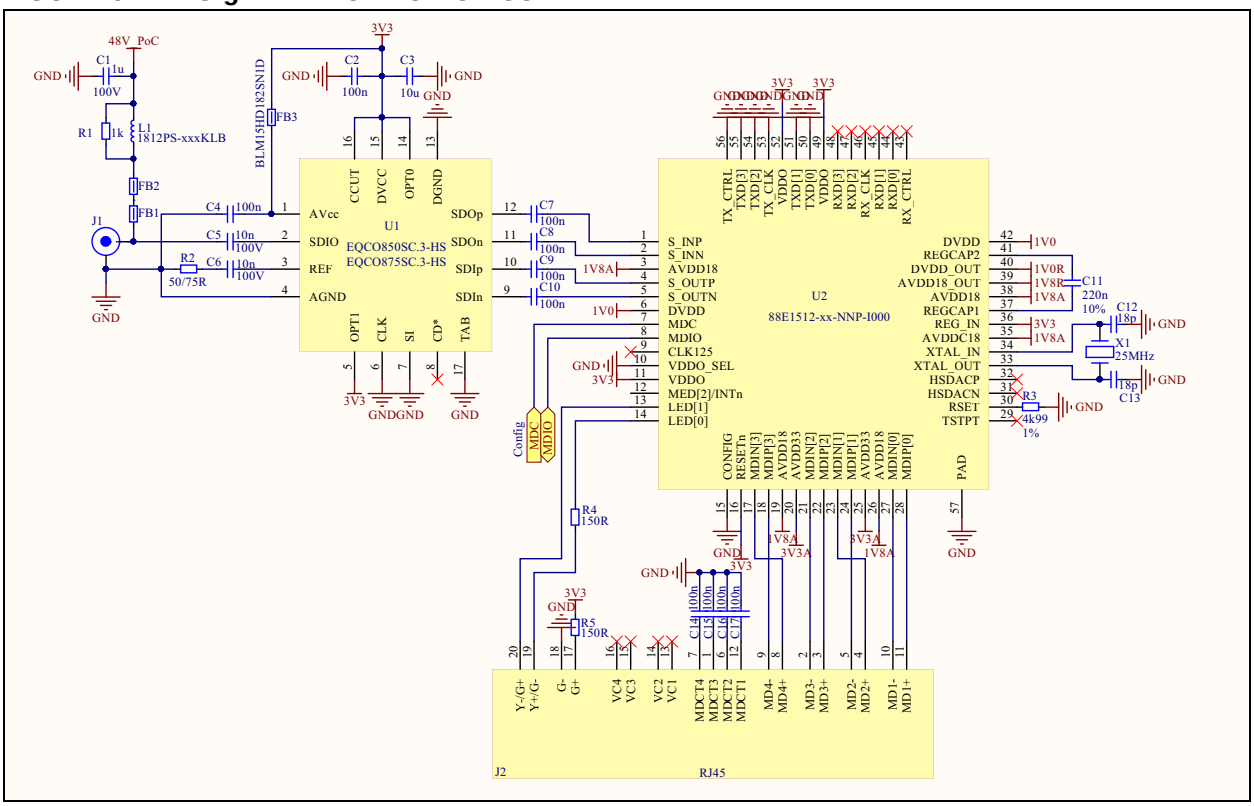
To improve isolation from noise on the board power plane and improve EMC immunity and emissions, it is recommended to power the transmit side of the equalizer (AVCC) through a ferrite bead. A 0.1 µF decoupling capacitor should be placed as close as possible to the chip between the VCC pin and the GND pin. Ground vias should be placed as close as possible to the device GND pins to minimize inductance.

In full duplex, the maximum-length performance depends on the level of near-end crosstalk and far-end return-loss. For full-duplex operation, position the chip close to the used connector.

All the elements need to have impedances according to the choice between a 50Ω system or a 75Ω system: the chips used on both sides, the impedances between the chip and the connector, the PCB connector itself, the connectors on the coax cable and the coax itself. If one impedance is wrong (e.g. a 75Ω BNC connector in a 50Ω system), this impedance discontinuity will cause a reflection, limiting the performance of the full-duplex maximum cable length.

5.2 Gigabit Ethernet Application Circuit

FIGURE 5-2: GigE APPLICATION CIRCUIT



The EQCO850SC.3-HS/EQCO875SC.3-HS can be interfaced with a Gigabit Ethernet PHY capable of 1000Base-X or SGMII operation.

The device operates completely transparent to the Ethernet PHY.

The schematic in Figure 5-2 shows a Gigabit Ethernet to coax converter. Two of such modules can be used in an Ethernet over coax application.

5.3 Power Over Coax

Figure 5-2 shows a typical power over coax (PoC) implementation with two ferrite beads (FB1, FB2) and an inductor (L1).

Alternatively, depending on the PoC and system requirements, a circuit with one ferrite bead can be used.

The PoC circuit increases the return loss of the system and therefore reduces the maximum attainable cable length.

To minimize the impact, special care must be taken during component selection.

Generally, the FB M series from Taiyo Yuden for the ferrite beads and the 1812PS series from Coilcraft are recommended.

TABLE 5-1: RECOMMENDED COMPONENTS

PoC Current	Ferrite Beads	Inductor
<1A	FBMH608HM102-T FBMH1608HL331-T	1812PS-103KLB
<1A	FBMH3225HM102NT	1812PS-152KLB

Depending on the specific application, other values may be optimal.

Typically the best results are obtained by choosing the ferrite bead with the smallest footprint and high impedance (~1kΩ at 625MHz) and the inductor with the highest SRF allowed by the required PoC current.

It is possible to reduce the impact of the PoC network by adding the same ferrite beads to the REF output between R2 and C6 to ground.

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5.4 Guidelines for PCB Layout

Because signals are strongly attenuated by long cables, special attention should be paid to the PCB layout between the coaxial connector and the EQCO850SC-HS. The EQCO850SC-HS should be as close as is practical to the coaxial connector. The trace between the coaxial connector and the EQCO850SC-HS (EQCO875SC-HS) must be a 50Ω (75Ω) trace referenced to GND. To avoid noise pickup, other traces carrying digital signals or fast-switching signals should be placed as far away as possible from this trace.

The following diagram shows the layout of the critical section of the circuit shown in Figure 5-2.

FIGURE 5-3: CIRCUIT DIAGRAM (CRITICAL LAYOUT SECTION)

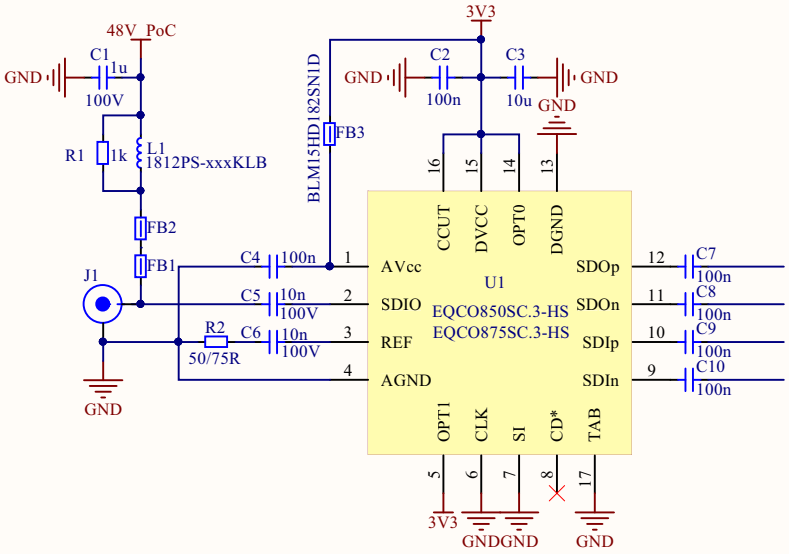
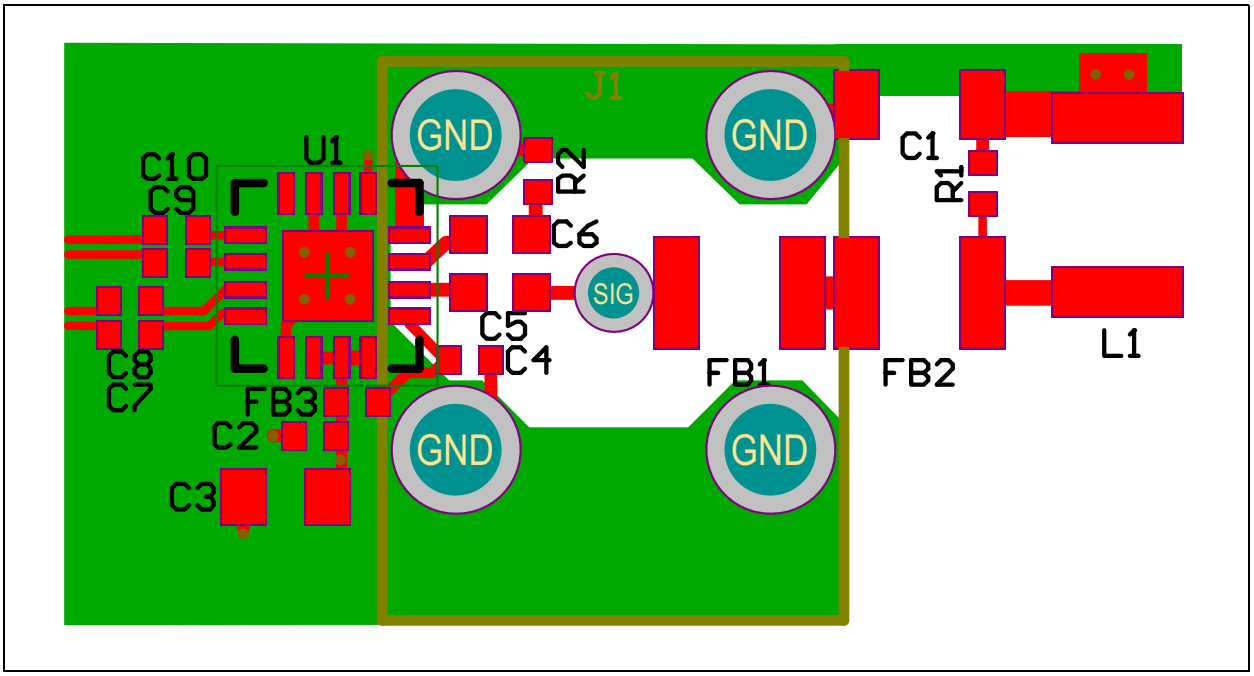


FIGURE 5-4: RECOMMENDED LAYOUT



The ground layout of the EQCO850SC.3-HS is critical to the EMC and EMI performance of the circuit. The AGND connection should be made directly to the body of the connector as shown in Figure 5-3. It should not be connected directly to the GND tab of the chip. Similarly, AVCC should be decoupled directly to the connector body (see position of C4). The termination resistor (R2) must have its ground connection at the connector body.

To reduce the parasitic capacitance of the connector, power over coax network and chip package, the ground and power planes should be removed underneath these areas as indicated in Figure 5-3.

The SDIp/SDIn and SDOp/SDOn differential traces should be laid out as 100Ω differential traces.

The power over coax network should be placed as close as possible to the connector.

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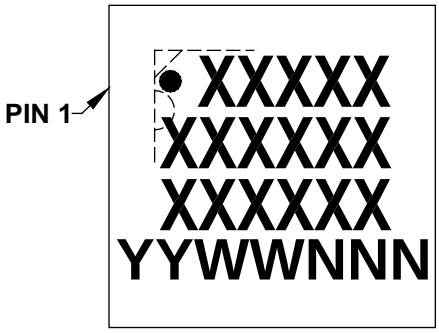
6.0 PACKAGING INFORMATION

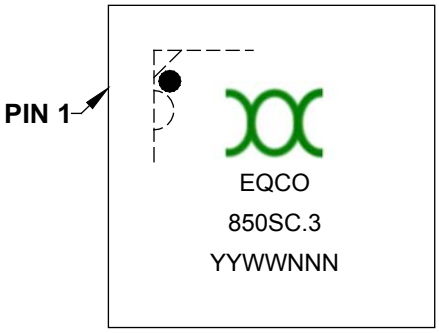
6.1 Package Marking Information

16-Lead Plastic Quad Flat, No Lead Package – 4x4x0.9 mm Body [QFN]

16-Lead QFN (4x4x0.9 mm)



Example

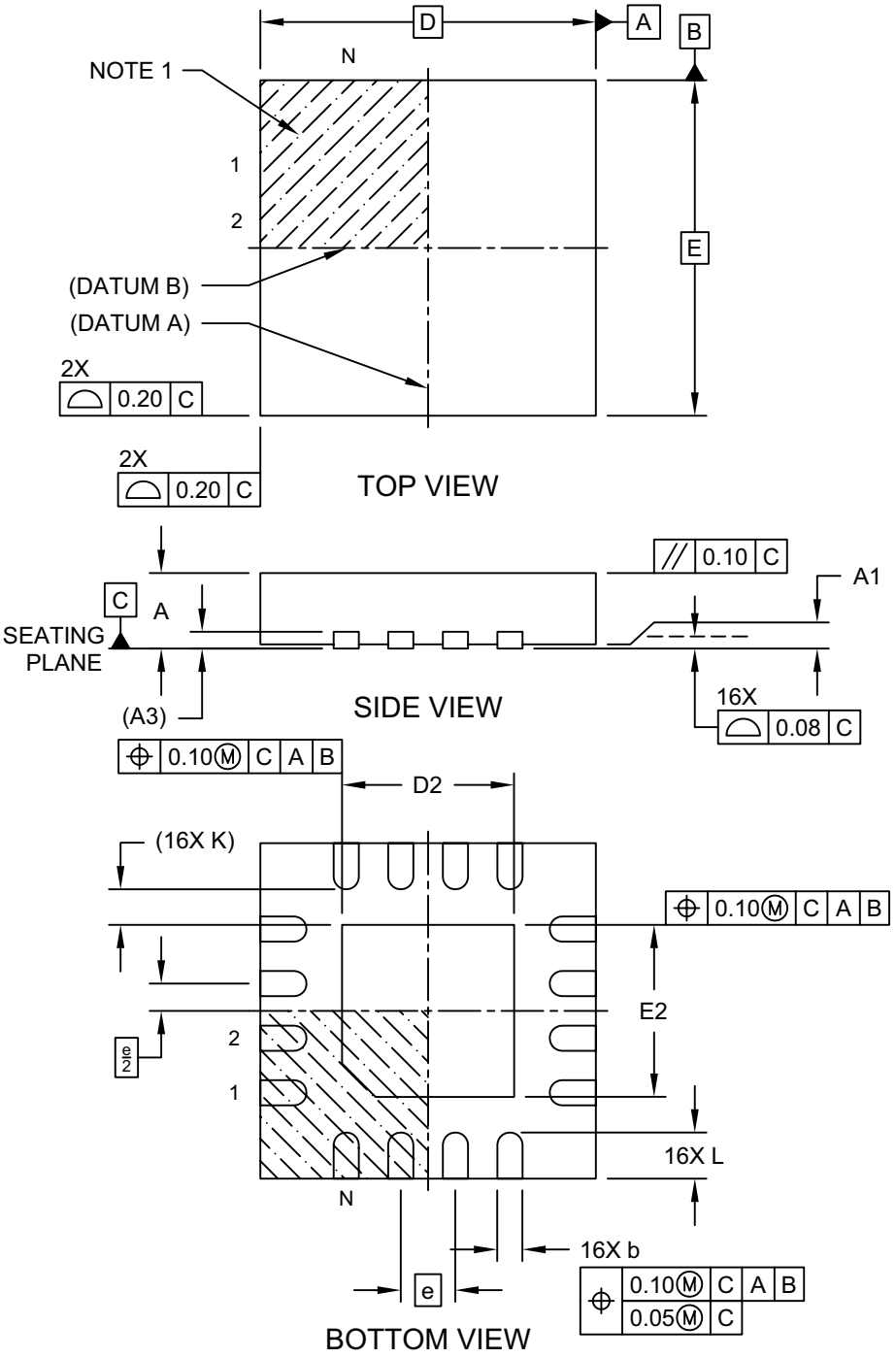


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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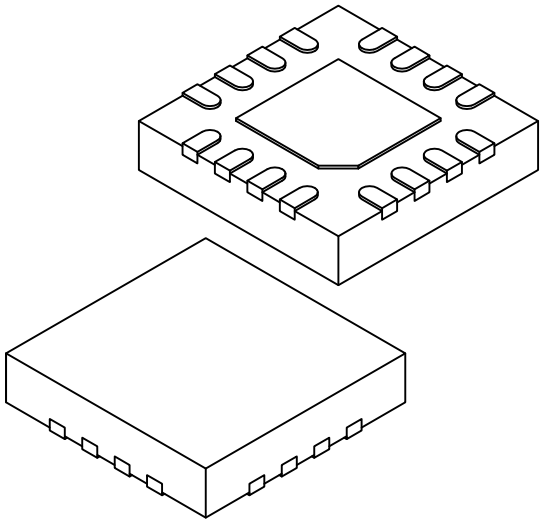
16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.87	0.95
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	1.95	2.05	2.15
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	1.95	2.05	2.15
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.45	0.55	0.65
Terminal-to-Exposed-Pad	K		0.425 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-259B Sheet 2 of 2

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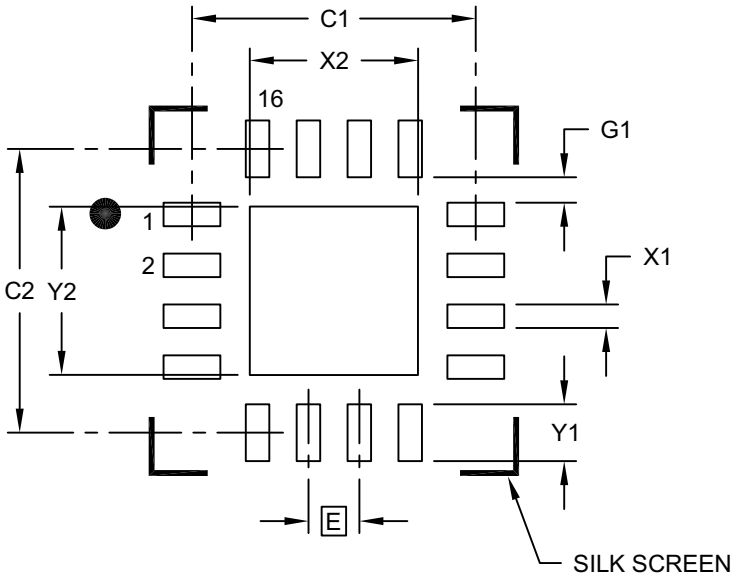
16-Lead Plastic Quad Flat, No Lead Package (8E) - 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			2.15
Optional Center Pad Length	Y2			2.15
Contact Pad Spacing	C1		3.625	
Contact Pad Spacing	C2		3.625	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.725
Contact Pad to Center Pad (X16)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2259A

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APPENDIX A: TYPICAL OPERATING CHARACTERISTICS

All measurements at VCC = 3.3V, temp = +25°C, data pattern = PRBS9, 630 mV PHY transmit amplitude.

FIGURE A-1: TYPICAL EYE AT SDO_P WITH A 1M COAX TYPE RG174

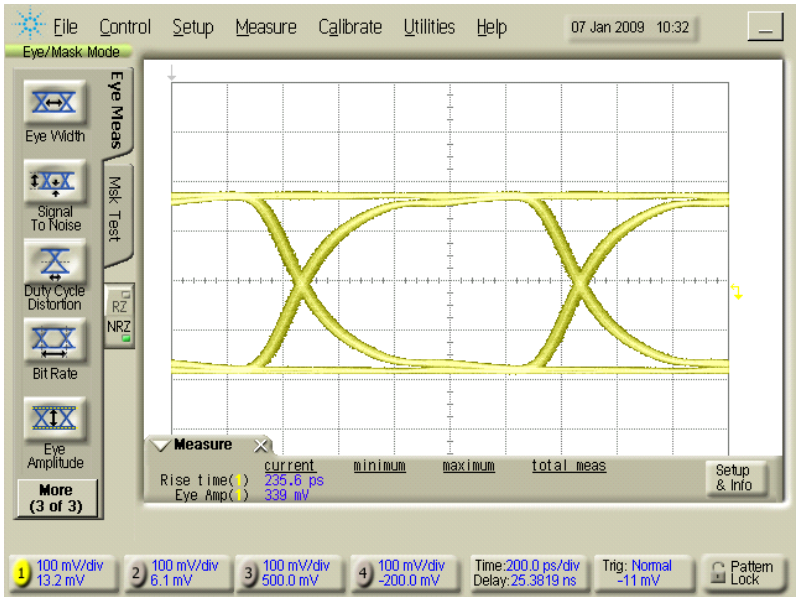
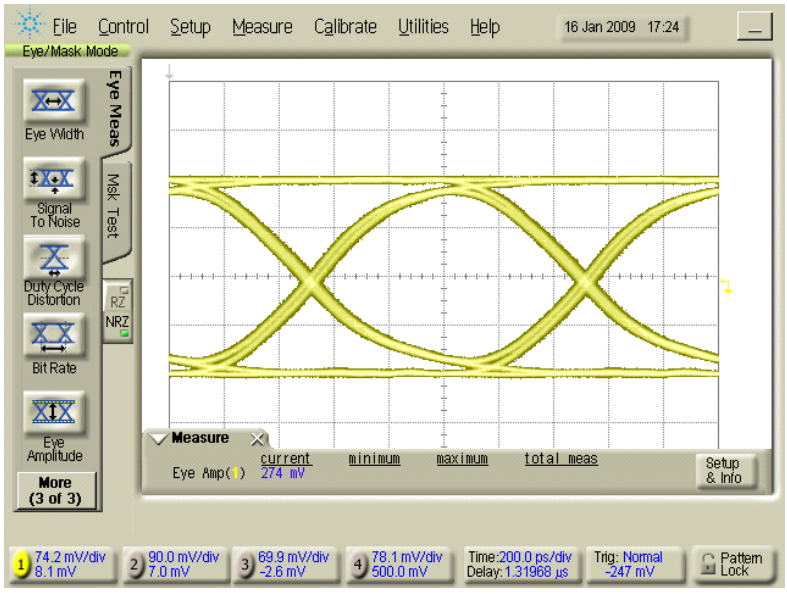


FIGURE A-2: TYPICAL EYE AT SDIO OUTPUT THROUGH 1M COAX CABLE



The following figures show a typical system link EYE-diagram at room temperature through a variable cable length full and half duplex. The differential output V_{SDOp}-V_{SDOn} is shown. The duty cycle distortion is due to the use of a shielded twisted pair cable/connector. Duty cycle distortion is normally very small.

FIGURE A-3: 1M RG174, HALF-DUPLEX

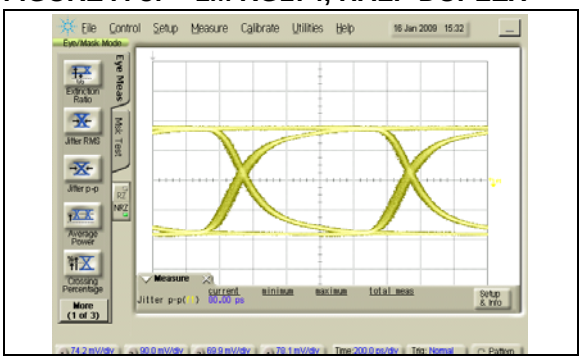


FIGURE A-4: 5M RG174, HALF-DUPLEX

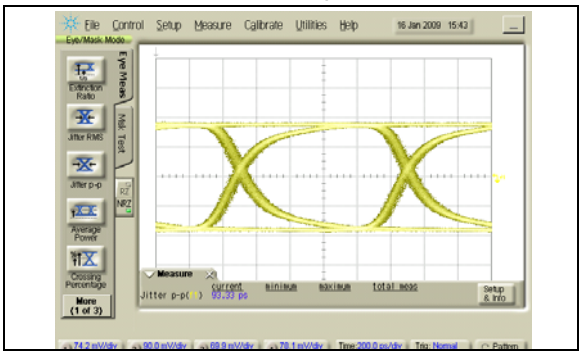


FIGURE A-5: 10M RG174, HALF-DUPLEX

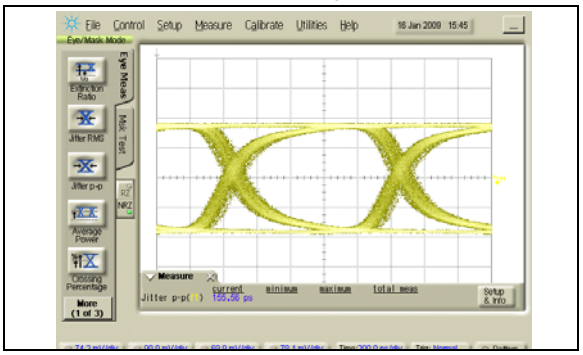


FIGURE A-6: 20M RG174, HALF-DUPLEX

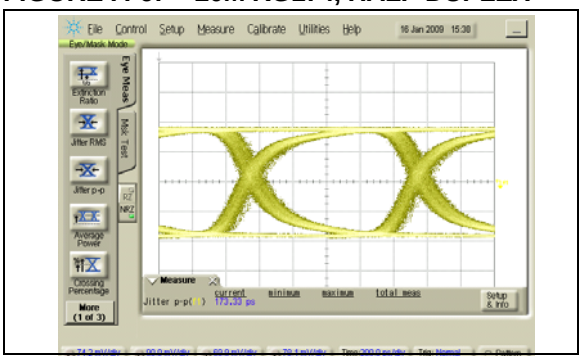


FIGURE A-7: 1M RG174, HALF-DUPLEX

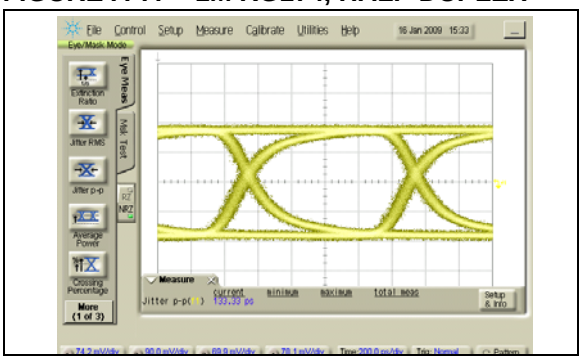


FIGURE A-8: 5M RG174, HALF-DUPLEX

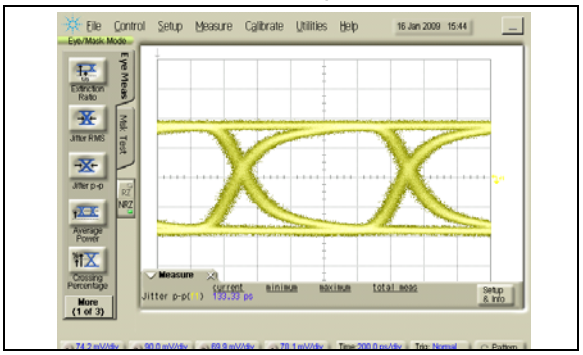


FIGURE A-9: 10M RG174, HALF-DUPLEX

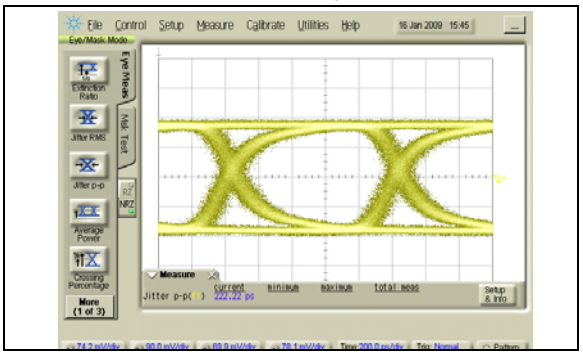
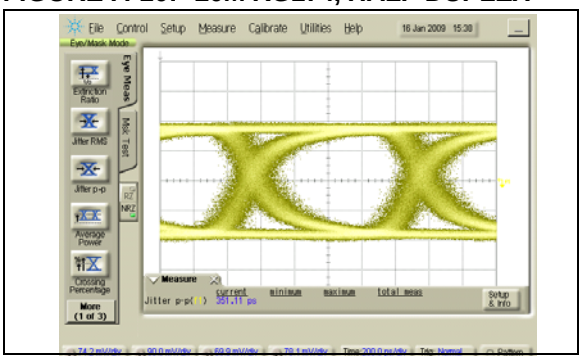


FIGURE A-10: 20M RG174, HALF-DUPLEX



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APPENDIX B: REVISION HISTORY

Revision D (December 2018)

- In Section 4.1 “Absolute Maximum Ratings”, in Electrical Characteristics table, changed Vcc range set to 3.2-3.4V
- In Section 5.2 “Gigabit Ethernet Application Circuit”, Included Gigabit Ethernet Application Circuit

Revision C (April 2016)

- Revised Section 2.1 “SDIp/SDIn”

Revision B (April 2016)

- Updated Section 6.0 “Packaging Information”.
- Removed electrostatic discharge ratings from Table 4-1.
- Minor typographical changes.

Revision A (July 2015)

- This is the initial release of the document in the Microchip format. This replaces EqcoLogic document version 2.0.

TABLE B-1: REVISION HISTORY

Revision Level	Date	Correction
2v0	1/28/14	Targeting data sheet for LVDS and Gigabit Ethernet applications. Merging 50Ω and 75Ω systems into one data sheet. Temperature limits set to -45°C to +85°C.
1v0	4/30/10	Based on the EQCO800SC generic data sheet, adapted for LVDS

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PART NO.	XXXX
Device	Package

Device:	EQCO850SC.3-HS EQCO875SC.3-HS
Package:	TRAY = Tray “blank” = Tube

Examples:

a) EQCO850SC.3-HS-TRAY = 50Ω Coax, Industrial temperature, 16-Lead QFN package, Tray packaging

b) EQCO875SC.3-HS = 75Ω Coax, Industrial temperature, 16-Lead QFN package, Tube packaging

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