

Bluetooth® 4.2 ROM Stereo Audio SoC

Features

- Qualified for Bluetooth v4.2 specification
- ROM SoC that supports Stereo Mode (audio playback on two Bluetooth audio devices)
- Bluetooth Audio Profiles
 - A2DP 1.3
 - AVRCP 1.6
 - HFP 1.6
 - HSP 1.2
 - SPP 1.2
- Bluetooth Low Energy (BLE)
 - Generic access service
 - Device information service
 - Proprietary services for data communication
 - Apple Notification Center Service (ANCS)
- Supports 16 kHz high definition (HD) voice
- Audio Interfaces
 - I²S digital output
 - Analog output
 - Aux input
 - Microphone inputs
- Integrated battery charger (up to 350 mA)

Baseband Features

- 16 MHz main clock input
- Built-in EEPROM
- Connects simultaneously to two hosts over HFP/A2DP and SPP/BLE
- Adaptive Frequency Hopping (AFH)

Audio Codec

- Sub-band Coding (SBC) and Advanced Audio Coding (AAC) decoding
- 20-bit digital-to-analog converter (DAC) with 98 dB SNR

Package Details

Parameter	IS2064S	IS2064B
Package type	QFN	BGA
Pin count	68	61
Contact/Lead Pitch	0.4	0.5
Package size	8x8x0.9	5x5x0.9

Note: All dimensions are in millimeters (mm) unless specified.

- 16-bit analog-to-digital converter (ADC) with 92 dB SNR
- Supports up to 24-bit, 96 kHz I²S digital audio

RF Features

- Transmit output power: +2 dBm
- Receive sensitivity: -90 dBm (2 Mbps EDR)
- Combined Tx/Rx RF terminal simplifies external matching and reduces external antenna switches
- Tx/Rx RF switch for Class 2 or Class 3 applications
- Integrated synthesizer requires no external voltage-controlled oscillator (VCO), varactor diode, resonator or loop filter
- Crystal oscillator with built-in digital trimming compensates for temperature or process variations

DSP Audio Processing

- Includes a 32-bit DSP core
- Synchronous Connection-Oriented (SCO) channel operation
- 8/16 kHz noise suppression
- 8/16 kHz echo cancellation
- Modified Sub-Band Coding (MSBC) decoder for wide band speech
- Built-in High Definition Clean Audio (HCA) algorithms for both narrow band and wide band speech processing
- Packet Loss Concealment (PLC)
- Built-in audio effect algorithms
- Serial Copy Management System (SCMS-T) content protection

IS2064S/B

Peripherals

- UART interface for host MCU communication
- Full-speed USB 1.1 interface (IS2064S)
- Built-in lithium-ion and lithium-polymer battery charger (up to 350 mA)
- Integrated 1.8V, and 3V configurable switching regulator and low-dropout (LDO) regulator
- Built-in ADC for battery monitoring, voltage sensor and charger thermal protection
- Built-in under-voltage protection (UVP)
- LED drivers: 3 (IS2064S), 2 (IS2064B)
- GPIO: 14 (IS2064S), 9 (IS2064B)

Operating Condition

- Operating voltage: 3.2V to 4.2V
- Operating temperature: -20°C to +70°C

Applications

- Portable speakers
- Headsets and headphones
- Earbuds and neckbands

Description

The IS2064S/B is a ROM-based stereo audio SoC qualified for Bluetooth v4.2 specification with Enhanced Data Rate (EDR). It supports audio playback on two devices, such as speakers from one audio source.

It integrates a 32-bit DSP co-processor and a codec, dedicated for voice and audio applications. For voice applications, the CVSD encoding/decoding, 8K/16K noise reduction and echo cancellation are implemented. For audio applications, the SBC and AAC Low-Complexity (AAC-LC) decoding functions are used.

The IS2064S/B SoC features a 20-bit audio DAC in addition to an I²S digital audio interface that supports up to 24-bit, 96 kHz data formats. The system optimization includes an integrated battery voltage sensor, a battery charger, a switching regulator, and LDOs.

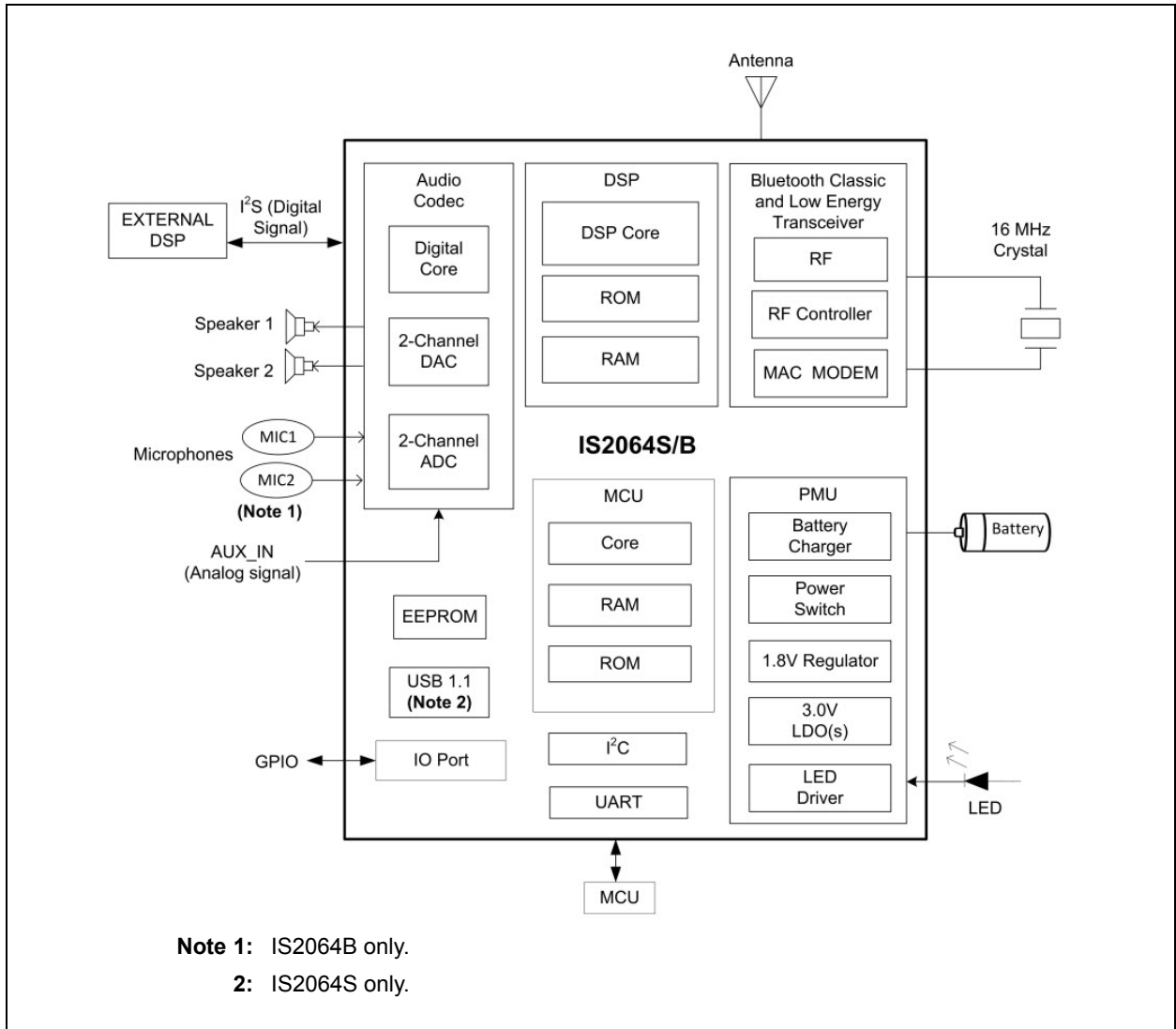
[Table 1](#) provides ordering information of the IS2064S/B SoC.

TABLE 1: ORDERING INFORMATION

Device	Bluetooth Version	Package	Part Number
IS2064S	Bluetooth 4.2, ROM SoC with integrated 1 microphone and stereo speaker output, I ² S digital interface	8x8x0.9 mm, 68-QFN package	IS2064S-114SM
IS2064B	Bluetooth 4.2, ROM SoC with integrated 2 microphones and stereo speaker output and I ² S digital interface	5x5x0.9 mm, 61-BGA package	IS2064B-114SM

Figure 1 illustrates a typical block diagram of the IS2064S/B SoC.

FIGURE 1: IS2064S/B SoC BLOCK DIAGRAM



IS2064S/B

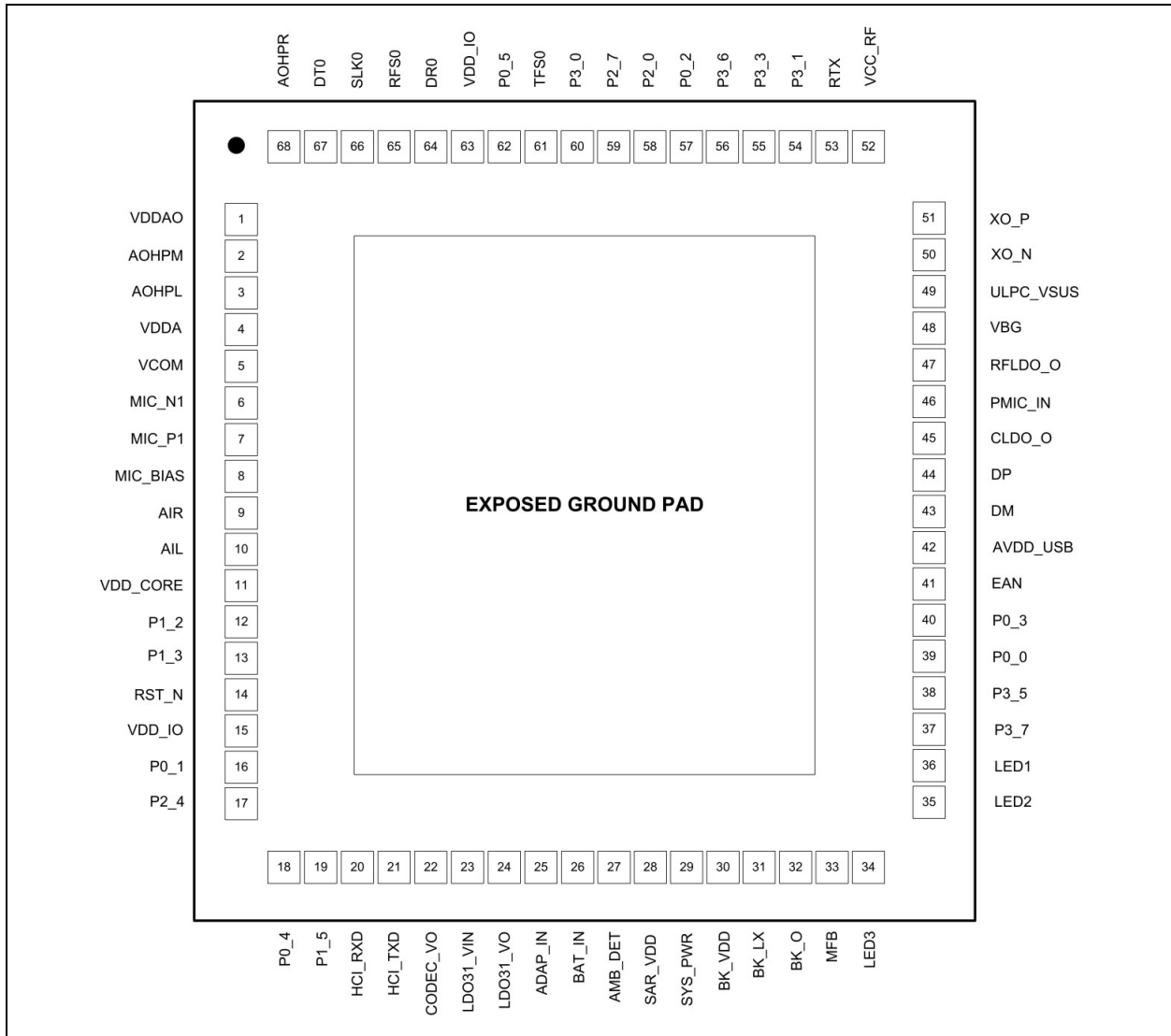
Table 2 provides the key features of the IS2064S/B SoC.

TABLE 2: IS2064S/B KEY FEATURES

Feature	IS2064S	IS2064B
Application	Portable Speaker	Headset (Gaming/over-the ear)
Pin count	68	61
Dimensions (mm)	8x8	5x5
Audio DAC output	2-channel	2-channel
DAC (single-ended) SNR at 2.8V (dB)	-98	-98
DAC (capless) SNR at 2.8V (dB)	-96	-96
ADC SNR at 2.8V (dB)	-92	-92
I ² S digital output	Yes	Yes
Analog out	Yes	Yes
Analog AUX-In	Yes	Yes
Mono microphone	1	2
External audio amplifier interface	Yes	Yes
UART	Yes	Yes
Full-speed USB 1.1	Yes	No
LED driver	3	2
Integrated DC-DC step-down regulator	1	1
Integrated LDO Regulator	2	2
DC 5V adaptor input	Yes	Yes
Battery charger (350 mA max)	Yes	Yes
ADC for thermal charger protection	Yes	Yes
Under-voltage protection (UVP)	Yes	Yes
GPIO	14	9
EEPROM	256K	256K
Multitone	Yes	Yes
DSP functions (audio playback and voice call)	Yes	Yes
BLE	Yes	Yes
Bluetooth profiles		
HFP	1.6	1.6
HSP	1.2	1.2
A2DP	1.3	1.3
SPP	1.2	1.2
AVRCP	1.6	1.6

Figure 2 illustrates the pin diagram of the IS2064S SoC.

FIGURE 2: IS2064S SoC PIN DIAGRAM



IS2064S/B

Figure 3 illustrates the pin diagram of the IS2064B SoC.

FIGURE 3: IS2064B SoC PIN DIAGRAM

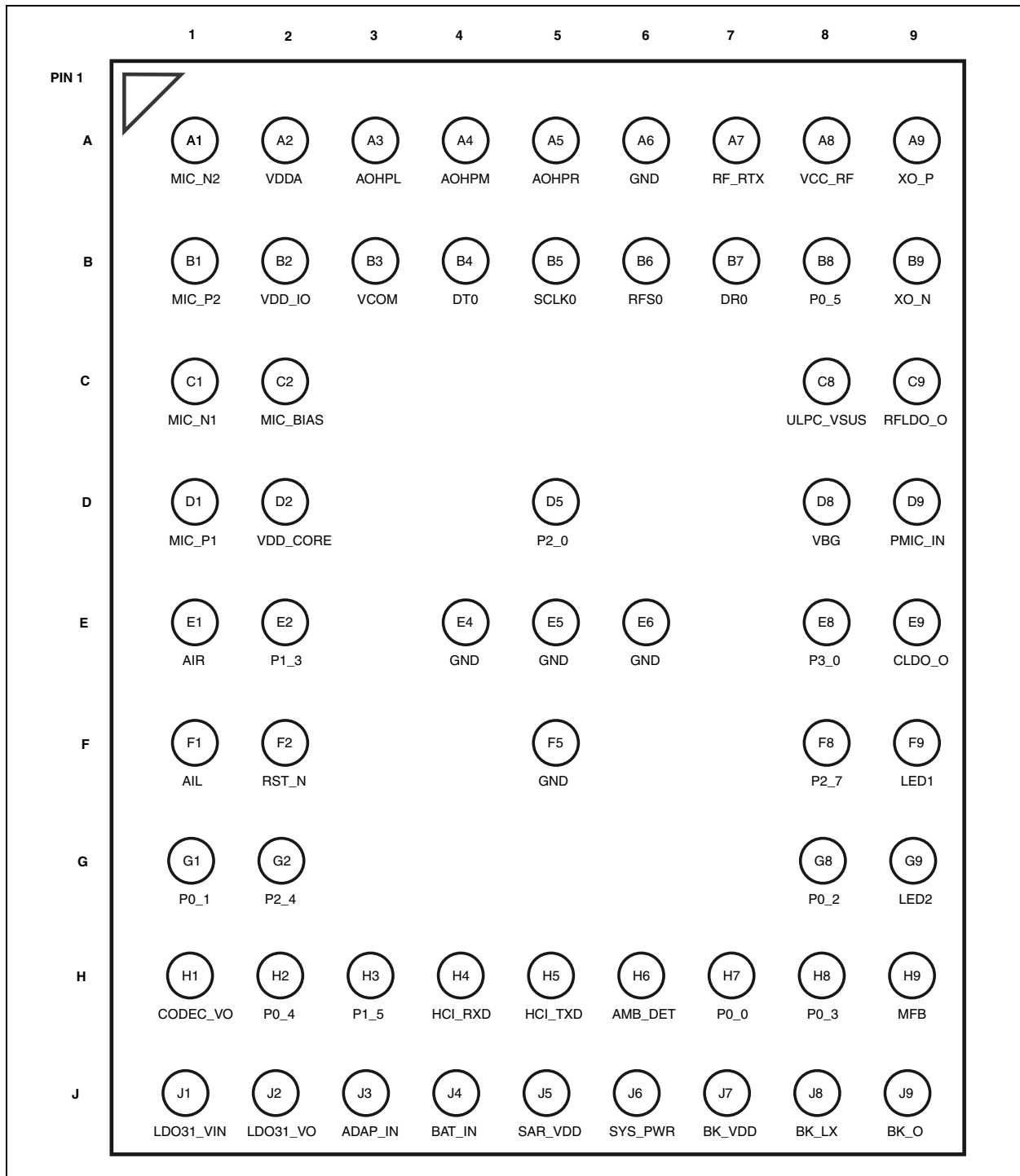


Table 3 provides the pin description of the IS2064S and IS2064B SoCs.

TABLE 3: PIN DESCRIPTION

IS2064S Pin No	IS2064B Ball No	Type	Name	Description
1	—	P	VDDAO	Power supply (3.0V to 3.6V) dedicated to codec output amplifiers; connect to the CODEC_VO pin
2	A4	O	AOHPM	Headphone common mode output/sense input
3	A3	O	AOHPL	Left channel analog headphone output
4	A2	P	VDDA	Power supply (3.0V to 3.6V) or reference voltage for external codec; connect to CODEC_VO pin
5	B3	P	VCOM	Internal biasing voltage for codec, connect a 4.7 μ F capacitor to ground
6	C1	I	MIC_N1	MIC1 mono differential analog negative input
7	D1	I	MIC_P1	MIC1 mono differential analog positive input
—	A1	I	MIC_N2	MIC2 mono differential analog negative input
—	B1	I	MIC_P2	MIC2 mono differential analog positive input
8	C2	P	MIC_BIAS	Electric microphone biasing voltage
9	E1	I	AIR	Right channel, single-ended analog input
10	F1	I	AIL	Left channel, single-ended analog input
11	D2	P	VDD_CORE	Core 1.2V power input; connect to CLDO_O pin; connect to GND through a 1 μ F (X5R/X7R) capacitor
12	—	O	P1_2	I ² C SCL (Internal EEPROM clock), do not connect
13	E2	I/O	P1_3	I ² C SDA (Internal EEPROM data), requires external 4.7K Ω pull-up resistor
14	F2	I	RST_N	System Reset (active-low)
15	B2	P	VDD_IO	I/O power supply input (3.0V to 3.6V); connect to LDO31_VO; connect to GND through a 1 μ F (X5R/X7R) capacitor
16	G1	I/O	P0_1	Configurable control or indication pin (Internally pulled up, if configured as an input) <ul style="list-style-type: none"> FWD key when Class 2 RF (default), active-low Class1 Tx control signal for external RF Tx/Rx switch, active-high
17	G2	I/O	P2_4	Do not connect
18	H2	I/O	P0_4	Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> Out_Ind_1
19	H3	I	P1_5	Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> Slide switch detector, active-high Out_Ind_1 Master/Slave mode control
20	H4	O	HCI_RXD	HCI UART data input
21	H5	I	HCI_TXD	HCI UART data output
22	H1	P	CODEC_VO	LDO output for codec power
23	J1	P	LDO31_VIN	LDO input, connect to SYS_PWR
24	J2	I	LDO31_VO	3V LDO output for VDD_IO power, do not calibrate
25	J3	P	ADAP_IN	5V power adapter input

IS2064S/B

TABLE 3: PIN DESCRIPTION

IS2064S Pin No	IS2064B Ball No	Type	Name	Description
26	J4	P	BAT_IN	Battery input, voltage range: 3.2V to 4.2V When an external power supply is connected to the ADAP_IN pin, the BAT_IN pin can be left open if battery is not connected
27	H6	P	AMB_DET	Analog input for ambient temperature detection
28	J5	P	SAR_VDD	SAR 1.8V input; connect to the BK_O pin
29	J6	P	SYS_PWR	System power output derived from the BAT_IN or ADAP_IN pin
30	J7	I	BK_VDD	1.8V buck VDD power input; connect to the SYS_PWR pin
31	J8	I	BK_LX	1.8V buck regulator feedback path
32	J9	I	BK_O	1.8V buck regulator output
33	H9	P	MFB	<ul style="list-style-type: none"> Multi-Function Button and power-on key UART RX IND, active-high (used by host MCU to wake-up the Bluetooth system)
34	—	P	LED3	LED driver 3
35	G9	P	LED2	LED driver 2
36	F9	P	LED1	LED driver 1
37	—	P	P3_7	Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> UART TX_IND, active-low (used by Bluetooth system to wake-up the host MCU)
38	—	P	P3_5	Configurable control or indication pin (Internally pulled up if configured as an input)
39	H7	I/O	P0_0	Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> Slide switch detector, active-high
40	H8	I/O	P0_3	Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> REV key (default), active-low Buzzer signal output Out_Ind_2 Class 1 Rx control signal of external RF T/R switch, active-high
41	—	I/O	EAN	Do not connect
42	—	P	AVDD_USB	USB power input; connect to LDO31_VO pin
43	—	I/O	DM	Differential data-minus USB
44	—	I/O	DP	Differential data-plus USB
45	E9	P	CLDO_O	1.2V core LDO output for internal use only. Connect to GND through a 1 μ F capacitor
46	D9	P	PMIC_IN	1.8V power input for internal blocks; connect to BK_O
47	C9	P	RFLDO_O	1.28V RF LDO output for internal use only. Connect to GND through a 1 μ F capacitor
48	D8	P	VBG	Bandgap output reference for decoupling interference, connect to GND through a 1 μ F capacitor
49	C8	P	ULPC_V-SUS	ULPC 1.2V output power, maximum loading 1 mA, connect to GND through a 1 μ F capacitor
50	B9	I	XO_N	16 MHz crystal input negative
51	A9	I	XO_P	16 MHz crystal input positive

TABLE 3: PIN DESCRIPTION

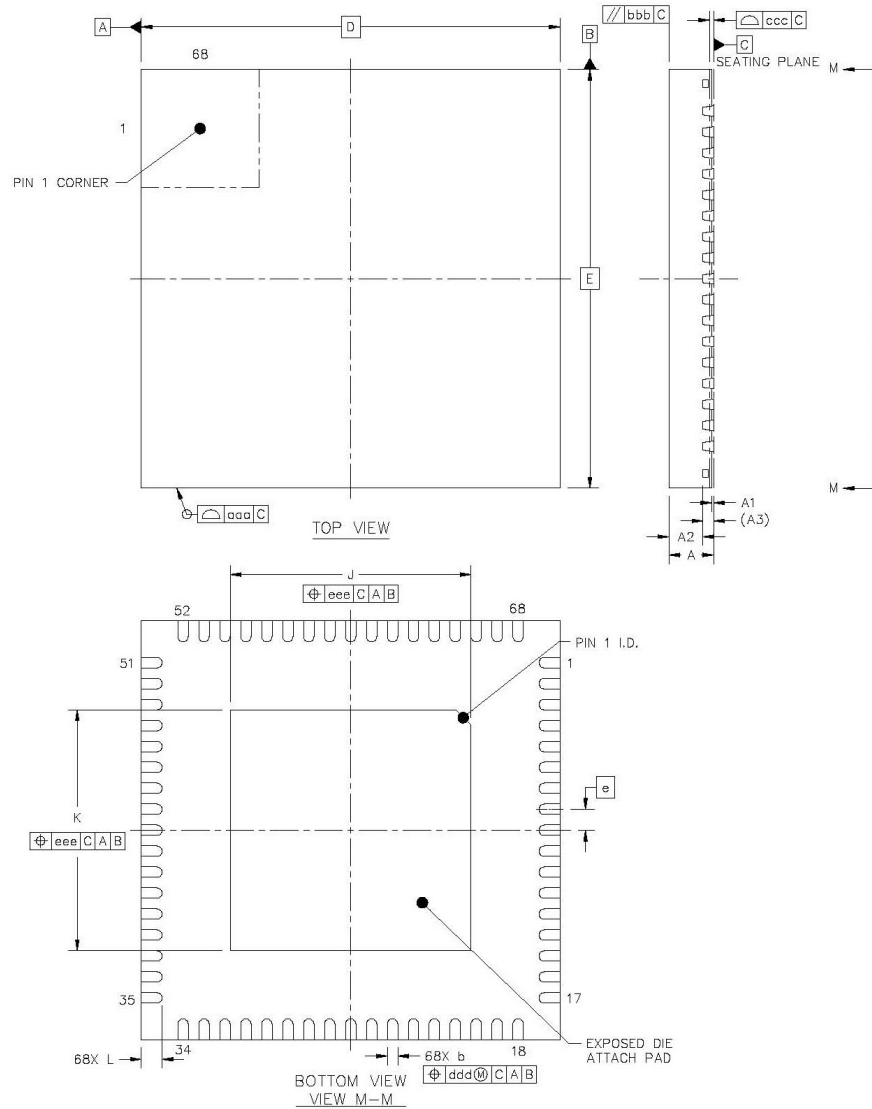
IS2064S Pin No	IS2064B Ball No	Type	Name	Description
52	A8	P	VCC_RF	RF power input (1.28V) for both synthesizer and Tx/Rx block, connect to RFLDO_O
53	A7	I/O	RTX/ RF_RTX	RF path (transmit/receive)
54	—	I/O	P3_1	Configurable control or indication pin (Internally pulled up if configured as an input) • REV key when Class 1 RF (default), active-low
55	—	I/O	P3_3	Configurable control or indication pin (Internally pulled up if configured as an input) • FWD key when Class 1 RF (default), active-low
56	—	I/O	P3_6	Configurable control or indication pin (Internally pulled up if configured as an input) • Master/Slave mode control
57	G8	I/O	P0_2	Configurable control or indication pin (Internally pulled up if configured as an input) • Play/Pause key (default)
58	D5	I/O	P2_0	System configuration pin to configure the SoC in any one of the following modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) Buzzer signal output
59	F8	I/O	P2_7	Configurable control or indication pin (Internally pulled up if configured as an input) • Volume up key (default), active-low
60	E8	I/O	P3_0	Configurable control or indication pin (Internally pulled up if configured as an input) • AUX-In detector, active-low
61	—	I/O	TFS0	I ² S interface: left/right clock
62	B8	I/O	P0_5	Configurable control or indication pin (Internally pulled up if configured as an input) • Volume down key (default), active-low
63	B2	P	VDD_IO	I/O power supply input (3V to 3.6V); connect to LDO31_VO pin, connect to GND through a 1 μF (X5R/X7R) capacitor
64	B7	I/O	DR0	I ² S interface: digital left/right data
65	B6	I/O	RFS0	I ² S interface: left/right clock
66	B5	I/O	SCLK0	I ² S interface: bit clock
67	B4	I/O	DT0	I ² S interface: digital left/right data
68	A5	O	AOHPR	Headphone output, right channel
69-83	—	P	EP	Exposed pads, used as ground (GND) pins
—	A6, E4, E5, E6, F5	P	GND	Ground reference

Legend: I= Input pin O= Output pin I/O= Input/Output pin P= Power pin

Note: All I/O pins can be configured using the UI tool, a Windows-based utility.

Figure 4 illustrates the package details of the IS2064S SoC.

FIGURE 4: IS2064S SoC PACKAGE DETAILS

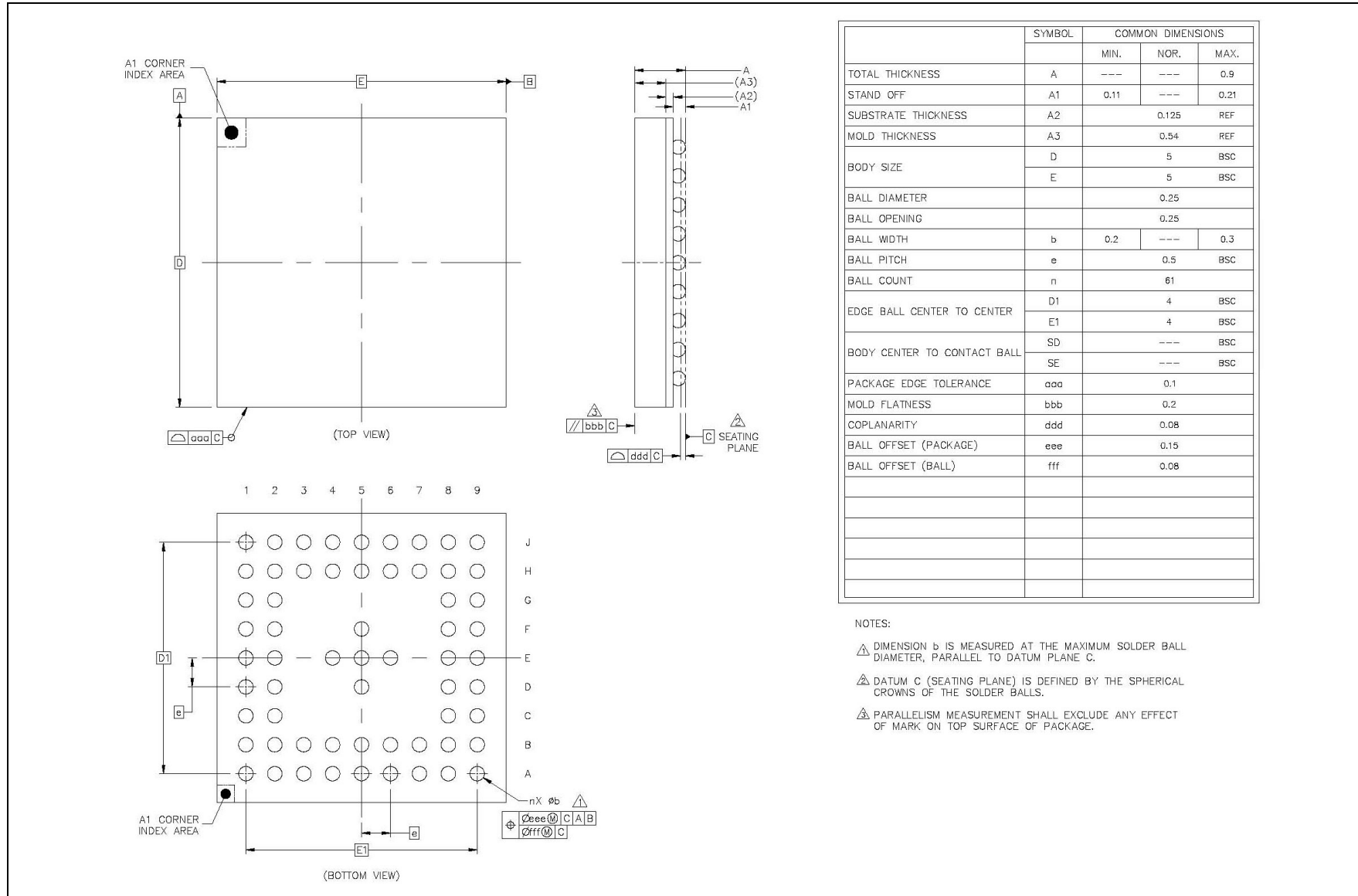


	SYMBOL	MIN	NOM	MAX	
TOTAL THICKNESS	A	0.8	0.85	0.9	
STAND OFF	A1	0	0.035	0.05	
MOLD THICKNESS	A2	---	0.65	0.67	
L/F THICKNESS	A3	0.203 REF			
LEAD WIDTH	b	0.15	0.2	0.25	
BODY SIZE	X	8 BSC			
	Y	8 BSC			
LEAD PITCH	e	0.4 BSC			
EP SIZE	X	J	4.5	4.6	4.7
	Y	K	4.5	4.6	4.7
LEAD LENGTH	L	0.35	0.4	0.45	
PACKAGE EDGE TOLERANCE	aaa	0.1			
MOLD FLATNESS	bbb	0.1			
COPLANARITY	ccc	0.08			
LEAD OFFSET	ddd	0.1			
EXPOSED PAD OFFSET	eee	0.1			

NOTES
 1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 5 illustrates the package details of the IS2064B SoC.

FIGURE 5: IS2064B SoC PACKAGE DETAILS



IS2064S/B

NOTES:

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ISBN: 978-1-5224-1466-7



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