OS81210

Intelligent Network Interface Controller for 50 Mbit/s Automotive Networks Product Brief

Features

- Complete 50 Mbit/s synchronous network interface
- Embedded network management functions
  - Network protection mode
  - Hardware & application watchdog timer
  - Intelligent muting
  - Diagnostics
  - Emergency Response System (eCall)
- IEEE MAC addressing and Ethernet channel
- Universal Serial Bus (USB) Port supports USB 2.0 High-speed upstream data transfers using either:
  - USB 2.0 physical layer
  - High-Speed Inter-Chip (HSIC) physical layer
- Media Local Bus (MediaLB®) Port
  - Eases inter-chip communication and streaming
  - MediaLB 3-pin interface at speeds up to 1024xFs
- I²C™ Control Port inter-chip message exchange
- Streaming Port supports synchronous, fixed latency data exchange for a variety of serial audio formats including time-division multiplex (TDM) and pulse density modulation (PDM)
- SPI Port supports asynchronous and control packets
- General Purpose I/O (GPIO) Port
- Remote control and configuration for operation without a local External Host Controller.
  - I²C (master) message tunneling
  - GPIO port control
- Operating voltages 3.3 V/1.8 V (and 1.2 V for HSIC)
- Available in 64-pin QFN package with exposed pad
- -40 to +125 °C junction temperature

Conformity

- This document applies to hardware revision B1A

Applications

- Automotive infotainment network nodes including head unit, instrument cluster, amplifier, and rear seat entertainment.

General Description

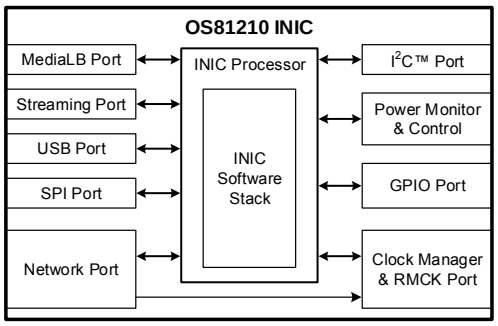
The OS81210 is a highly integrated *Intelligent Network Interface Controller* (INIC) for 50 Mbit/s INICnet-based automotive networks with a transformer-less balanced media physical layer (bPHY) optimized for unshielded twisted pair (UTP) copper wire.

The INIC provides encapsulation of all low-level functions necessary to develop a network-compliant device, significantly simplifying network implementation in a node. Integration of the *INIC Software Stack* into the INIC provides network-compliant real-time behavior. The *INIC Software Stack* significantly relieves the External Host Controller (EHC) from real-time processing tasks. Supervision of the application is also provided, including a protection mode that is entered when an application is not present (i.e. start-up) or the EHC malfunctions. This protection mode prevents application malfunctions from influencing the integrity of the network and the system.

When the EHC is engaged, a message-based interface, as opposed to a register-based interface, is available for communication with INIC. A unified and centralized network management software stack (UNICENS) is available for the EHC to build a complete, lean, system solution.

The INIC can also support a fully compliant MOST® network.

FIGURE: OS81210 BLOCK DIAGRAM



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1.0 PINOUT

FIGURE 1-1: OS81210 PIN DIAGRAM

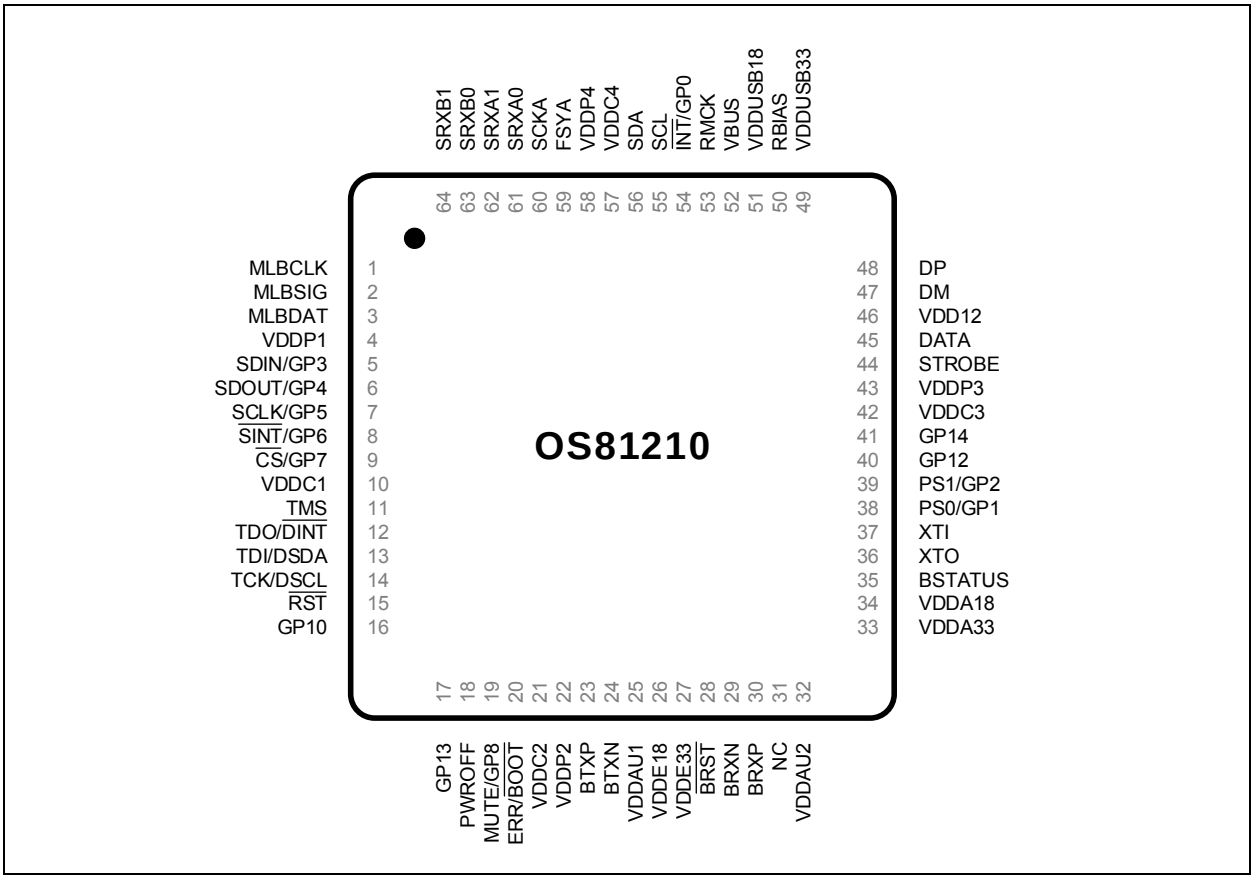


TABLE 1-1: OS81210 PIN ALLOCATION TABLE

Pin	Name	HW Port	Description
1	MLBCLK [2]	MediaLB	Singled-ended Clock line for MediaLB 3-pin Interface
2	MLBSIG [2]	MediaLB	Singled-ended Signal line for MediaLB 3-pin Interface
3	MLBDAT [2]	MediaLB	Singled-ended Data line for MediaLB 3-pin Interface
4	VDDP1		3.3 V periphery power supply (digital)
5	SDIN	SPI	Data In (MOSI - Master Out, Slave In)
	GP3	GPIO	General Input/Output 3
6	SDOUT	SPI	Data Out (MISO - Master In, Slave Out)
	GP4	GPIO	General Purpose Input/Output 4
7	SCLK	SPI	Clock
	GP5	GPIO	General Purpose Input/Output 5
8	$\overline{\text{SINT}}$	SPI	Interrupt (active low)
	GP6	GPIO	General Purpose Input/Output 6
9	$\overline{\text{CS}}$	SPI	Chip Select (active low)
	GP7	GPIO	General Purpose Input/Output 7
10	VDDC1		1.8 V core power supply (digital)
11	TMS [1]	JTAG	Test Mode Select

Note 1: Pull-up resistor required.

2: Pull-down resistor required.

TABLE 1-1: OS81210 PIN ALLOCATION TABLE (CONTINUED)

Pin	Name	HW Port	Description
12	TDO [1]	JTAG	Test Data Output
	$\overline{\text{DINT}}$ [1]		Debug Interrupt (active low)
13	TDI [1]	JTAG	Test Data Input
	DSDA [1]		Debug Data
14	TCK [1]	JTAG	Test Clock Input
	DSCL [1]		Debug Clock
15	$\overline{\text{RST}}$		Hardware Reset Input (active low). (Pull-up resistor to **VDDPn** supply should be used when not driven high by an external device. A series resistor should be used in lieu of the pull-up when always driven by an external device.)
16	GP10	GPIO	General Purpose Input/Output 10
17	GP13	GPIO	General Purpose Input/Output 13
18	PWROFF [1]		External Power Management Power-Down Indicator. This pin is driven low by INIC after initialization. When high, indicates that the INIC Processor is ready to be shut down. A pull-up resistor is required when used. If not used, this pin may be left unconnected.
19	MUTE [1]		Mute Indicator Output. A pull-up resistor is required when used. If not used, this pin may be left unconnected.
	GP8	GPIO	General Purpose Input/Output 8
20	ERR	Network	Network Error Indicator Output. This pin is driven high when the network is unlocked. When low, this pin indicates the INIC is locked to the network.
	$\overline{\text{BOOT}}$ [1]		Configuration Pin. This pin is attached to the configuration/debug header and used by the Microchip *INICkit Tool* to load initial configuration data into INIC. May also be connected to the EHC to allow in-system configuration of the INIC.
21	VDDC2		1.8 V core power supply (digital)
22	VDDP2		3.3 V periphery power supply (digital)
23	BTXP	Network	Positive (differential) bPHY network transmitter output
24	BTXN	Network	Negative (differential) bPHY network transmitter output
25	VDDAU1		3.3 V continuous power supply (analog)
26	VDDE18		1.8 V bPHY power supply (analog)
27	VDDE33		3.3 V bPHY power supply (analog)
28	$\overline{\text{BRST}}$	Network	Hardware Reset Input (active low) for the Balanced Media Physical Layer. When asserted, the transmitter output is disabled.
29	BRXN	Network	Negative (differential) bPHY network receiver input
30	BRXP	Network	Positive (differential) bPHY network receiver input
31	NC		No Connect. This pin must be left open and floating.
32	VDDAU2		3.3 V continuous power supply (analog)
33	VDDA33		3.3 V power supply (analog)
34	VDDA18		1.8 V power supply (analog)
35	BSTATUS	Network	bPHY Network Activity Status Output: - Driven low when a valid signal is detected - Driven high to **VDDAUn** when a qualified signal is not present
36	XTO		Crystal Oscillator Output
37	XTI		Crystal Oscillator Input or External CMOS Clock Input
38	PS0		External Power Management Status Bit 0
	GP1	GPIO	General Purpose Input/Output 1

Note 1: Pull-up resistor required.

2: Pull-down resistor required.

TABLE 1-1: OS81210 PIN ALLOCATION TABLE (CONTINUED)

Pin	Name	HW Port	Description
39	PS1		External Power Management Status Bit 1
	GP2	GPIO	General Purpose Input/Output 2
40	GP12	GPIO	General Purpose Input/Output 12
41	GP14	GPIO	General Purpose Input/Output 14
42	VDDC3		1.8 V core power supply (digital)
43	VDDP3		3.3 V periphery power supply (digital)
44	STROBE	USB	Strobe line for HSIC physical interface. Connect to **GND** when HSIC is not used.
45	DATA	USB	Data line for HSIC physical interface. Connect to **GND** when HSIC is not used.
46	VDD12		1.2 V power supply for HSIC physical interface transceiver. Connect to **GND** through a 1 kΩ resistor when HSIC is not used.
47	DM	USB	Negative (differential) data line for USB physical interface. Connect to **GND** when the USB physical interface is not used.
48	DP	USB	Positive (differential) data line for USB physical interface. Connect to **GND** when the USB physical interface is not used.
49	VDDUSB33		3.3 V USB power supply (analog)
50	RBIAS [2]	USB	Connect to **GND** through a 12 kΩ resistor (0.5 %, 1/16 W, ≤ ± 100 ppm). This pin may be left unconnected when both the USB and HSIC physical interfaces are not used.
51	VDDUSB18		1.8 V USB power supply (analog)
52	VBUS	USB	USB Bus Power State Indicator Input. The application should drive this pin high when an external USB Host Controller is present. Note that this pin is not 5 V tolerant and must not be connected directly to USB bus power. This signal is ignored when using the HSIC physical interface. Connect to **GND** when the USB physical interface is not used.
53	RMCK	RMCK	Recovered Master Clock Output
54	$\overline{INT}$ [1]	I^2C	Interrupt (active low). Indicates a service request from the EHC when the Control Port is operating as an I^2C slave.
	GP0	GPIO	General Purpose Input/Output 0
55	SCL [1]	I^2C	Clock
56	SDA [1]	I^2C	Data
57	VDDC4		1.8 V core power supply (digital)
58	VDDP4		3.3 V periphery power supply (digital)
59	FSYA	Streaming	Frame Sync for Streaming Port A and B
60	SCKA	Streaming	Bit Clock for Streaming Port A and B
61	SRXA0	Streaming	Data I/O Signal 0 for Streaming Port A
62	SRXA1	Streaming	Data I/O Signal 1 for Streaming Port A
63	SRXB0	Streaming	Data I/O Signal 0 for Streaming Port B
64	SRXB1	Streaming	Data I/O Signal 1 for Streaming Port B
ePAD	GND		The exposed paddle on the bottom side of the QFN package is the primary ground for the OS81210 and must be connected to ground on the PCB for proper operation.

Note 1: Pull-up resistor required.

2: Pull-down resistor required.

2.0 BASIC APPLICATION INFORMATION

The OS81210 and OS81212/4/6 INICs are part of the OS8121x 50 Mbit/s INICnet product family that support point-to-point, simplex daisy chain, and ring topologies through an integrated balanced media physical layer (bPHY). The integrated *INIC Software Stack* can independently run the network and manage the low-level protocols such as startup, shutdown, error reporting, or Plug-and-Play node positioning. Alternatively, INIC can operate in conjunction with an External Host Controller (EHC) managing the mid- and high-level functions. Additionally the OS81210 provides power management capabilities and industry standard application interfaces such a USB 2.0, MediaLB 3-Pin, Streaming Port, I^2C Port, SPI port, and GPIOs.

The OS81210 is optimized for high performance head unit applications with USB 2.0 or HSIC high-speed communication.

The OS81212 is targeted for audio / video streaming data applications with the dual Streaming Ports and MediaLB interface. It can operate with an EHC or it can exist remotely on the network.

The OS81214 is targeted for audio data applications using the Streaming Port or packets over the SPI Port. It can operate with an EHC or it can exist remotely on the network.

The OS81216 INIC is targeted for remotely configured microphone applications (without a local EHC).

FIGURE 2-1: OS8121x PRODUCT FAMILY OVERVIEW

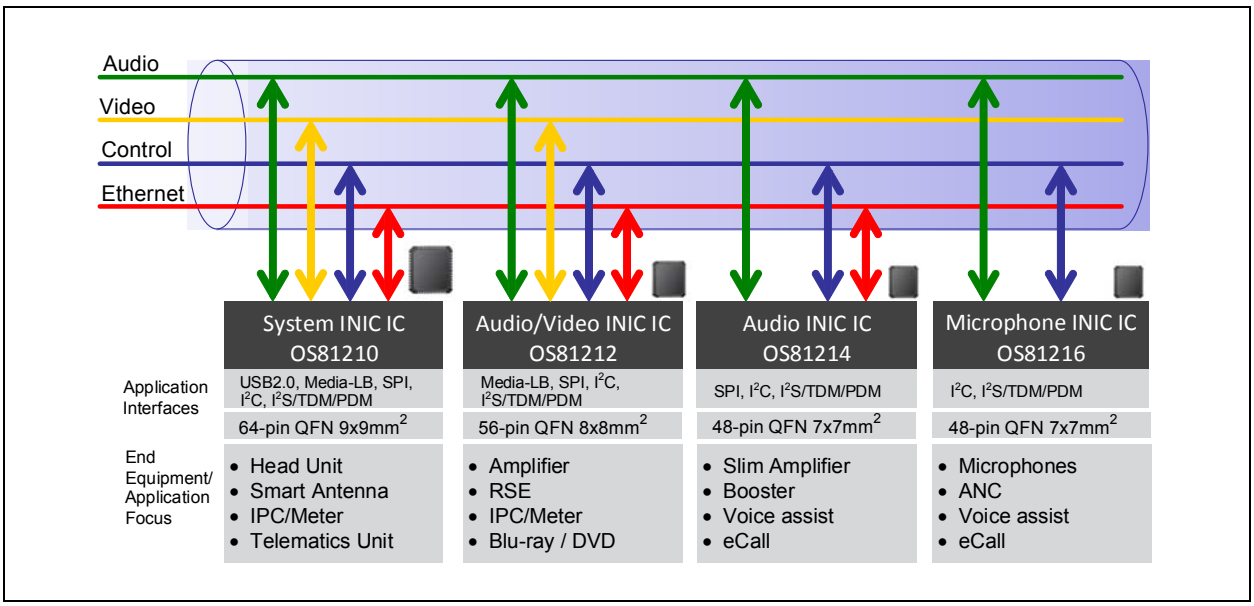
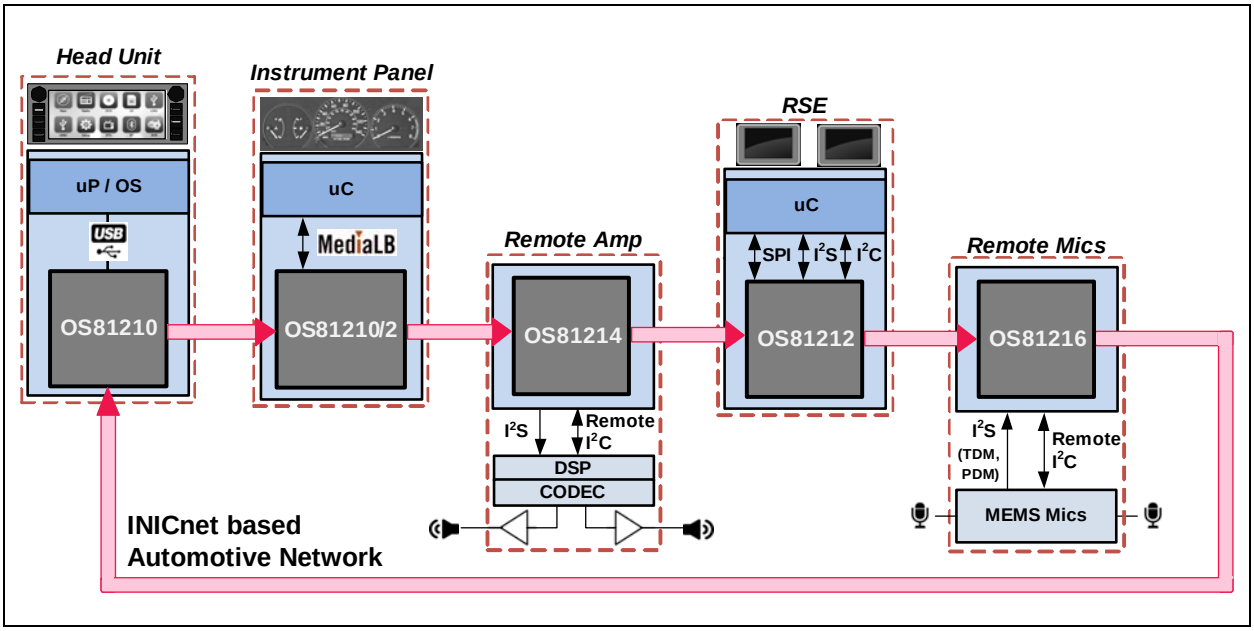


Figure 2-2 depicts an example 50 Mbit/s INICnet application. Using a combination of OS81210 and OS81212/4/6 INICs, a system supporting audio, video, and packet data applications can be easily configured. The Head Unit INIC can communicate with an operating system (such as a GNU/Linux, QNX, Android Auto, etc.) to manage the network and control the remote nodes. The asynchronous channel on the INIC can be used for high-speed routing of application packet data such as graphics images, system information, or software downloads. The EHC can access both synchronous and packet data through the OS81210 USB interface. An Instrument Panel can be implemented with control and Ethernet packets sent over the OS81210/2 MediaLB Port. Without a local EHC, the microphones are configured remotely over I^2C. Only a single INIC streaming pin is used to source a mono PDM bit stream from a MEMS microphone to the network. As shown in the Remote Amp, the amplifier is remotely controlled and configured. Synchronous audio data is routed over the network and is sourced/sinked through I^2S to CODECs or DSPs. The Rear Seat Entertainment (RSE) can route synchronous streams or asynchronous data such a IP packets over the network Ethernet Channel.

FIGURE 2-2: BASIC APPLICATION DIAGRAM



3.0 PACKAGING INFORMATION

3.1 Package Marking

FIGURE 3-1: OS81210 TOP MARKING

The package designators are:

- xx - Device Identifier
  - **OS81210AF** - Solderable Flank QFN
- rrr - Product Revision Code
- yy - last two digits of Assembly Year
- ww - Assembly Work Week
- nnn - Tracking Number
- cc - Country of Origin Abbreviation (optional - up to 2 characters)
- e3 - Pb Free Symbol

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	[X]	-	rrr	-	vvvvvv	[ss]	-	[xxx]
Device	Grade	Package Type	Tape and Reel Flag		Product Revision Code		Firmware Revision Code	Firmware Service Release		Special Feature Code

Device	OS81210	=	50 Mbit/s Automotive Intelligent Network Interface Controller with USB
Grade	A	=	All Features
Package Type	F	=	QFN with solderable flanks
Tape and Reel Flag (optional)	Blank R	= =	Standard Packaging (Tube/Tray) Tape and Reel
Product Revision Code	rrr	=	3 character code specifying product revision
Firmware Revision Code	vvvvvv	=	6 character code specifying firmware revision
Firmware Service Release (optional)	ss	=	2 character code specifying service release
Special Feature Code (optional)	xxx	=	3 character code for special requirements

Examples:

a) OS81210AF-rrr-vvvvvv-xxx
64-pin solderable flank QFN package

b) OS81210AFR-rrr-vvvvvv-xxx
64-pin solderable flank QFN package,
Tape and Reel

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