LAN83C185

High Performance Single Chip Low Power 10/100 Ethernet Physical Layer Transceiver (PHY)

PRODUCT FEATURES

Data Brief

- Single Chip Ethernet Phy
- Fully compliant with IEEE 802.3/802.3u standards
- 10BASE-T and 100BASE-TX support
- Supports Auto-negotiation and Parallel Detection
- Automatic Polarity Correction
- Integrated DSP with Adaptive Equalizer
- Baseline Wander (BLW) Correction
- Media Independent Interface (MII)
- 802.3u compliant register functions
- Vendor Specific register functions
- Comprehensive power management features
- General power-down mode
- Energy Detect power-down mode
- Low profile 64-pin TQFP package; lead-free RoHS compliant package also available
- Single +3.3V supply with 5V tolerant I/O
- 0.18 micron technology
- Low power consumption
- Operating Temperature 0° C to 70° C
- Internal +1.8V Regulator

Applications

- LAN on Motherboard
- 10/100 PCMCIA/CardBus Applications
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems And Set-Top Boxes
- Digital Televisions
- Wireless Access Points

ORDER NUMBERS:

LAN83C185-JD FOR 64-PIN TQFP PACKAGE

LAN83C185-JT FOR 64-PIN TQFP LEAD-FREE ROHS COMPLIANT PACKAGE

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

General Description

The SMSC LAN83C185 is a low-power, highly integrated analog interface IC for high-performance embedded Ethernet applications. The LAN83C185 requires only a single +3.3V supply.

The LAN83C185 consists of an encoder/decoder, scrambler/descrambler, transmitter with wave-shaping and output driver, twisted-pair receiver with on-chip adaptive equalizer and baseline wander (BLW) correction, clock and data recovery, and Media Independent Interface (MII).

The LAN83C185 is fully compliant with IEEE 802.3/ 802.3u standards and supports both 802.3u-compliant and vendor-specific register functions. It contains a full-duplex 10-BASET/100BASE-TX transceiver and supports 10-Mbps (10BASE-T) operation on Category 3 and Category 5 unshielded twisted-pair cable, and 100-Mbps (100BASE-TX) operation on Category 5 unshielded twisted-pair cable.

Block Diagram

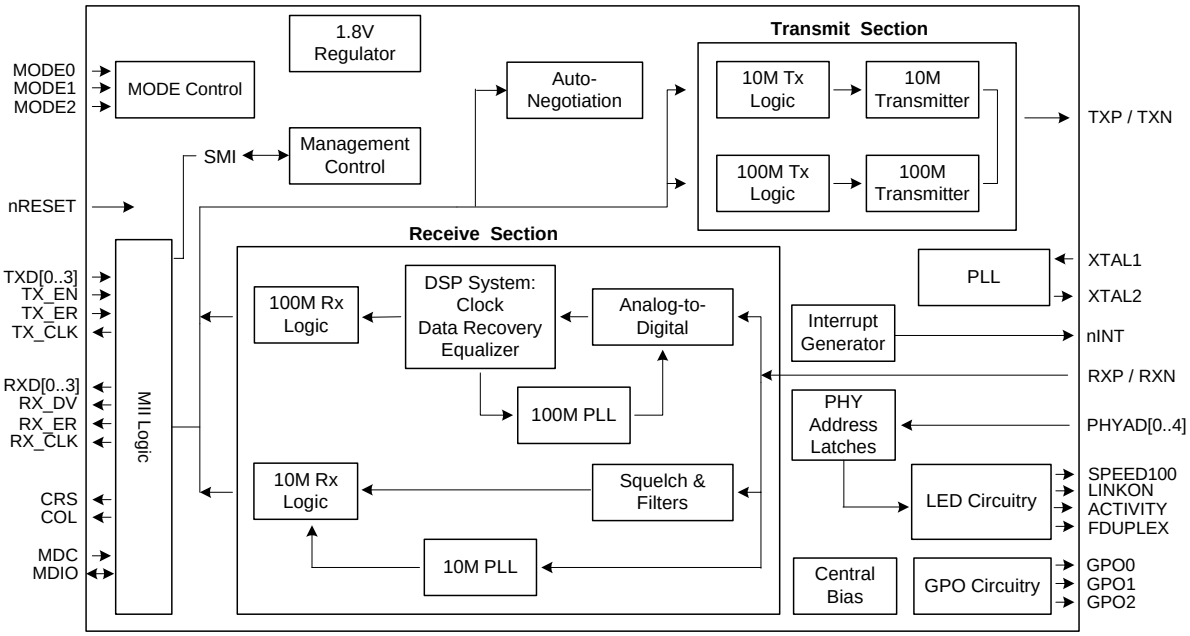

Figure 1 LAN83C185 Architectural Overview

Package Outline

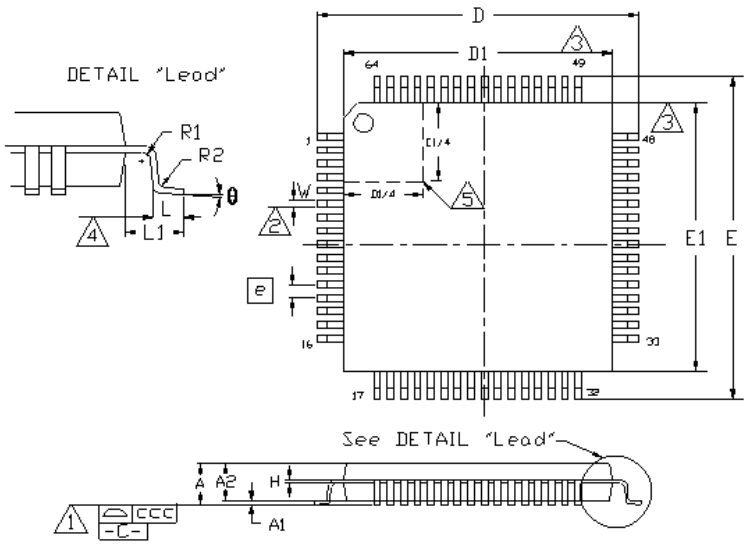

Figure 2 64 Pin TQFP Package Outline, 10X10X1.4 Body, 2 MM Footprint

Table 1 64 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	11.80	~	12.20	X Span
D1	9.80	~	10.20	X body Size
E	11.80	~	12.20	Y Span
E1	9.80	~	10.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm per side.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.