LAN9116

Highly Efficient Single-Chip 10/100 Non-PCI Ethernet Controller

PRODUCT FEATURES

Data Brief

Highlights

- Member of LAN9118 Family; optimized for medium-high performance applications
- Easily interfaces to most 32-bit and 16-bit embedded CPU's
- Efficient architecture with low CPU overhead
- Integrated PHY
- Supports audio & video streaming over Ethernet: 1-2 high-definition (HD) MPEG2 streams
- Medium-high speed member of LAN9118 Family (all members are pin-compatible)

Target Applications

- Medium-range Cable, satellite, and IP set-top boxes
- Digital video recorders and DVD recorders/players
- High definition televisions
- Digital media clients/servers and home gateways
- Video-over IP Solutions, IP PBX & video phones
- Wireless routers & access points

Key Benefits

- Non-PCI Ethernet controller for medium-high performance applications
  - 32-bit interface
  - Burst-mode read support
- Eliminates dropped packets
  - Internal buffer memory can store over 200 packets
  - Supports automatic or host-triggered PAUSE and back-pressure flow control
- Minimizes CPU overhead
  - Supports Slave-DMA
  - Interrupt Pin with Programmable Hold-off timer
- Reduces system cost and increases design flexibility
  - SRAM-like interface easily interfaces to most embedded CPU's or SoC's
  - Low-cost, low--pin count non-PCI interface for embedded designs
- Reduced Power Modes
  - Numerous power management modes
  - Wake on LAN*
  - Magic packet wakeup*
  - Wakeup indicator event signal
  - Link Status Change
- Single chip Ethernet controller
  - Fully compliant with IEEE 802.3/802.3u standards
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and Half-duplex support
  - Full-duplex flow control
  - Backpressure for half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
- Flexible address filtering modes
  - One 48-bit perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast
  - Promiscuous mode
  - Inverse filtering
  - Pass all incoming with status report
  - Disable reception of broadcast packets
- Integrated Ethernet PHY
  - Auto-negotiation
  - Automatic polarity detection and correction
- High-Performance host bus interface
  - Simple, SRAM-like interface
  - 32/16-bit data bus
  - Large, 16Kbyte FIFO memory that can be allocated to RX or TX functions
  - One configurable host interrupt
- Miscellaneous features
  - Low profile 100-pin, TQFP lead-free RoHS Compliant package
  - Integral 1.8V regulator
  - General Purpose Timer
  - Support for optional EEPROM
  - Support for 3 status LEDs multiplexed with Programmable GPIO signals
- 3.3V Power Supply with 5V tolerant I/O
- 0 to 70°C

ORDER NUMBER:

LAN9116-MT FOR 100 PIN, TQFP LEAD-FREE ROHS COMPLIANT PACKAGE WITH E3 FINISH (MATTE TIN)

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

General Description

The LAN9116 is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9116 has been architected to provide the best price-performance ratio for any 32-bit application with medium-high performance requirements. The LAN9116 is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant.

The LAN9116 includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit and 32-bitmicroprocessors and microcontrollers. The LAN9116 includes large transmit and receive data FIFOs to accommodate high latency applications. In addition, the LAN9116 memory buffer architecture allows the most efficient use of memory resources by optimizing packet granularity.

Applications

The LAN9116 is well suited for medium-high-performance embedded applications, including:

- Medium-range cable, satellite and IP set-top boxes
- Digital video recorders
- DVD Recorders/Players
- High-definition televisions
- Digital media clients/servers
- Home gateways

The LAN9116 also supports features which reduce or eliminate packet loss. Its internal 16-KByte SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9116 can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

The LAN9116 supports numerous power management and wakeup features. The LAN9116 can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including “Magic Packet”, “Wake on LAN” and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command.

The SMSC LAN9116 integrated 10/100 MAC/PHY controller is a peripheral chip that performs the function of translating parallel data from a host controller into Ethernet packets. The LAN9116 Ethernet MAC/PHY controller is designed and optimized to function in an embedded environment. All communication is performed with programmed I/O transactions using the simple SRAM-like host interface bus.

The LAN9116 is a general purpose, platform independent, Ethernet controller. The LAN9116 consists of four major functional blocks. The four blocks are:

- 10/100 Ethernet PHY
- 10/100 Ethernet MAC
- RX/TX FIFOs
- Host Bus Interface (HBI)

Block Diagrams

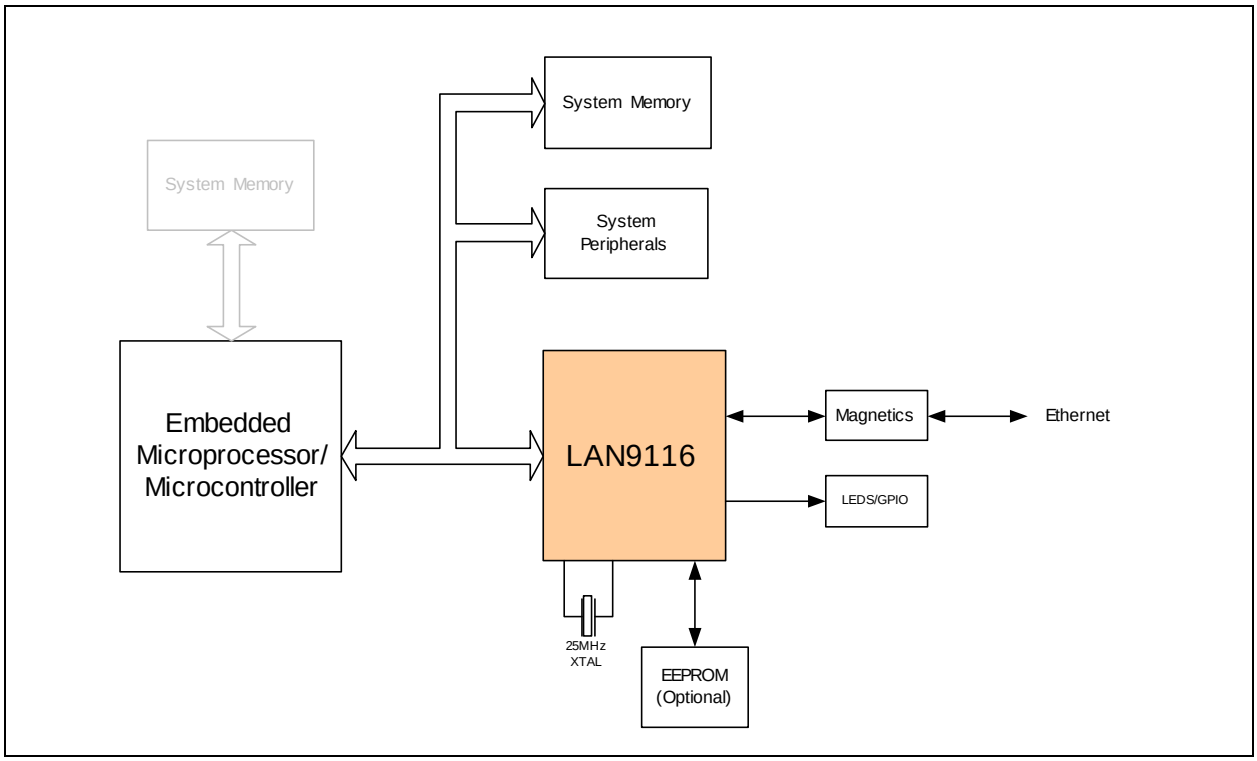


Figure 1 System Block Diagram Utilizing the SMSC LAN9116

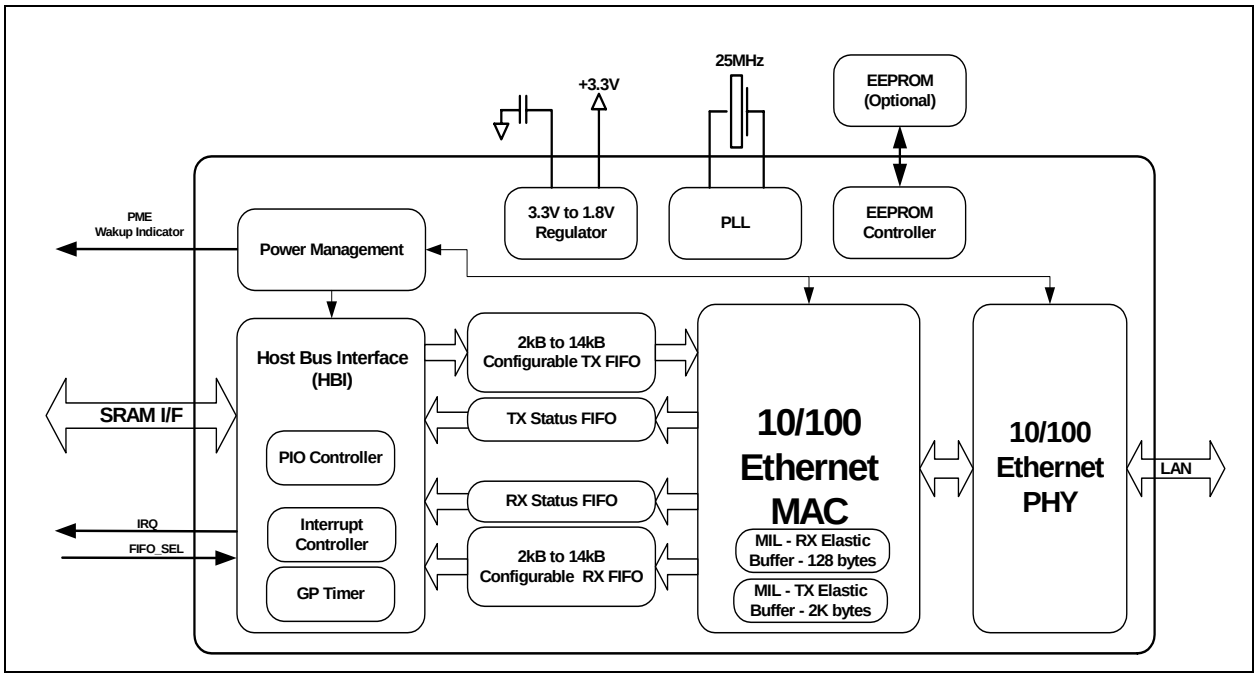
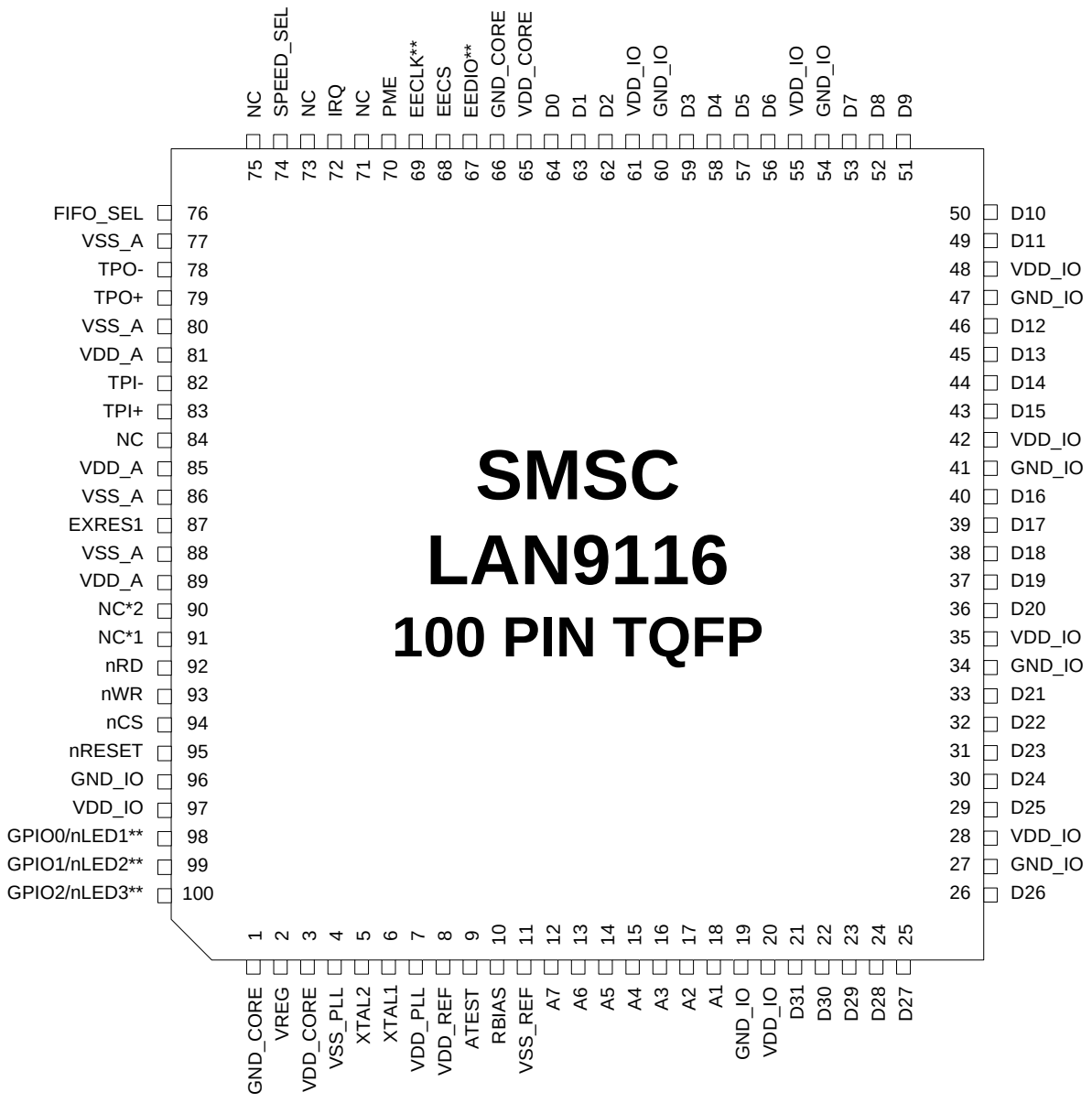


Figure 2 Internal Block Diagram

Pin Configuration



**Denotes a multifunction pin
*1 This NC pin can also be tied to VDD_A for backward compatibility
*2 This NC pin can also be tied to VSS_A for backward compatibility

Figure 3 Pin Configuration

Package Outline

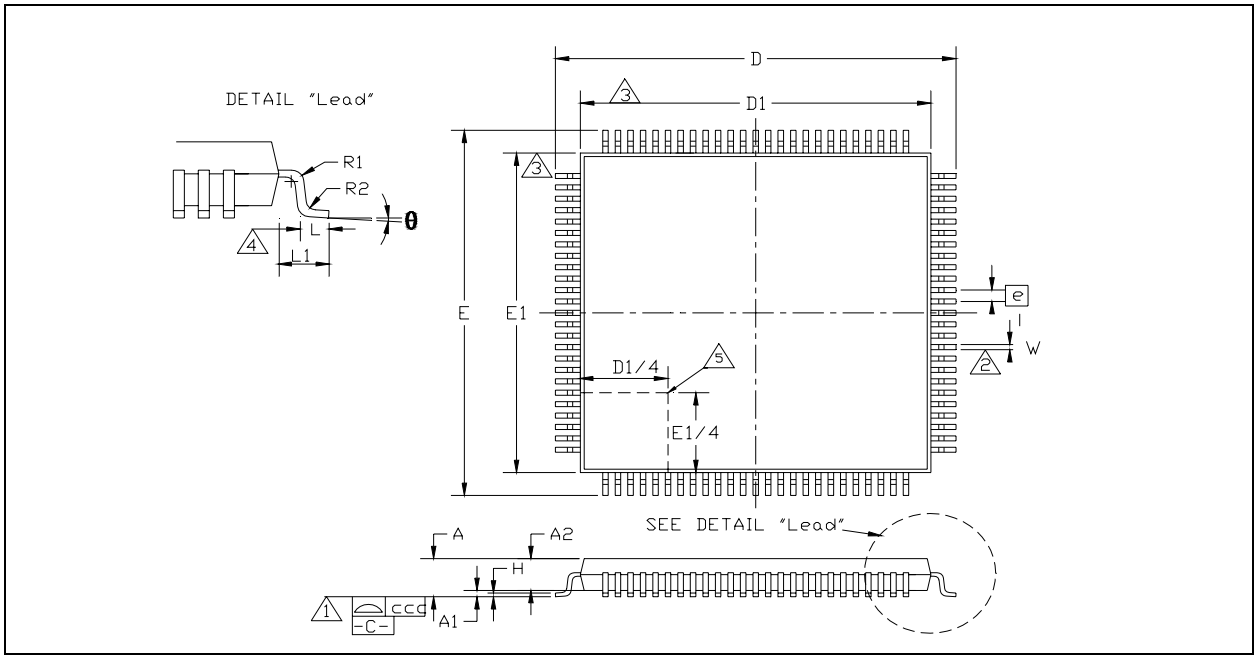


Figure 4 100 Pin TQFP Package Definition

Table 1 100 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	15.80	~	16.20	X Span
D1	13.90	~	14.10	X body Size
E	15.80	~	16.20	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.