LAN91C111

10/100 Non-PCI Ethernet Single Chip MAC + PHY

PRODUCT FEATURES

Data Brief

- Single Chip Ethernet Controller
- Dual Speed - 10/100 Mbps
- Fully Supports Full Duplex Switched Ethernet
- Supports Burst Data Transfer
- 8 Kbytes Internal Memory for Receive and Transmit FIFO Buffers
- Enhanced Power Management Features
- Optional Configuration via Serial EEPROM Interface
- Supports 8, 16 and 32 Bit CPU Accesses
- Internal 32 Bit Wide Data Path (Into Packet Buffer Memory)
- Built-in Transparent Arbitration for Slave Sequential Access Architecture
- Flat MMU Architecture with Symmetric Transmit and Receive Structures and Queues
- 3.3V Operation with 5V Tolerant IO Buffers (See Pin List Description for Additional Details)
- Single 25 MHz Reference Clock for Both PHY and MAC
- External 25Mhz-output pin for an external PHY supporting PHYs physical media.
- Low Power CMOS Design
- Supports Multiple Embedded Processor Host Interfaces
  - ARM
  - SH
  - Power PC
  - Coldfire
  - 680X0, 683XX
  - MIPS R3000
- 3.3V MII (Media Independent Interface) MAC-PHY Interface Running at Nibble Rate
- MII Management Serial Interface
- 128-Pin QFP lead-free RoHS compliant package
- 128-Pin TQFP 1.0 mm height lead-free RoHS compliant package
- Commercial Temperature Range from 0°C to 70°C (LAN91C111)
- Industrial Temperature Range from -40°C to 85°C (LAN91C111i)

Network Interface

- Fully Integrated IEEE 802.3/802.3u-100Base-TX/ 10Base-T Physical Layer
- Auto Negotiation: 10/100, Full / Half Duplex
- On Chip Wave Shaping - No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- LED Outputs (User selectable – Up to 2 LED functions at one time)
  - Link
  - Activity
  - Full Duplex
  - 10/100
  - Transmit
  - Receive

Order Numbers:

LAN91C111-NS, LAN91C111i-NS (Industrial Temperature)

for 128-Pin QFP Lead-free RoHS Compliant packages

LAN91C111-NU (1.0mm height); LAN91C111i-NU (Industrlal Temperature)

for 128-Pin TQFP Lead-free RoHS Ccompliant packages

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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General Description

The SMSC LAN91C111 is designed to facilitate the implementation of a third generation of Fast Ethernet connectivity solutions for embedded applications. For this third generation of products, flexibility and integration dominate the design requirements. The LAN91C111 is a mixed signal Analog/Digital device that implements the MAC and PHY portion of the CSMA/CD protocol at 10 and 100 Mbps. The design will also minimize data throughput constraints utilizing a 32-bit, 16-bit or 8-bit bus Host interface in embedded applications.

The total internal memory FIFO buffer size is 8 Kbytes, which is the total chip storage for transmit and receive operations.

The SMSC LAN91C111 is software compatible with the LAN9000 family of products.

Memory management is handled using a patented optimized MMU (Memory Management Unit) architecture and a 32-bit wide internal data path. This I/O mapped architecture can sustain back-to-back frame transmission and reception for superior data throughput and optimal performance. It also dynamically allocates buffer memory in an efficient buffer utilization scheme, reducing software tasks and relieving the host CPU from performing these housekeeping functions.

The SMSC LAN91C111 provides a flexible slave interface for easy connectivity with industry-standard buses. The Bus Interface Unit (BIU) can handle synchronous as well as asynchronous transfers, with different signals being used for each one. Asynchronous bus support for ISA is supported even though ISA cannot sustain 100 Mbps traffic. Fast Ethernet data rates are attainable for ISA-based nodes on the basis of the aggregate traffic benefits.

Two different interfaces are supported on the network side. The first Interface is a standard Magnetics transmit/receive pair interfacing to 10/100Base-T utilizing the internal physical layer block. The second interface follows the MII (Media Independent Interface) specification standard, consisting of 4 bit wide data transfers at the nibble rate. This interface is applicable to 10 Mbps standard Ethernet or 100 Mbps Ethernet networks. Three of the LAN91C111's pins are used to interface to the two-line MII serial management protocol.

The SMSC LAN91C111 integrates IEEE 802.3 Physical Layer for twisted pair Ethernet applications. The PHY can be configured for either 100 Mbps (100Base-TX) or 10 Mbps (10Base-T) Ethernet operation. The Analog PHY block consists of a 4B5B/Manchester encoder/decoder, scrambler/de-scrambler, transmitter with wave shaping and output driver, twisted pair receiver with on chip equalizer and baseline wander correction, clock and data recovery, Auto-Negotiation, controller interface (MII), and serial port (MI). Internal output wave shaping circuitry and on-chip filters eliminate the need for external filters normally required in 100Base-TX and 10Base-T applications.

The LAN91C111 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation with the on-chip Auto-Negotiation algorithm. The LAN91C111 is ideal for media interfaces for embedded application desiring Ethernet connectivity as well as 100Base-TX/10Base-T adapter cards, motherboards, repeaters, switching hubs. The LAN91C111 operates from a single 3.3V supply. The inputs and outputs of the host Interface are 5V tolerant and will directly interface to other 5V devices.

Block Diagram

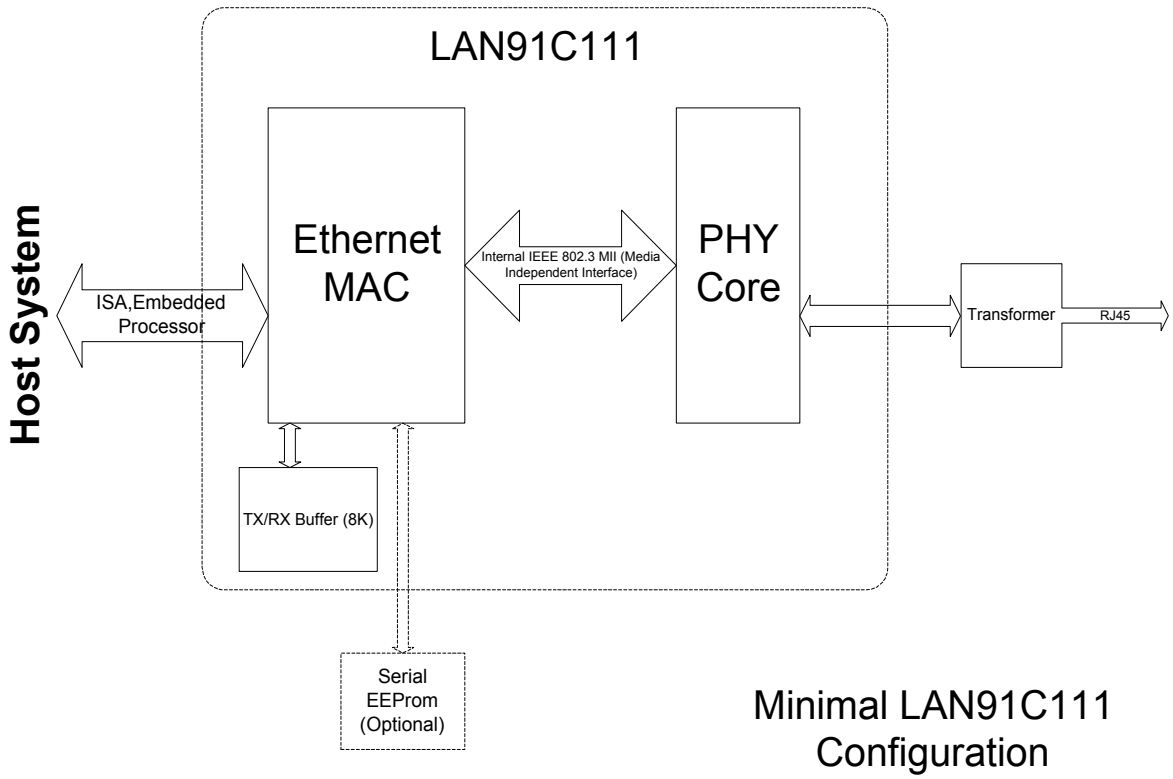

Figure 1 LAN91C111 Basic Functional Block Diagram

Package Outlines

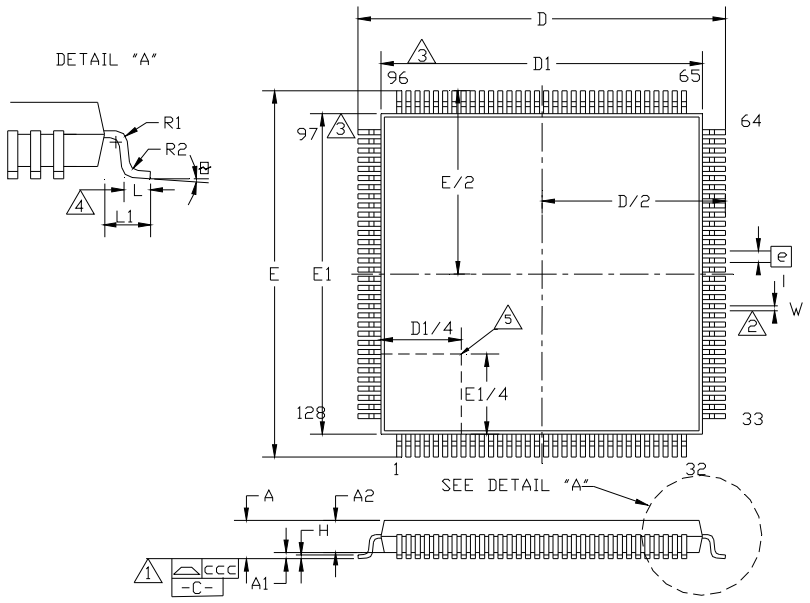

Figure 2 128 Pin TQFP Package Outline, 14X14X1.0 Body

Table 1 128 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D	15.80	16.00	16.20	X Span
D/2	7.90	8.00	8.10	$^1/_2$ X Span Measure from Centerline
D1	13.80	14.00	14.20	X body Size
E	15.80	16.00	16.20	Y Span
E/2	7.90	8.00	8.10	$^1/_2$ Y Span Measure from Centerline
E1	13.80	14.00	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e		0.40 Basic		Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.0762	Coplanarity *(Assemblers)*
ccc	~	~	0.08	Coplanarity *(Test House)*

Notes:

1. Controlling Unit: millimeter
2. Tolerance on the position of the leads is ± 0.035 mm maximum
3. Package body dimensions D1 and E1 do not include the mold protrusion.
   Maximum mold protrusion is 0.25 mm
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane is 0.78-1.08 mm.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.
6. Shoulder widths must conform to JEDEC MS-026 dimension 'S' of a minimum of 0.20mm.

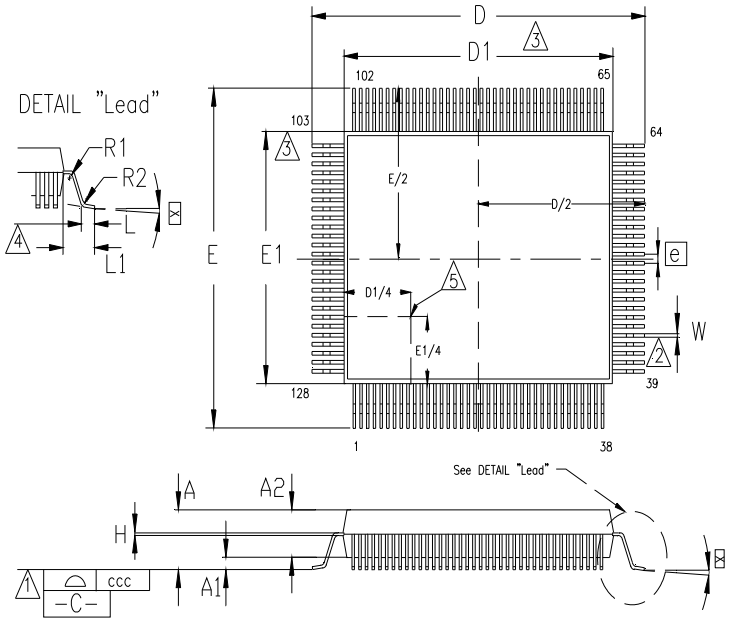

Figure 3 128 Pin QFP Package Outline, 3.9 MM Footprint

Table 2 128 Pin QFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.70	23.90	24.10	X Span
D/2	11.85	11.95	12.05	$^1/_2$ X Span Measured from Centerline
D1	19.90	20.0	20.10	X body Size
E	17.70	17.90	18.10	Y Span
E/2	8.85	8.95	9.05	$^1/_2$ Y Span Measured from Centerline
E1	13.90	14.00	14.10	Y body Size
H	~	~	~	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.95	~	Lead Length
e		0.5 Basic		Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.13	~	~	Lead Shoulder Radius
R2	0.13	~	0.30	Lead Foot Radius
ccc	~	~	0.0762	Coplanarity *(Assemblers)*
ccc	~	~	0.08	Coplanarity *(Test House)*

Notes:

1. Controlling Unit: millimeter
2. Tolerance on the position of the leads is + 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.