SMSC® SUCCESS BY DESIGN

LAN9215

16-bit Non-PCI 10/100 Ethernet Controller with HP Auto-MDIX Support

PRODUCT FEATURES

Data Brief

Highlights

- Optimized for medium performance applications
- Efficient architecture with low CPU overhead
- Easily interfaces to most 16-bit embedded CPU's
- Integrated PHY with HP Auto-MDIX support
- Supports audio & video streaming over Ethernet: multiple standard-definition (SD) MPEG2 streams
- Compatible with other members of LAN9218 family

Target Applications

- Basic cable, satellite, and IP set-top boxes
- Digital video recorders
- Video-over IP solutions, IP PBX & video phones
- Wireless routers & access points
- Audio distribution systems
- Printers, kiosks, security systems
- General embedded applications

Key Benefits

- Non-PCI Ethernet controller for medium performance applications
  - 16-bit interface
  - Burst-mode read support
  - External MII Interface
- Eliminates dropped packets
  - Internal buffer memory can store over 200 packets
  - Automatic PAUSE and back-pressure flow control
- Minimizes CPU overhead
  - Supports Slave-DMA
  - Interrupt Pin with Programmable Hold-off timer
- Reduces system cost and increases design flexibility
- SRAM-like interface easily interfaces to most embedded CPU's or SoC's
- Reduced Power Modes
  - Numerous power management modes
  - Wake on LAN*
  - Magic packet wakeup*
  - Wakeup indicator event signal
  - Link Status Change
- Single chip Ethernet controller
  - Fully compliant with IEEE 802.3/802.3u standards
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and Half-duplex support
  - Full-duplex flow control
  - Backpressure for half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
- Flexible address filtering modes
  - One 48-bit perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast
  - Promiscuous mode
  - Inverse filtering
  - Pass all incoming with status report
  - Disable reception of broadcast packets
- Integrated 10/100 Ethernet PHY
  - Supports HP Auto-MDIX
  - Auto-negotiation
  - Supports energy-detect power down
- Host bus interface
  - Simple, SRAM-like interface
  - 16-bit data bus
  - 16Kbyte FIFO with flexible TX/RX allocation
  - One configurable host interrupt
- Miscellaneous features
  - Low-profile 100-pin TQFP, or 100-ball LFBGA lead-free RoHS Compliant package
  - Integrated 1.8V regulator
  - General Purpose Timer
  - Optional EEPROM interface
  - Support for 3 status LEDs multiplexed with Programmable GPIO signals
- Single 3.3V Power Supply with 5V tolerant I/O
- 0°C to +70°C Commercial Temperature Support

Order Number(s):

LAN9215-MT for 100-pin, TQFP Lead-free RoHS Compliant package with E3 Finish (Matte Tin) (0 to +70°C Temp Range)

LAN9215-MZP for 100-ball, LFBGA Lead-free RoHS Compliant package (0 to +70°C Temp Range)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

General Description

The LAN9215 is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9215 has been architected to provide the best price-performance ratio for any 16-bit application with medium performance requirements. The LAN9215 is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX.

The LAN9215 includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit microprocessors and microcontrollers as well as 32-bit microprocessors with a 16-bit external bus. The LAN9215 includes large transmit and receive data FIFOs to accommodate high latency applications. In addition, the LAN9215 memory buffer architecture allows highly efficient use of memory resources by optimizing packet granularity.

Applications

The LAN9215 is well suited for many medium-performance embedded applications, including:

- Printers, kiosks, POS terminals and security systems
- Audio distribution systems
- General embedded systems
- Basic cable, satellite and IP set-top boxes
- Voice-over-IP solutions

The LAN9215 also supports features which reduce or eliminate packet loss. Its internal 16-KByte SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9215 can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

The LAN9215 supports numerous power management and wakeup features. The LAN9215 can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including “Magic Packet”, “Wake on LAN” and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command.

Block Diagram

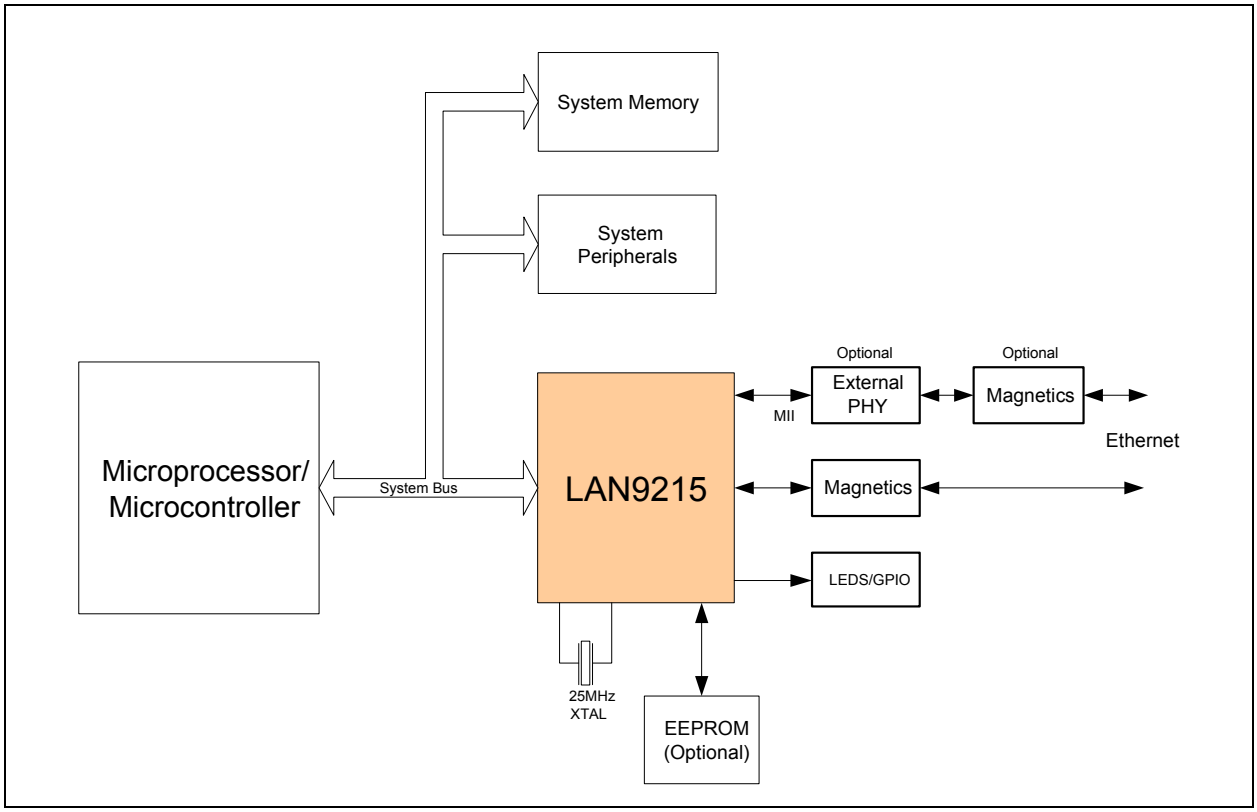

Figure 1 System Block Diagram

Package Outline

100-TQFP Package

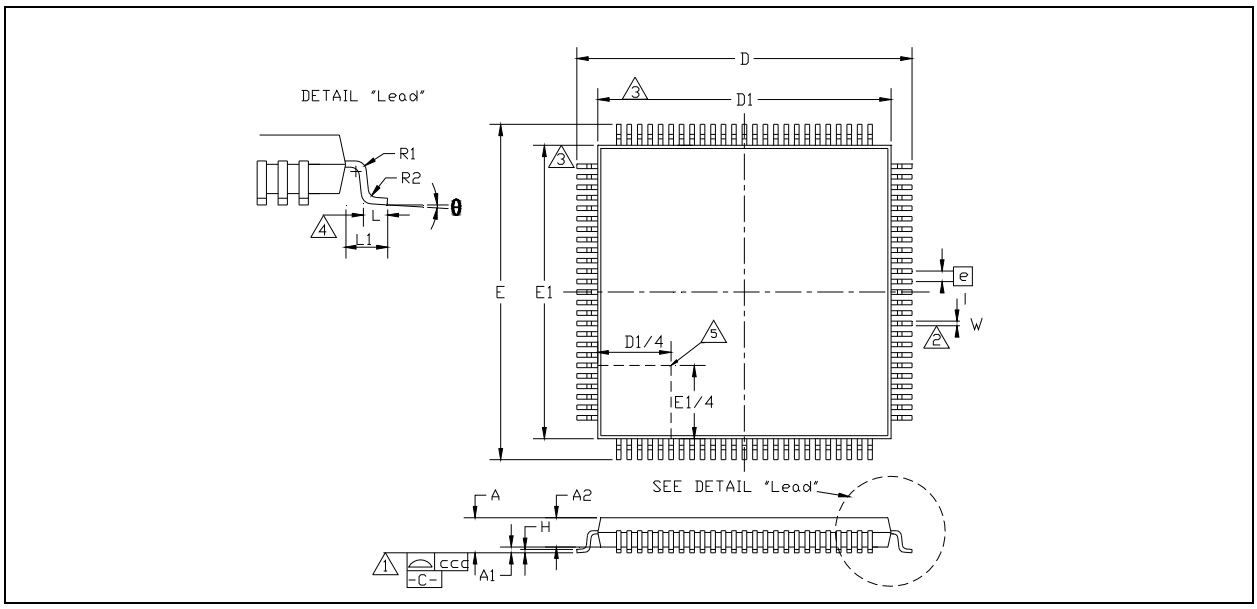

Figure 2 100-Pin TQFP Package Definition

Table 1 100-Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	15.80	~	16.20	X Span
D1	13.90	~	14.10	X body Size
E	15.80	~	16.20	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

2.1 100-LFBGA Package

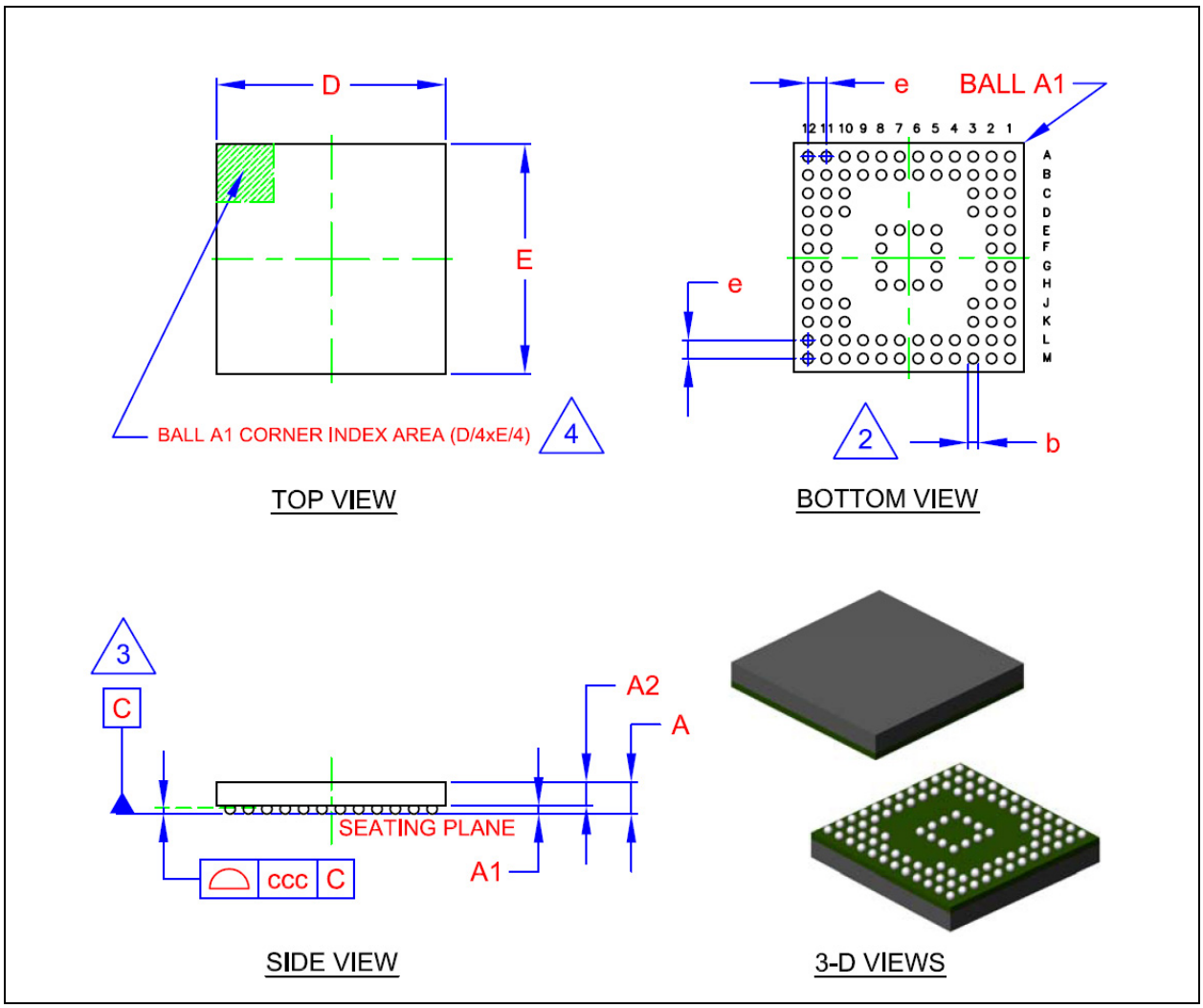

Figure 3 100 Ball LFBGA Package Definition

Table 2 100 Ball LFBGA Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	1.60	1.70	Overall Package Height
A1	0.25	0.34	~	Standoff
A2	1.16	1.26	1.36	Package Body Thickness
D/E	9.90	10.00	10.10	Overall Package Size
b	0.40	~	0.50	Ball Diameter
e	0.80 Basic			Ball Pitch
ccc	~	~	0.20	Coplanarity

Notes:

1. All dimensions are in millimeters.
2. Maximum radial true position tolerance of each ball is +/- 0.075mm at maximum material condition. Dimension “b” is measured at the maximum ball diameter, parallel to primary datum “C”.
3. Primary datum “C” (seating plane) is defined by the spherical crowns of the contact balls.
4. The A1 corner identifier may vary, but is always located within the zone indicated.

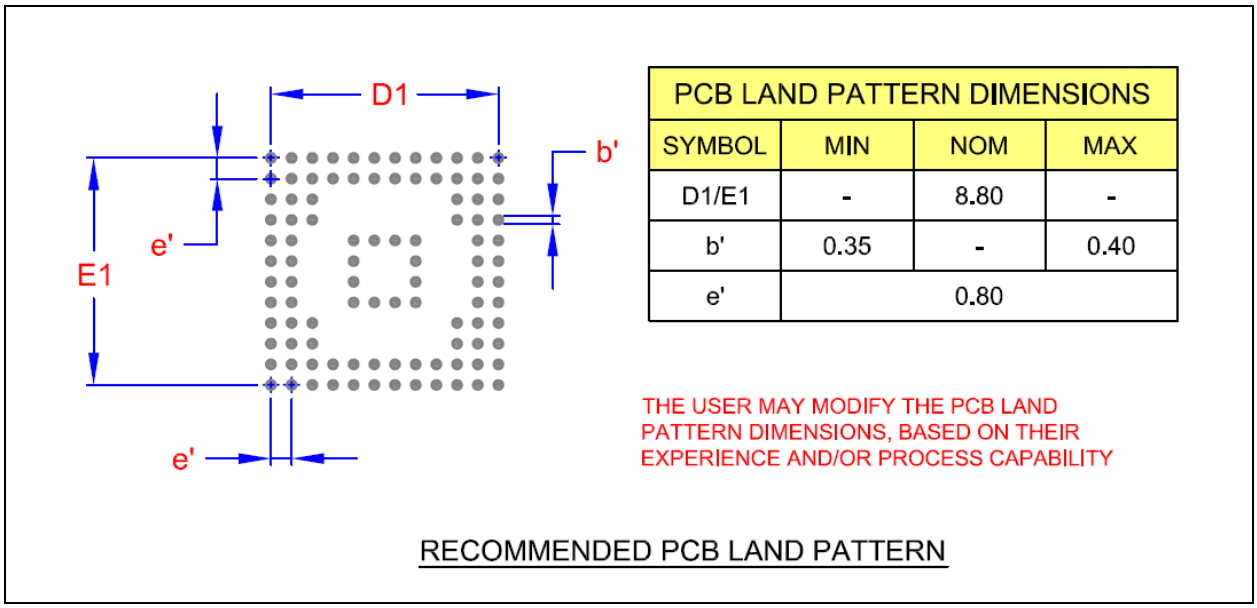

Figure 4 100 Ball LFBGA Recommended PCB Land Pattern