ATA6824C

High-Temperature H-Bridge Motor Driver

Features

- PWM and Direction Controlled Driving of Four Externally Powered NMOS Transistors
- High-Temperature Capability of Up to +200°C Junction
- A Programmable Dead Time is Included to Avoid Peak Currents within the H-Bridge
- Integrated Charge Pump to Provide Gate Voltages for High-Side Drivers and to Supply the Gate of the External Battery Reverse Protection NMOS
- 5V/3.3V Regulator and Current Limitation Function
- Reset Derived from 5V/3.3V Regulator Output Voltage
- A Programmable Window Watchdog Timer (WDT)
- Battery Overvoltage Protection and Battery Undervoltage Management
- Overtemperature Warning and Protection (Shutdown)
- High-Voltage Serial Interface for Communication
- TQFP Package

Description

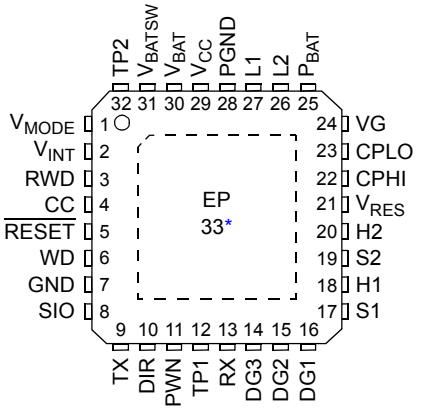
The Microchip Technology ATA6824C is designed for DC motor control applications in high-temperature automotive environments, such as mechatronic assemblies in the vicinity of the hot engine (e.g., the turbocharger). With a maximum junction temperature of +200°C, the ATA6824C is suitable for applications with an ambient temperature of up to +150°C.

The device includes four driver stages to control four external power MOSFETs. An external microcontroller provides the direction signal and the PWM frequency. In PWM operation, the high-side switches are permanently on, while the low-side switches are activated by the PWM frequency. The ATA6824C also includes a voltage regulator to supply the microcontroller; the output voltage can be set to either 5V or 3.3V via the V_{MODE} input pin.

The on-chip window Watchdog Timer provides a pin-programmable time window. The Watchdog Timer is internally trimmed to a 10% accuracy. For communication, a high-voltage serial interface with a maximum data range of 20 Kbaud is integrated.

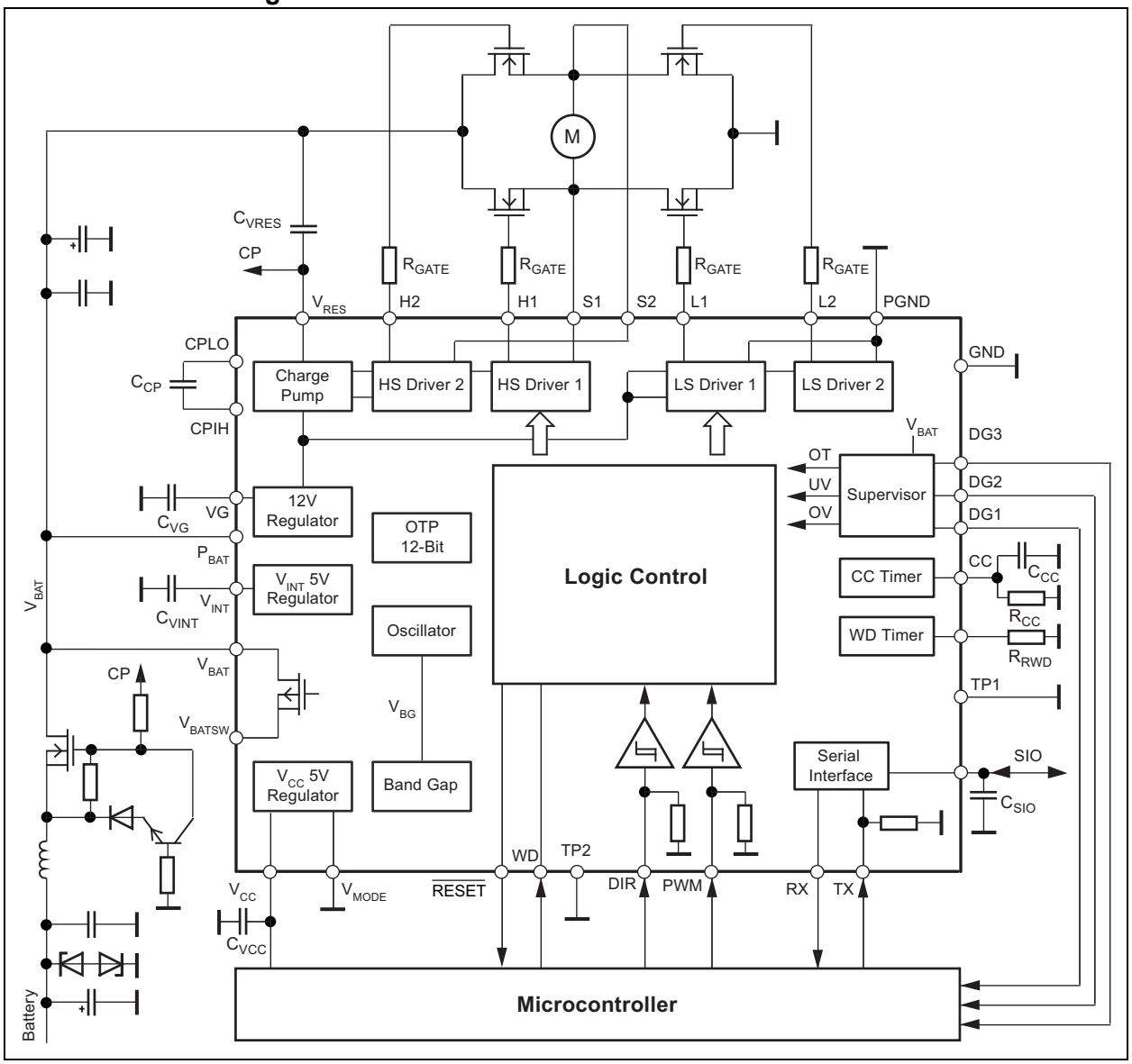
Package Types

TQFP-32



* Includes Exposed Thermal Pad (EP); see Table 2-1.

Functional Block Diagram



Typical External Components

Component	Function	Value	Tolerance
C_{VINT}	Blocking Capacitor at V_{INT} Pin	220 nF, 10V, X7R	50%
C_{VCC}	Blocking Capacitor at V_{CC} Pin	2.2 µF, 10V, X7R	50%
C_{CC}	Cross-Conduction Time Definition Capacitor	Typical 680 pF, 100V, COG	
R_{CC}	Cross-Conduction Time Definition Resistor	Typical 10 kΩ	
C_{VG}	Blocking Capacitor at VG Pin	Typical 470 nF, 25V, X7R	50%
C_{CP}	Charge Pump Capacitor	Typical 220 nF, 25V, X7R	
C_{VRES}	Reservoir Capacitor	Typical 470 nF, 25V, X7R	
R_{RWD}	Watchdog Timer Definition Resistor	Typical 51 kΩ	
C_{SIO}	Filter Capacitor for SIO Pin	Typical 220 pF, 100V	

Note: The **Functional Block Diagram** and **Typical External Components** sections describe the principal application for which the Microchip ATA6824C was designed. Microchip cannot be considered to understand fully all aspects of the system, application and environment. Therefore, no warranties of fitness for a particular purpose are given.

General Statement and Conventions

- Parameter values given without tolerances are indicative only and not to be tested in production.
- Parameters given with tolerances, but without a parameter number in the first column of the parameter table, are ensured by design (mainly covered by measurement of other specified parameters). These parameters are not to be tested in production. The tolerances are given if the knowledge of the parameter tolerances is important for the application.
- The lowest power supply voltage is named GND.
- All voltage specifications are referred to GND if not otherwise stated.
- Sinking current means that the current is flowing into the pin (value is positive).
- Sourcing current means that the current is flowing out of the pin (value is negative).

Related Documents

- Qualification of integrated circuits according to Atmel HNO procedure based on AEC-Q100
- AEC-Q100-004 and JESD78 (Latch-up)
- ESD STM 5.1-1998
- CEI 801-2 (only for information regarding ESD requirements of the PCB)

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

GND Pin 0V
PGND Pin ..... -0.3V to +0.3V
V_{BAT}, P_{BAT} Pins ..... ≤ 40V
Reverse Current Out of V_{BAT} Pin ..... ≥ -1 mA
Reverse Current Out of P_{BAT} Pin ..... ≥ -20 mA
$\overline{RESET}$, DG1, DG2, DG3, CC, WD, RWD, DIR, PWM, RX and TX Pins ..... -0.3V to (V_{VCC} + 0.3V)
V_{INT} and V_{CC} Pins ..... -0.3V to +5.5V
V_{MODE} Pin ..... -0.3V to (V_{INT} + 0.3V)
VG Pin ..... ≤16V
SIO Pin ..... -27V to (V_{VBAT} + 2V)
S1 and S2 Pins ..... -2V to +30V
-2V to +40V **(Note 1)**
L1 and L2 Pins ..... (V_{PGND} – 0.3V) to (V_{VG} + 0.3V)
H1 and H2 Pins ..... (V_{Sx} – 1V) to (V_{Sx} + 16V) **(Note 2)**
CPLO Pin ..... ≤ (V_{PBAT} + 0.3V)
CPHI Pin ..... ≤ (V_{VRES} + 0.3V)
V_{RES} ..... ≤ 40V **(Note 3)**
Reverse Current for CPLO, CPHI, VG, V_{RES}, S1 and S2 Pins ..... ≥ -2 mA
Reverse Current for L1, L2, H1 and H2 Pins ..... ≥ -1 mA
V_{BATSW} ..... -0.3V to (V_{VBAT} + 0.3V)
Power Dissipation (P_{tot}) ..... ≤ 1.4W **(Note 4)**
Storage Temperature ..... -55°C to +150°C

Note 1: Tolerated up to t < 0.5s.

2: Valid for respective pins as x = 1, x = 2.

3: Load dump of t < 0.5s tolerated.

4: May be additionally limited by external thermal resistance.

† **Notice:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise stated, all parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 150°C$.

No.	Parameters	Symbol	Pins	Min.	Typ.	Max.	Units	Conditions
1	**Power Supply and Supervisor Functions**							
1.1	Current Consumption V_{VBAT}	I_{VBAT1}	25, 30	—	—	7	mA	V_{VBAT} = 13.5V **(Note 4)**
1.2	Internal Power Supply	V_{INT}	2	4.8	4.94	5.1	V	
1.3	Band Gap Voltage	V_{BG}	3	—	1.235	—	V	
1.4	Overvoltage Threshold Up V_{PBAT}	V_{THOV_UP}	25	21.2	—	22.7	V	
1.4.1	Overvoltage Threshold Down V_{PBAT}	V_{THOV_DOWN}		19.7	—	21.3	V	
1.5	Overvoltage Threshold Hysteresis V_{PBAT}	V_{TOVhys}		1	—	2.4	V	
1.6	Undervoltage Threshold Up V_{VBAT}	V_{THUV_UP}	30	6.8	—	7.4	V	
1.6.1	Undervoltage Threshold Down V_{VBAT}	V_{THUV_DOWN}		6.5	—	7.0	V	
1.7	Undervoltage Threshold Hysteresis V_{VBAT}	V_{TUVhys}		0.2	—	0.6	V	Measured during qualification only
1.8	On Resistance of V_{VBAT} Switch	R_{ON_VBATSW}	31	—	—	100	Ω	V_{VBAT} = 13.5V
1.9	Undervoltage Threshold P_{BAT}	V_{PBAT_OK}	25	6.1	—	7	V	V_{VBAT} = 13.5V
1.10	Undervoltage Threshold Hysteresis P_{BAT}	$V_{PBAT\_OK\_HYST}$		0	—	100	mV	V_{VBAT} = 13.5V
2	**5V/3.3V Regulator**							
2.1	Regulated Output Voltage	V_{CC1}	29	4.85 (3.2)	—	5.15 (3.4)	V	$9V < V_{VBAT} < 40V$, I_{Load} = 0 mA to 100 mA
2.2		V_{CC2}		4.75 (3.2)	—	5.25 (3.4)	V	$6V < V_{VBAT} \le 9V$, I_{Load} = 0 mA to 100 mA
2.2a				4.75 (3.2)	—	5.25 (3.4)	V	$6V < V_{VBAT} \le 9V$, I_{Load} = 0 mA to 80 mA $T_A > 125°C$
2.3	Line Regulation	DC Line Regulation		—	< 1	50	mV	I_{Load} = 0 mA to 100 mA
2.4	Load Regulation	DC Load Regulation		—	< 10	50	mV	I_{Load} = 0 mA to 100 mA
2.5	Output Current Limitation	I_{OS1}		100	—	350	mA	$V_{VBAT} \ge 6V$
2.6	Serial Inductance to C_{VCC} Including PCB	ESL		1	—	20	nH	**Note 3**
2.7	Serial Resistance to C_{VCC} Including PCB	ESR		0	—	0.5	Ω	**Note 3**
2.8	Blocking Cap at V_{CC}	C_{VCC}		1.1	—	3.3	µF	**Note 5**, **Note 6**
2.9	High Threshold V_{MODE}	V_{MODE} H	1	—	—	4.0	V	
2.10	Low Threshold V_{MODE}	V_{MODE} L		0.7	—	—	V	

Note 1: 100% correlation tested.
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5: The use of X7R material is recommended.
6: For higher values, stability at zero load is not ensured.
7: Tested during qualification only.
8: Value depends on T_{100}. Function tested with digital test pattern.
9: Tested during characterization only.
10: Supplied by charge pump.
11: See **Section 3.9.1 "Cross-Conduction Time"**.
12: Voltage between source drain of external switching transistors in active case.
13: The short-circuit message will never be generated for switch-on time < t_{SC}.
14: See Figure 3-5 for the definition of bus timing parameters.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise stated, all parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 150°C$.

No.	Parameters	Symbol	Pins	Min.	Typ.	Max.	Units	Conditions
3	**VG Regulator**							
3.1	Regulated Output Voltage	V_{VG}	24	11	—	14	V	$V_{PBAT} \ge 14V$, $I_{max} = 20$ mA
3.2				7.0	—	9.0	V	$V_{PBAT} \ge 9V$, $I_{max} = 20$ mA
4	**Reset and Watchdog Timer**							
4.1	V_{CC} Threshold Voltage Level for $\overline{\text{RESET}}$	V_{tHRESH}	29	—	4.8 (3.15)	—	V	V_{MODE} = "H" (V_{MODE} = "L")
4.1a	Tracking of Reset Threshold with Regulated Output Voltage	$V_{VCC1\text{-}VtHRESH}$		75 (50)	—	—	mV	V_{MODE} = "H" (V_{MODE} = "L")
4.2	V_{CC} Threshold Voltage Level for $\overline{\text{RESET}}$	V_{tHRESL}		4.3 (2.86)	—	—	V	V_{MODE} = "H" (V_{MODE} = "L")
4.3	Hysteresis of $\overline{\text{RESET}}$ Level	HYS_{RESth}		70	200	350 (240)	mV	V_{MODE} = "H" (V_{MODE} = "L") **(Note 7)**
4.4	Length of Pulse at $\overline{\text{RESET}}$ Pin	t_{RES}	5	—	7000	—	T_{100}	**Note 8**
4.5	Length of Short Pulse at $\overline{\text{RESET}}$ Pin	$t_{RESSHORT}$		—	200	—	T_{100}	**Note 8**
4.6	Wait for First WD Trigger	t_d		—	7000	—	T_{100}	**Note 8**
4.7	Time for $V_{CC} < V_{tHRESL}$ Before Activating $\overline{\text{RESET}}$	$t_{delayRESL}$	29	0.5	—	2	µs	**Note 3**
4.8	Resistor Defining Internal Bias Currents for Watchdog Timer Oscillator	R_{RWD}	3	10	—	91	kΩ	**Note 3**
4.9	Watchdog Timer Oscillator Period	T_{OSC}		11.09	—	13.55	µs	R_{RWD} = 33 kΩ
4.11	Watchdog Timer Input Low-Voltage Threshold	V_{ILWD}	6	—	—	0.3 × V_{VCC}	V	
4.12	Watchdog Timer Input High-Voltage Threshold	V_{IHWD}		0.7 × V_{VCC}	—	—	V	
4.13	Hysteresis of Watchdog Timer Input Voltage Threshold	V_{hysWD}		0.3	—	0.8	V	
4.14	Close Window	t1		—	980 × T_{OSC}	—		**Note 8**
4.15	Open Window	t2		—	780 × T_{OSC}	—		**Note 8**
4.16	Output Low Voltage of $\overline{\text{RESET}}$	V_{OLRES}	5	—	—	0.4	V	At I_{OLRES} = 1 mA
4.17	Internal Pull-up Resistor at $\overline{\text{RESET}}$ Pin	R_{PURES}		5	10	15	kΩ	

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise stated, all parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 150°C$.

No.	Parameters	Symbol	Pins	Min.	Typ.	Max.	Units	Conditions
5	**High-Voltage Serial Interface**							
5.1	Low-Level Output Current	IL_{RX}	13	2	—	—	mA	Normal mode, V_{SIO} = 0V, V_{RX} = 0.4V
5.2	High-Level Output Current	IH_{RX}		0.8	—	—	mA	Normal mode, $V_{SIO} = V_{BAT}$, $V_{RX} = V_{CC} - 0.4V$
5.4	Driver-Dominant Voltage $V_{BUSdom\_DRV\_LoSUP}$	$V_{\_LoSUP}$	8	—	—	1.2	V	V_{BAT} = 7.3V, R_{load} = 500Ω
5.5	Driver-Dominant Voltage $V_{BUSdom\_DRV\_HiSUP}$	$V_{\_HiSUP}$		—	—	2	V	V_{BAT} = 18V, R_{load} = 500Ω
5.6	Driver-Dominant Voltage $V_{BUSdom\_DRV\_LoSUP}$	$V_{\_LoSUP\_1k}$		0.6	—	—	V	V_{BAT} = 7.3V, R_{load} = 1000Ω
5.7	Driver-Dominant Voltage $V_{BUSdom\_DRV\_HiSUP}$	$V_{\_HiSUP\_1k}$		0.8	—	1.5	V	V_{BAT} = 18V, R_{load} = 1000Ω
5.8	Pull-up Resistor to V_{BAT}	R_{SIO}		20	30	60	kΩ	Serial diode is mandatory
5.9	Current Limitation	I_{SIO_LIM}		40	—	250	mA	$V_{SIO} = V_{BAT\_max}$
5.9a	Current Limitation, $\overline{\text{RESET}}$ and SIO Overheat	$I_{SIO\_LIM\_RESET}$		30	—	100	mA	$V_{SIO} = V_{BAT\_max}$, $\overline{\text{RESET}}$ = high
5.10	Input Leakage Current at the Receiver Including Pull-up Resistor as Specified	$I_{SIO\_PAS\_dom}$		-1	—	—	mA	Input leakage current driver off, V_{SIO} = 0V, V_{VBAT} = 12V
5.11	Leakage Current SIO Recessive	$I_{SIO\_PAS\_rec}$		—	—	30	µA	Driver off, $8V < V_{VBAT} < 18V$, $8V < V_{SIO} < 18V$, $V_{SIO} \ge V_{VBAT}$
5.12	Leakage Current at Ground Loss Control Unit, Disconnected from Ground Loss of Local Ground Must Not Affect Communication in the Residual Network	$I_{SIO\_NO\_gnd}$		-1	—	1	mA	$GND_{Device} = V_{VBAT}$, V_{VBAT} = 12V, $0V < V_{SIO} < 18V$
5.13	Node has to Sustain the Current that can Flow Under this Condition, Bus Must Remain Operational	I_{SIO}		—	—	100	µA	V_{VBAT} disconnected, V_{SUP_Device} = GND, 0V < VSIO < 18V
5.14	Center of Receiver Threshold	V_{SIO_CNT}		$0.475 \times V_{VBAT}$	$0.5 \times V_{VBAT}$	$0.525 \times V_{VBAT}$	V	$V_{SIO\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$
5.15	Receiver Dominant State	V_{SIOdom}		—	—	$0.4 \times V_{VBAT}$	V	V_{EN} = 5V
5.16	Receiver Recessive State	V_{SIOrec}		$0.6 \times V_{VBAT}$	—	—	V	V_{EN} = 5V
5.17	Receiver Input Hysteresis	V_{SIOhys}		—	$0.1 \times V_{VBAT}$	$0.175 \times V_{VBAT}$	V	$V_{HYS} = V_{th\_rec} - V_{th\_dom}$

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8: Value depends on T_{100}. Function tested with digital test pattern.
9: Tested during characterization only.
10: Supplied by charge pump.
11: See **Section 3.9.1 "Cross-Conduction Time"**.
12: Voltage between source drain of external switching transistors in active case.
13: The short-circuit message will never be generated for switch-on time < t_{SC}.
14: See Figure 3-5 for the definition of bus timing parameters.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise stated, all parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 150°C$.

No.	Parameters	Symbol	Pins	Min.	Typ.	Max.	Units	Conditions
5.18	Duty Cycle 1	D1	8	0.380	—	—		$TH_{Rec(max)} = 0.744 \times V_{VBAT}$, $TH_{Dom(max)} = 0.581 \times V_{VBAT}$, V_{VBAT} = 7V to 18V, t_{Bit} = 50 µs, D1 = $t_{sio\_rec(min)}/2 \times t_{Bit}$ (Note 14)
5.19	Duty Cycle 2	D2		—	—	0.600		$TH_{Rec(min)} = 0.422 \times V_{VBAT}$, $TH_{Dom(min)} = 0.284 \times V_{VBAT}$, V_{VBAT} = 7V to 18V, t_{Bit} = 50 µs, D1 = $t_{sio\_rec(max)}/2 \times t_{Bit}$ (Note 14)
5.20	Propagation Delay of Receiver	t_{rx_pd}		—	—	6	µs	t_{rec_pd} = max (t_{rx_pdr}, t_{rx_pdf}) (Note 14), 7V < V_{VBAT} < 18V
5.21	Symmetry of Receiver Propagation Delay	t_{rx_sym}		-2	—	+2	µs	$t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$ (Note 14), 7V < V_{VBAT} < 18V
6	**Control Inputs DIR, PWN, WD, TX**							
6.1	Input Low-Voltage Threshold	V_{IL}	10, 11, 6, 9	—	—	0.3 × V_{VCC}	V	
6.2	Input High-Voltage Threshold	V_{IH}		0.7 × V_{VCC}	—	—	V	
6.3	Hysteresis	HYS		0.3	0.5	0.8	V	
6.4	Pull-Down Resistor	R_{PD}		25	50	140	kΩ	DIR, PWM, WD, TX
6.5	Rise/Fall Time	t_{rf}		—	—	100	ns	
7	**Charge Pump**							
7.1	Charge Pump Voltage	V_{CP}	21	—	—	V_{VBAT} + V_{VG}	V	Load = 0A
7.2				V_{VBAT} + V_{VG} – 1	—	—	V	Load = 3 mA, C_{CP} = 100 nF
7.3	Period Charge Pump Oscillator	T_{100}		9	—	11	µs	
7.4	CP Load Current in VG without CP Load	I_{VGCPz}		—	—	600	µA	Load = 0A
7.5	CP Load Current in VG with CP Load	I_{VGCP}		—	—	4	mA	Load = 3 mA, C_{CP} = 100 nF
7.6	Charge Pump OK Threshold UP	V_{CPOK_UP}		5.3	—	6.3	V	Reference: P_{BAT}
7.7	Charge Pump OK Threshold DOWN	V_{CPOK_DOWN}		4.5	—	5.5	V	Reference: P_{BAT}
7.8	Charge Pump OK Hysteresis	V_{CPOK_HYS}		0.3	—	1.3	V	

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise stated, all parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 150°C$.

No.	Parameters	Symbol	Pins	Min.	Typ.	Max.	Units	Conditions
8	**H-Bridge Driver**							
8.1	Low-Side Driver HIGH Output Voltage	V_{LxH}	26, 27	V_{VG} – 0.5V	—	V_{VG}	V	
8.2	On-Resistance of Sink Stage of Pins L1, L2	R_{DSON_LxL}, x = 1, 2		—	—	25	Ω	
8.3	ON-Resistance of Source Stage of Pins L1, L2	R_{DSON_LxH}, x = 1, 2		—	—	25	Ω	
8.4	Output Peak Current at Pins L1, L2, Switched to LOW	I_{LxL}, x = 1, 2		100	—	—	mA	V_{Lx} = 3V
8.5	Output Peak Current at Pins L1, L2, Switched to HIGH	I_{LxH}, x = 1, 2		—	—	-100	mA	V_{Lx} = 3V
8.6	Ohmic Pull-Down Resistance at Pins L1, L2	R_{PDLx}, x = 1, 2		25	—	140	kΩ	Designed for: 0V < V_{VBAT} < 40V
8.7	ON-Resistance of Sink Stage of Pins H1, H2	R_{DSON_HxL}, x = 1, 2	18, 20	—	—	25	Ω	V_{Sx} = 0V
8.8	ON-Resistance of Source Stage of Pins H1, H2	R_{DSON_HxH}, x = 1, 2		—	—	25	Ω	V_{Sx} = V_{VBAT}
8.9	Output Peak Current at Pins H1, H2, Switched to LOW	I_{HxL}, x = 1, 2		100	—	—	mA	V_{VBAT} = 13.5V, V_{Sx} = V_{VBAT}, V_{Hx} = V_{VBAT} + 3V
8.10	Output Peak Current at Pins H1, H2, Switched to HIGH	I_{HxH}, x = 1, 2		—	—	-100	mA	V_{VBAT} = 13.5V, V_{Sx} = V_{VBAT}, V_{Hx} = V_{VBAT} + 3V
8.11	Static Switch Output Low Voltage at Pins Hx and Lx	V_{HxL}, V_{LxL}, x = 1, 2	18, 20, 26, 27	—	—	0.3	V	V_{Sx} = 0V, I_{Hx} = 1 mA, I_{Lx} = 1 mA
8.12	Static High-Side Switch Output High-Voltage Pins H1, H2	$V_{HxHstat1}$ **(Note 10)**	18,20	V_{VBAT} + V_{VG} – 1	—	V_{VBAT} + V_{VG}	V	I_{Lx} = -10 µA (PWM = static)
8.13	Ohmic Sink Resistance Between Pins Hx and Sx	R_{PDHx}, x = 1, 2	17, 18, 19, 20	25	—	140	kΩ	Designed for: 0V < V_{VBAT} < 40V

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13: The short-circuit message will never be generated for switch-on time < t_{SC}.
14: See Figure 3-5 for the definition of bus timing parameters.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise stated, all parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 150°C$.

No.	Parameters	Symbol	Pins	Min.	Typ.	Max.	Units	Conditions
9	**Dynamic Parameters**							
9.1	Propagation Delay Time, Low-Side Driver from High-to-Low	t_{LxHL}	26, 27	—	—	0.5	µs	V_{VBAT} = 13.5V (see Figure 3-6)
9.2	Propagation Delay Time, Low-Side Driver from Low-to-High	t_{LxLH}		—	—	0.5 + t_{CC}	µs	V_{VBAT} = 13.5V
9.3	Fall Time Low-Side Driver	t_{Lxf}		—	—	0.5	µs	V_{VBAT} = 13.5V, C_{Gx} = 5 nF
9.4	Rise Time Low-Side Driver	t_{Lxr}		—	—	0.5	µs	V_{VBAT} = 13.5V
9.5	Propagation Delay Time, High-Side Driver from High-to-Low	t_{HxHL}	18, 20	—	—	0.5	µs	V_{VBAT} = 13.5V (see Figure 3-6)
9.6	Propagation Delay Time, High-Side Driver from Low-to-High	t_{HxLH}		—	—	0.5 + t_{CC}	µs	V_{VBAT} = 13.5V
9.7	Fall Time High-Side Driver	t_{Hxf}		—	—	0.5	µs	V_{VBAT} = 13.5V, C_{Gx} = 5 nF
9.8	Rise Time High-Side Driver	t_{Hxr}		—	—	0.5	µs	V_{VBAT} = 13.5V
9.9	External Resistor	R_{CC}	4	5	—	—	kΩ	**Note 3**
9.10	External Capacitor	C_{CC}		—	—	5	nF	**Note 3**
9.11	R_{ON} of t_{CC} Switching Transistor	R_{ONCC}		—	—	200	Ω	
9.12	Cross-Conduction Time (**Note 11**)	t_{CC}		3.75	—	4.45	µs	R_{CC} = 10 kΩ, C_{CC} = 1 nF
9.13	Short-Circuit Detection Voltage	V_{SC}	17, 19	3.5	4	4.7	V	**Note 12**
9.14	Short-Circuit Blanking Time	t_{SC}		5	10	15	µs	**Note 13**
10	**Diagnostic Outputs DG1, DG2, DG3**							
10.1	Low-Level Output Current	IL	14, 15, 16	2	—	—	mA	V_{DG} = 0.4V (**Note 9**)
10.2	High-Level Output Current	IH		0.8	—	—	mA	$V_{DG} = V_{CC} - 0.4V$ (**Note 9**)

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.
4: DIR, PWN = high.
5: The use of X7R material is recommended.
6: For higher values, stability at zero load is not ensured.
7: Tested during qualification only.
8: Value depends on T_{100}. Function tested with digital test pattern.
9: Tested during characterization only.
10: Supplied by charge pump.
11: See **Section 3.9.1 "Cross-Conduction Time"**.
12: Voltage between source drain of external switching transistors in active case.
13: The short-circuit message will never be generated for switch-on time < t_{SC}.
14: See Figure 3-5 for the definition of bus timing parameters.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Thermal Resistance Junction to Heat Slug	R_{thjc}	—	—	5	K/W	
Thermal Resistance Junction to Ambient when Heat Slub is Soldered to PCB	R_{thja}	—	25	—	K/W	

OPERATING RANGE

The operating conditions define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied unless otherwise stated explicitly.

TABLE 1-1: OPERATING RANGES

Parameters	Symbol	Min.	Max.	Units	Conditions
Operating Supply Voltage	V_{VBAT1}	V_{THUV}	V_{THOV}	V	Full functionality.
	V_{VBAT2}	6	< V_{THUV}		H-bridge drivers are switched off (undervoltage detection).
	V_{VBAT3}	4.5	< 6		H-bridge drivers are switched off, 5V/3.3V regulator with reduced parameters, $\overline{\text{RESET}}$ works correctly.
	V_{VBAT4}	0	< 4.5		H-bridge drivers are switched off, 5V regulator not working, $\overline{\text{RESET}}$ not correct.
	V_{VBAT5}	> V_{THOV}	40		H-bridge drivers are switched off.
Junction Temperature Range Under Bias	T_j	-40	+200	°C	
Normal Functionality	T_a	-40	+150		
Normal Functionality, Overtemperature Warning Set	T_j	+165	+195		
Switch-Off Temperatures of Drivers for H1, H2, L1, L2, SIO and of V_{CC} Regulator	T_j	+185	215		

NOISE AND SURGE IMMUNITY

Parameters	Value	Conditions
Conducted Interferences	Level 4[(1)]	ISO 7637-1
Interference Suppression	Level 5	IEC-CISPR25
ESD (Human Body Model)	2 kV	ESD S 5.1
CDM (Change Device Model)	500V	ESD STM5.3.

Note 1: Test Pulse 5: V_{vbmax} = 40V.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol	I/O	Function
1	V_{MODE}	I	Selector for V_{CC} and interface logic voltage level.
2	V_{INT}	I/O	Blocking capacitor, 220 nF/10V/X7R.
3	RWD	I	Resistor defining the Watchdog Timer interval.
4	CC	I/O	RC combination to adjust cross-conduction time.
5	$\overline{RESET}$	O	Reset signal for microcontroller.
6	WD	I	Watchdog Timer trigger signal.
7	GND	I	Ground for chip core.
8	SIO	I/O	High-voltage serial interface.
9	TX	I	Transmit signal to serial interface from microcontroller.
10	DIR	I	Defines the rotation direction for the motor.
11	PWM	I	PWM input; controls motor speed.
12	TP1	—	Test pin; to be connected to GND.
13	RX	O	Receive signal from serial interface for microcontroller.
14	DG3	O	Diagnostic Output 3.
15	DG2	O	Diagnostic Output 2.
16	DG1	O	Diagnostic Output 1.
17	S1	I/O	Source voltage H-bridge, High-Side 1.
18	H1	O	Gate voltage H-bridge, High-Side 1.
19	S2	I/O	Source voltage H-bridge, High-Side 2.
20	H2	O	Gate voltage H-bridge, High-Side 2.
21	V_{RES}	I/O	Gate voltage for reverse protection NMOS, blocking capacitor, 470 nF/25V/X7R.
22	CPHI	I	Charge pump capacitor, 220 nF/25V/X7R.
23	CPLO	O	
24	VG	I/O	Blocking capacitor, 470 nF/25V/X7R.
25	P_{BAT}	I	Power supply (after reverse protection) for charge pump and H-bridge.
26	L2	O	Gate voltage H-bridge, Low-Side 2.
27	L1	O	Gate voltage H-bridge, Low-Side 1.
28	PGND	I	Power ground for H-bridge and charge pump.
29	V_{CC}	O	5V/100 mA supply for microcontroller; blocking capacitor, 2.2 µF/10V/X7R.
30	V_{BAT}	I	Supply voltage for IC core (after reverse protection).
31	V_{BATSW}	O	100Ω PMOS switch from V_{VBAT}.
32	TP2	—	Test pin to be connected to GND.
33	EP	—	Exposed Thermal Pad; must be connected to GND.

NOTES:

3.0 FUNCTIONAL DESCRIPTION

3.1 Power Supply Unit with Supervisor Functions

3.1.1 4.1.1 POWER SUPPLY

The ATA6824C is supplied by a reverse-protected battery voltage. To prevent damage to the device, proper external protection circuitry must be added. It is recommended to use, at the very least, a capacitor combination of storage and HF caps behind the reverse protection circuitry, and closed to the V_{BAT} pin (see **Functional Block Diagram**).

An internal low-power and low-drop regulator (V_{INT}), stabilized by an external blocking capacitor, provides the necessary low-voltage supply for all internal blocks except the digital I/O pins. This voltage is also needed in the wake-up process. The low-power band gap reference is trimmed and is used for the bigger V_{CC} regulator, too. All internal blocks are supplied by the internal regulator.

The internal supply voltage, V_{VINT}, must not be used for any other supply purpose.

Nothing inside the ATA6824C, except the logic interface to the microcontroller, is supplied by the 5V/3.3V V_{CC} regulator.

A Power Good comparator checks the output voltage of the V_{INT} regulator and keeps the whole chip in Reset as long as the voltage is too low.

There is a high-voltage switch which brings out the battery voltage to the V_{BATSW} pin for measurement purposes. It is switched on for V_{CC} = HIGH and stays on in case of a Watchdog Timer Reset. The signal can be used, for example, to switch on external voltage regulators.

3.1.2 VOLTAGE SUPERVISOR

This block is intended to protect the device and the external power MOS transistors against overvoltage on the battery level and to manage the undervoltage on it.

In case of both overvoltage alarm (V_{THOV}) and undervoltage alarm (V_{THUV}), the external NMOS motor bridge transistors will be switched off. The failure state will be flagged via the DG2 pin. No other actions will be carried out. The undervoltage comparator is connected to the V_{BAT} pin, while the overvoltage comparator is connected to the P_{BAT} pin. Both are filtered by a first-order low-pass with a corner frequency of 15 kHz (typical).

3.1.3 TEMPERATURE SUPERVISOR

The device is equipped with an on-chip temperature sensor to prevent it from overheating due to a failure in the external circuitry and to protect the external NMOSFET transistors.

In case of overtemperature (+180°C), the DG3 diagnostic pin will be switched to “H” to signal an overtemperature warning to the microcontroller. It should then reduce the power dissipation in the ATA6824C.

In case of detected overtemperature (+200°C), the V_{CC} regulator and all drivers, including the serial interface, will be switched off immediately and the $\overline{\text{RESET}}$ pin will go low.

Both temperature thresholds are correlated. The absolute tolerance is ±15K and there is a built-in hysteresis of about 10K to avoid fast oscillations. After cooling down below the +170°C temperature threshold, the device will go into Active mode.

The occurrence of an overtemperature shutdown event is latched in DG3. DG3 stays on high until the first WD trigger.

3.2 5V/3.3V V_{CC} Regulator

The 5V/3.3V regulator is fully integrated on-chip. It requires a 2.2 µF ceramic capacitor for stability and has a current capability of 100 mA.

Using the V_{MODE} pin, the output voltage can be set to either 5V or 3.3V. For the 5V output voltage setting, the V_{MODE} pin must be hardwired to the V_{INT} pin. For the 3.3V output voltage option, the V_{MODE} pin must be hardwired to GND. The logic high level of the microcontroller interface will be adapted to the V_{CC} regulator voltage.

Note:	Changing the output voltage setting during operation is not intended to be supported.

The output voltage accuracy is generally < ±3%. In the 5V mode with V_{VBAT} < 9V, the output voltage accuracy is limited to < ±5%.

To prevent damage to the device, the current delivered by the regulator is limited to a maximum of 100 mA to 350 mA. The delivered voltage will break down and a Reset may occur.

Note:	This regulator is the main heat source on the chip. The maximum output current at maximum battery voltage and high ambient temperature can only be ensured if the device is mounted on an efficient heat sink.

A Power Good comparator checks the output voltage of the V_{CC} regulator and keeps the external microcontroller in Reset as long as the voltage is too low.

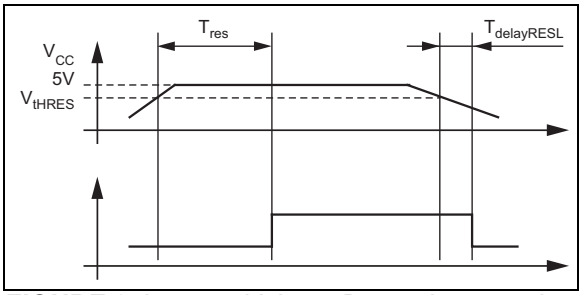


FIGURE 3-1: *Voltage Dependence and Timing of V_{CC} Controlled Reset.*

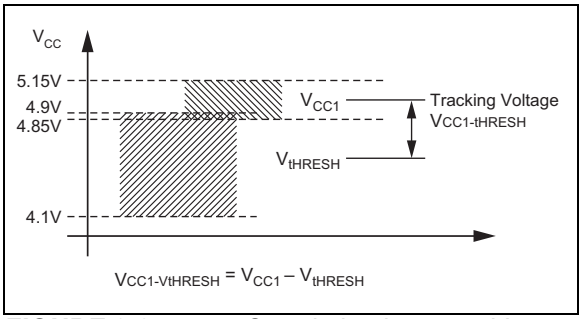


FIGURE 3-2: *Correlation between V_{CC} Output Voltage and Reset Threshold.*

The voltage difference between the regulator's output voltage and the upper Reset threshold voltage is higher than 75 mV when V_{MODE} is high and higher than 50 mV when V_{MODE} is low.

3.3 Reset and Watchdog Timer Management

The timing basis of the Watchdog Timer is provided by the trimmed internal oscillator. Its period, T_{OSC}, is adjustable via the external resistor, R_{WD}.

The Watchdog Timer expects a rising edge from the microcontroller at the WD input within a time window of T_{WD}.

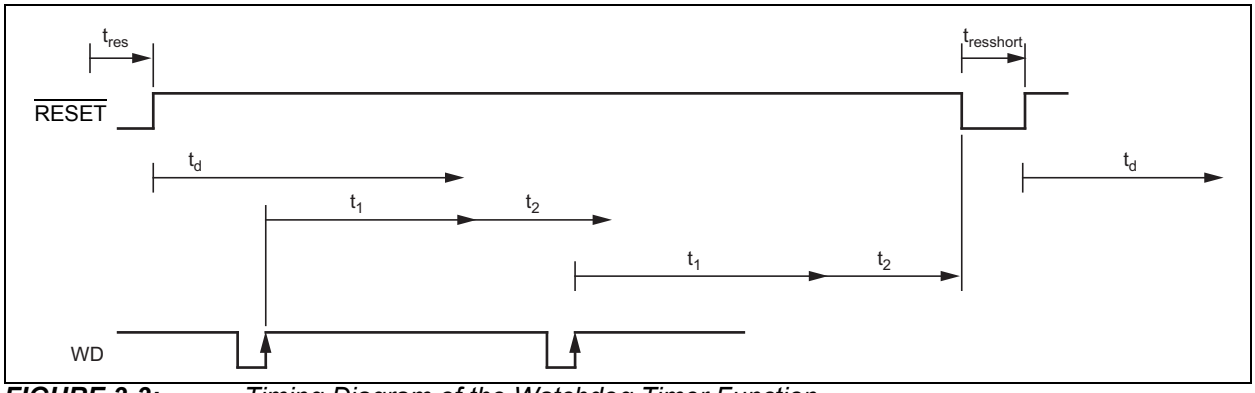


FIGURE 3-3: *Timing Diagram of the Watchdog Timer Function.*

3.3.1 TIMING SEQUENCE

For example, with an external resistor, R_{WD} = (33 kΩ ± 1%), the following typical parameters of the Watchdog Timer result in:

- T_{OSC} = 12.32 µs
- t_1 = 12.1 ms
- t_2 = 9.61 ms
- T_{WD} = 16.88 ms ± 10%

The times, t_{res} = 70 ms and t_d = 70 ms, are fixed values with a tolerance of 10%.

After the ramp-up of the battery voltage (Power-on Reset), the V_{CC} regulator is switched on. The Reset output, $\overline{RESET}$, stays low for the time, t_{res}, then switches to high. For an initial lead time, t_d (for setups in the controller), the Watchdog Timer waits for a rising edge on WD to start its normal window Watchdog Timer sequence. If no rising edge is detected, the Watchdog Timer will reset the microcontroller for t_{res} and wait t_d for the rising edge on WD.

Times, t_1 (close window) and t_2 (open window), form the window Watchdog Timer sequence. To avoid receiving a Reset from the Watchdog Timer, the triggering signal from the microcontroller must hit within the time frame of t_2 = 9.61 ms. The trigger event will restart the Watchdog Timer sequence.

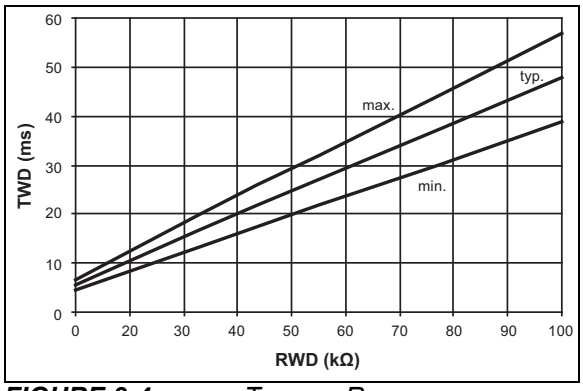


FIGURE 3-4: *T_{WD} vs. R_{WD}.*

If triggering fails, $\overline{RESET}$ will be pulled to ground for a shortened Reset time of typically 2 ms. The Watchdog Timer start sequence is similar to the Power-on Reset.

The internal oscillator is trimmed to a tolerance of < ±10%. This means that t_1 and t_2 can also vary by ±10%. The following calculation shows the worst-case calculation of the Watchdog Timer period, T_{WD}, which the microcontroller has to provide:

- $t_{1min} = 0.90 \times t_1 = 10.87$ ms
- $t_{1max} = 1.10 \times t_1 = 13.28$ ms
- $t_{2min} = 0.90 \times t_2 = 8.65$ ms
- $t_{2max} = 1.10 \times t_2 = 10.57$ ms
- $T_{WDmax} = t_{1min} + t_{2min} = 10.87$ ms + 8.65 ms = 19.52 ms
- $T_{WDmin} = t_{1max} = 13.28$ ms
- T_{WD} = 16.42 ms ± 3.15 ms (±19.1%)

Figure 3-4 shows the typical Watchdog Timer period, T_{WD}, depending on the value of the external resistor, R_{OSC}. A Reset will be active for $V_{CC} < V_{tHRESx}$. The level, V_{tHRESx}, is realized with a hysteresis (HYS_{RESth}).

3.4 High-Voltage Serial Interface

A bidirectional bus interface is implemented for data transfer between the host controller and the local microcontroller (SIO).

The transceiver consists of a low-side driver (1.2V at 40 mA) with slew rate control, wave shaping, current limitation and a high-voltage comparator, followed by a debouncing unit in the receiver.

3.4.1 TRANSMIT MODE

During transmission, the data at the TX pin will be transferred to the bus driver to generate a bus signal on the SIO pin. The TX pin has an included pull-down resistor.

To minimize the electromagnetic emission of the bus line, the bus driver has an integrated slew rate control and wave shaping unit. In Transmit mode, transmission will be interrupted in case of overheating at the SIO driver.

3.4.2 RESET MODE

In case of an active Reset shown at the $\overline{\text{RESET}}$ pin, the SIO pin is switched to low, independent of the temperature. The maximum current is limited to $I_{SIO\_LIM\_RESET}$.

The recessive bus level is generated from the integrated 30 kΩ pull-up resistor in series with an active diode. This diode prevents the reverse current of V_{BUS} during differential voltage between V_{SUP} and V_{BUS} ($V_{BUS} > V_{SUP}$).

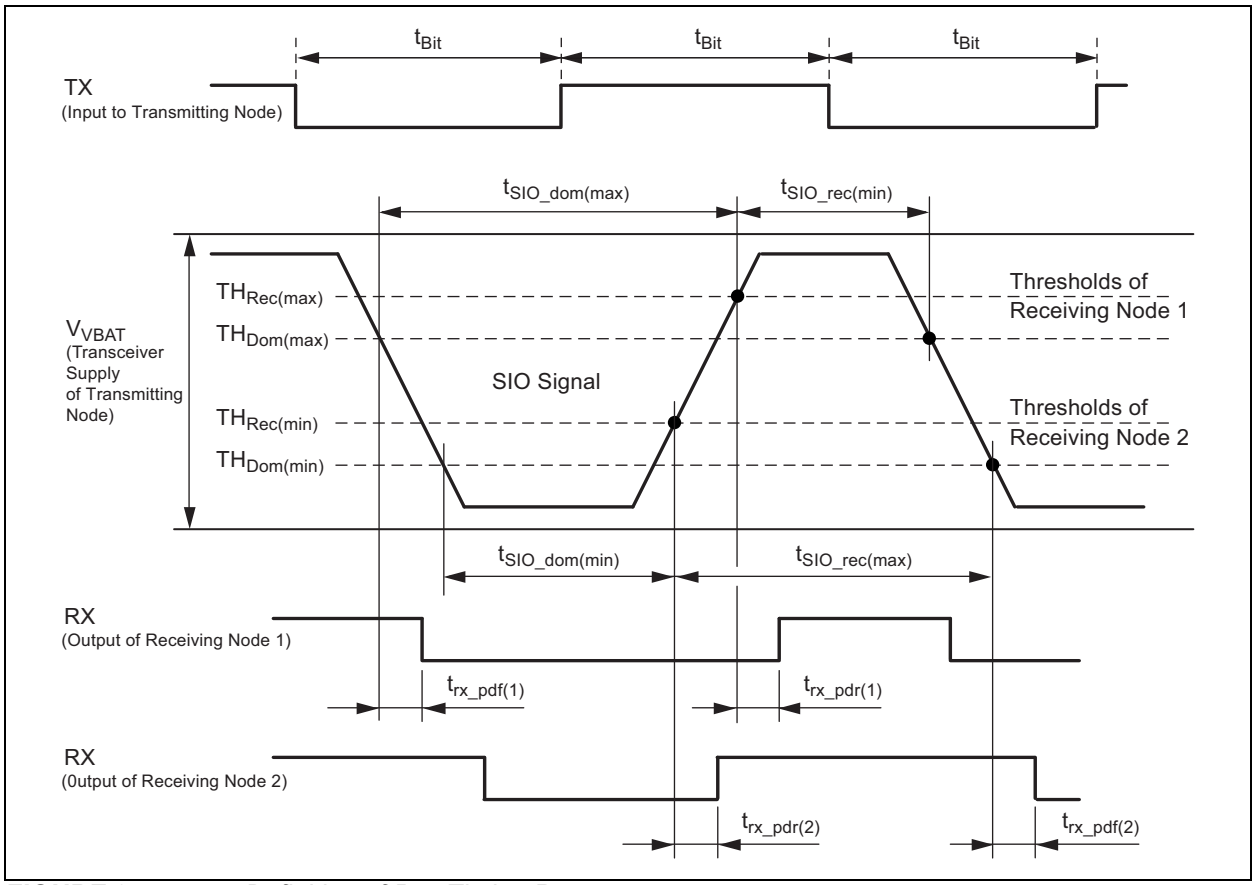


FIGURE 3-5: *Definition of Bus Timing Parameters.*

3.5 Control Inputs DIR and PWM

3.5.1 DIR PIN

The DIR pin is used as a logical input to control the direction of the external motor to be controlled by the IC. An internal pull-down resistor is included.

3.5.2 PWM PIN

The PWM pin is used as a logical input for PWM information delivered by the external microcontroller. Duty cycle and frequency at this pin are passed through to the H-bridge. An internal pull-down resistor is included.

TABLE 3-1: STATUS OF THE IC DEPENDING ON CONTROL INPUTS AND DETECTED FAILURES

Control Inputs			Driver Stage for External Power MOS				Comments
ON	DIR	PWM	H1	L1	H2	L2	
0	x	x	OFF	OFF	OFF	OFF	DG1, DG2 Fault or $\overline{\text{RESET}}$
1	0	PWM	ON	OFF	$\overline{\text{PWM}}$	PWM	Motor PWM Forward
1	1	PWM	$\overline{\text{PWM}}$	PWM	ON	OFF	Motor PWM Reverse

The internal signal ON is high when:

- At least one valid WD trigger has been accepted.
- No short circuit has been detected.
- V_{PBAT} is inside the specified range ($V_{PBAT\_OV} \leq V_{PBAT} \leq V_{THOV}$).
- V_{VBAT} is higher than V_{THUV}.
- The device temperature is not above the shutdown threshold.

In case of a short circuit, the appropriate transistor is switched off after a blanking time of t_{SC}. In order to avoid cross-current through the bridge, a cross-conduction timer is implemented. Its time constant is programmable by using an RC combination.

TABLE 3-2: STATUS OF THE DIAGNOSTIC OUTPUTS

Device Status						Diagnostic Outputs			Comments
PBAT_UV	SC	VBAT_UV	PBAT_OV	CPOK	OT	DG1	DG2	DG3	
x	x	x	x	1	1	—	—	1	Overtemperature Warning
x	x	x	0	x	x	0	1	—	Charge Pump Failure
x	x	1	x	x	x	0	1	—	Overvoltage P_{BAT}
x	x	x	x	x	x	0	1	—	Undervoltage V_{BAT}
x	1	0	1	x	x	1	0	—	Short Circuit
1	0	0	1	x	x	1	1	—	Undervoltage P_{BAT}

Note: Status of the diagnostic outputs depends on device status: x = don't care, no effect;
PBAT_UV = Undervoltage P_{BAT} pin; SC = Short-Circuit drain source monitoring;
VBAT_UV = Undervoltage of V_{BAT} pin; PBAT_OV = Overvoltage of P_{BAT} pin; CPOK = Charge Pump OK;
OT = Overtemperature warning.

3.6 VG Regulator

The VG regulator is used to generate the gate voltage for the low-side driver. Its output voltage will be used as an input for the charge pump, which generates the gate voltage for the high-side driver. The purpose of the regulator is to limit the gate voltage for the external power MOS transistors to 12V. It needs a ceramic capacitor of 470 nF for stability. The output voltage is reduced if the supply voltage at the V_{BAT} pin falls below 12V.

3.7 Charge Pump

The integrated charge pump is needed to supply the gates of the external power MOS transistors. It needs a shuffle capacitor of 220 nF and a reservoir capacitor of 470 nF. Without load, the output voltage on the reservoir capacitor is V_{VBAT} plus VG. The charge pump is clocked with a dedicated internal oscillator of 100 kHz. The charge pump is designed to reach a good EMC level. The charge pump will be switched off for $V_{VBAT} > V_{THOV}$.

3.8 Thermal Shutdown

There is a thermal shutdown block implemented. With rising junction temperature, a first warning level will be reached at +180°C. At this point, the ATA6824C stays fully functional and a warning will be sent to the microcontroller. At junction temperature +200°C, the drivers for H1, H2, L1, L2, SIO and the V_{CC} regulator will be switched off and a Reset occurs.

3.9 H-Bridge Driver

The device includes two push-pull drivers for control of two external power NMOS used as high-side drivers and two push-pull drivers for control of two external power NMOS used as low-side drivers. The drivers are able to be used with standard and logic-level power NMOS.

The drivers for the high-side control use the charge pump voltage to supply the gates with a voltage of VG above the battery voltage level. The low-side drivers are supplied by VG directly. It is possible to control the external load (motor) in the forward and reverse direction (see Table 3-1). The duty cycle of the PMW controls the speed. A duty cycle of 100% is possible in both directions.

3.9.1 CROSS-CONDUCTION TIME

To prevent high peak currents in the H-bridge, a non-overlapping phase for switching the external power NMOS is realized. An external RC combination defines the cross conduction time in the following way:

t_{CC} (µs) = 0.41 × R_{CC} (kΩ) × C_{CC} (nF)
(tolerance: ±5%, ±0.15 µs)

The RC combination is charged to 5V and the switching level of the internal comparator is 67% of the start level.

The resistor R_{CC} must be greater than 5 kΩ and should be as close as possible to 10 kΩ. The C_{CC} value must be ≤ 5 nF. It is recommended to use COG capacitor material.

The time measurement is triggered by the PWM or DIR signal crossing the 50% level.

The delays, t_{HxLH} and t_{LxLH}, include the cross-conduction time, t_{CC}.

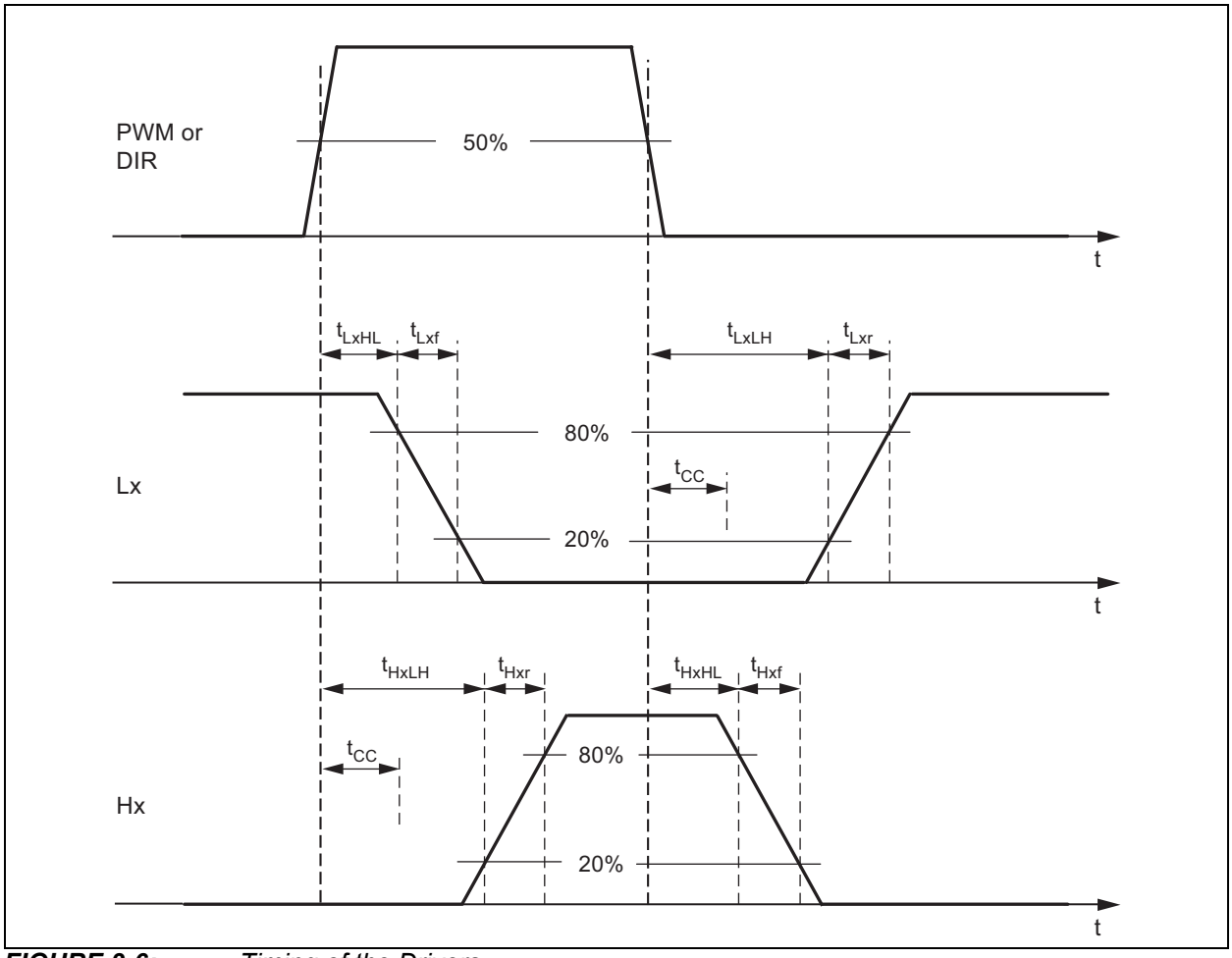


FIGURE 3-6: *Timing of the Drivers.*

3.10 Short-Circuit Detection

To detect a short circuit in the H-bridge circuitry, internal comparators detect the voltage difference between the source and the drain of the external power NMOS. If the transistors are switched on, and the voltage difference between the source and the drain is higher than the value V_{SC} (4V with tolerances), the diagnosis pin DG1 will be set to 'H' and the drivers will be switched off. All gate driver outputs (Hx and Lx) will be set to 'L'. Releasing the gate driver outputs will set DG1 back to 'L'. With the next transition on the PWM pin, the corresponding drivers, depending on the DIR pin, will be switched on again.

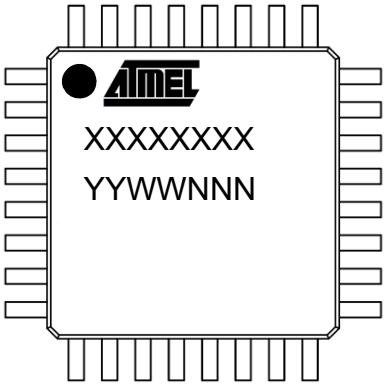
There is a P_{BAT} supervision block implemented to detect the possible voltage drop on P_{BAT} during a short circuit. If the voltage at P_{BAT} falls under V_{PBAT_OK}, the drivers will be switched off and DG1 will be set to 'H'. It will be cleared as soon as the P_{BAT} undervoltage condition disappears.

The detection of drain source voltage exceedance is activated after the short-circuit blanking time, t_{SC}. The short-circuit detection of P_{BAT} failures operates immediately.

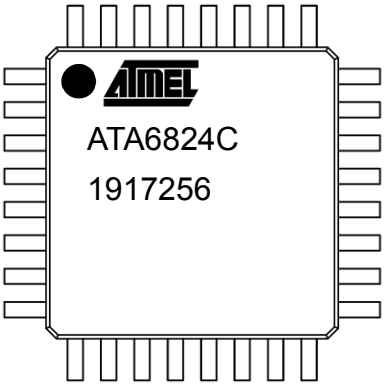
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

32-Lead 7×7 mm TQFP



Example

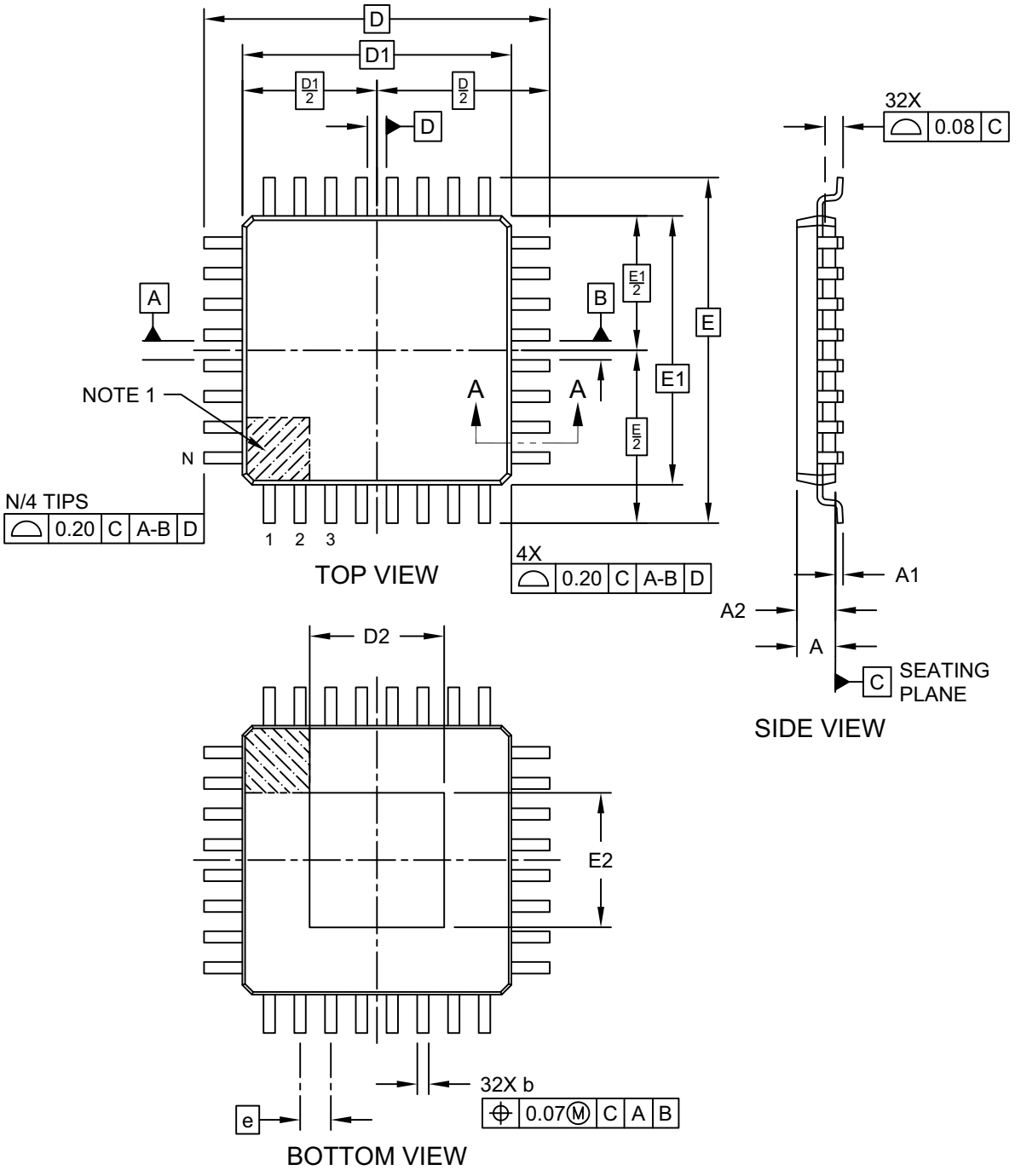


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

32-Lead Plastic Thin Quad Flatpack (3CB) - 7x7x1.0 mm Body [TQFP]
With 3.5x3.5 mm Exposed Pad; Atmel Legacy Global Package Code ADL

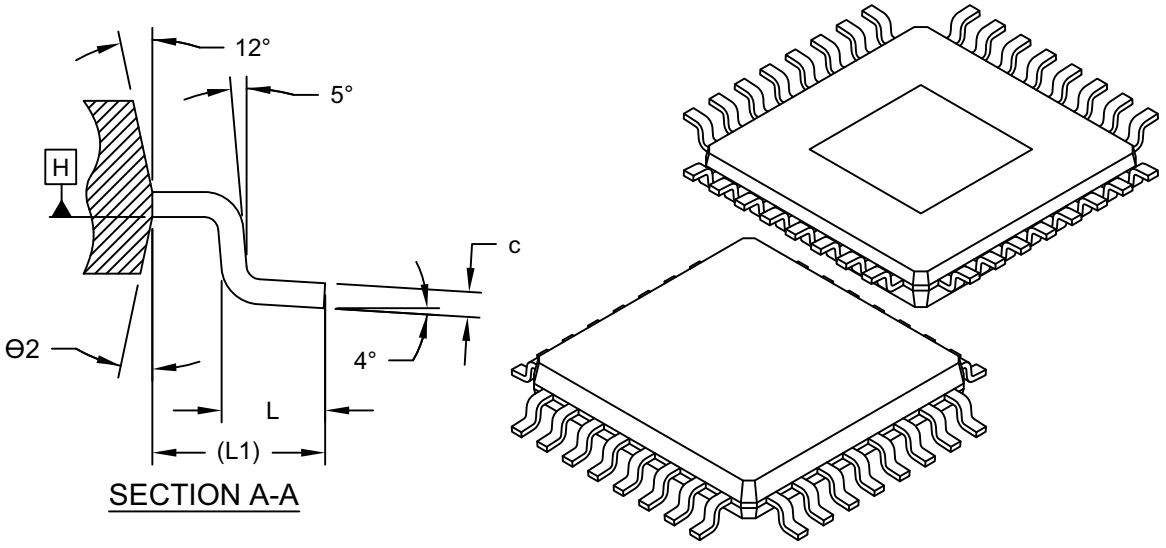
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21018 Rev A Sheet 1 of 2

32-Lead Plastic Thin Quad Flatpack (3CB) - 7x7x1.0 mm Body [TQFP] With 3.5x3.5 mm Exposed Pad; Atmel Legacy Global Package Code ADL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		9.00 BSC	
Molded Package Length	D1		7.00 BSC	
Exposed Pad Length	D2	3.40	3.50	3.60
Overall Width	E		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Exposed Pad Width	E2	3.40	3.50	3.60
Terminal Width	b	0.30	0.37	0.45
Terminal Thickness	c	0.09	-	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	-
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Terminal-to-Exposed-Pad	Θ2	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
3. BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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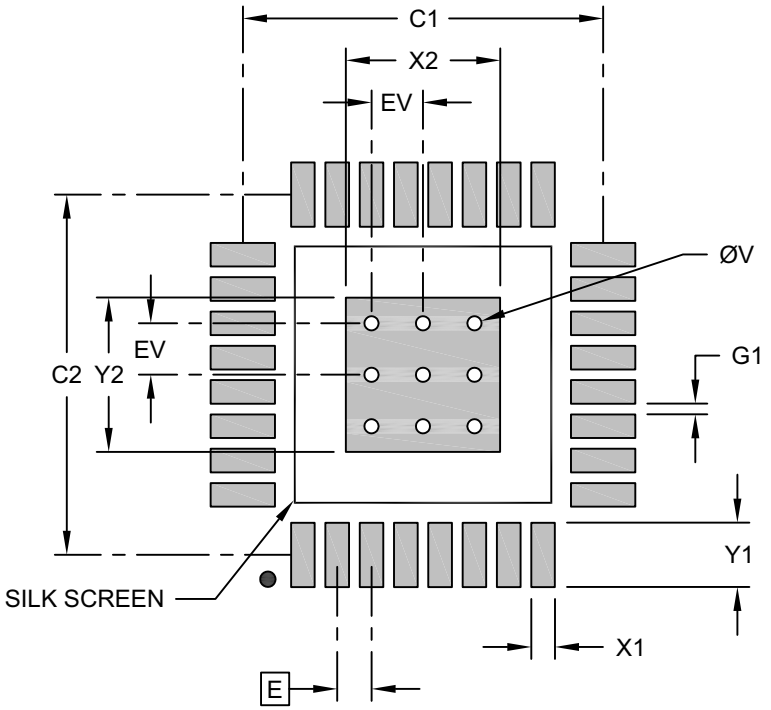
32-Lead Plastic Thin Quad Flatpack (3CB) - 7x7x1.0 mm Body [TQFP] With 3.5x3.5 mm Exposed Pad; Atmel Legacy Global Package Code ADL

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Optional Center Pad Width	X2			3.60
Optional Center Pad Length	Y2			3.60
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X32)	X1			0.55
Contact Pad Length (X32)	Y1			1.50
Contact Pad to Contact Pad (X28)	G1	0.25		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23018 Rev A

APPENDIX A: REVISION HISTORY

Revision A (June 2019)

- Original release of this document.
- This document replaces Atmel 9212G-AUTO-09/13.
- Updated Parameter 5.7, ‘Driver Dominant Voltage $V_{BUSdom\_DRV\_HiSUP}$’, in the **Electrical Characteristics** table.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-	X	XX	X	-	X
Device		Mask	Package Type	Compound		Assembly Location

Device:	ATA6824C = High-Temperature H-Bridge Motor Driver
Mask:	M = 75007
Package Type:	FH = TQFP (Plastic Thin Quad Flatpack)
Compound:	W = Green Mold Compound

Examples:

a) ATA6824C-MFHW-1 = 32-Lead High-Temperature H-Bridge Motor Driver, 75007 Mask, Green Mold Compound, TQFP Package.

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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